6 CHANNEL ESD PROTECTION ARRAY WITH ZENER SUPPLY CLAMP

Features

- Six channels of ESD protection
- Integral Zener diode clamp to suppress supply rail transient
- 15KV ESD protection (HBM)
- 8KV contact, 15KV air ESD protection per IEC 61000-4-2
- Low loading capacitance, 3pF typ
- Miniature 8-pin MSOP or SOIC package

Applications

- I/O port protection for cellular phones, notebook computers, PDAs, etc.
- ESD protection for VGA (Video) port in PC's or Notebook computers.
- ESD protection for sensitive electronic equipment.

Product Description

The PAC™ DN016 is a diode array designed to provide 6 channels of ESD protection for electronic components or sub-systems. Each channel consists of a pair of diodes which steers the ESD current pulse either to the positive (V_P) or negative (V_N) supply. In addition, there is an integral Zener diode between V_P and V_N to suppress any voltage disturbance due to these ESD current pulses. The PAC DN016 will protect against ESD pulses up to 15KV Human Body Model, and 8KV contact discharge per International Standard IEC 61000-4-2.

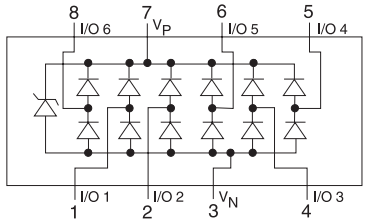
This device is particularly well-suited for portable electronics (e.g. cellular phones, PDAs, notebook computers) because of its small package footprint, high ESD protection level, and low loading capacitance. It is also suitable for protecting video output lines and I/O ports in computers and peripheral equipment.

ABSOLUTE MAXIMUM RATINGS

Diode Forward DC Current (Note 1)	20mA
Storage Temperature	-65°C to 150°C
Operating Temperature Range	-20°C to 85°C
DC Voltage at any Channel Input	V_N-0.5V to V_P+0.5V

Note 1: Only one diode conducting at a time.

SCHEMATIC CONFIGURATION



STANDARD SPECIFICATIONS

Parameter	Min.	Typ.	Max.
Operating Supply Voltage (V_P-V_N)			5.5V
Supply Current @ V_P-V_N = 5.5V			20µA
Diode Forward Voltage, I_F = 20mA, T = 25°C	0.65V		0.95V
Zener clamp reverse breakdown voltage @ 1mA, T = 25°C		6.6V	
ESD Protection Peak Discharge Voltage at any Channel Input, in-system (Note 2) Human Body Model, Method 3015 (Note 3, 4) Contact Discharge per IEC 61000-4-2 (Note 5)	 ±15KV ±8KV		
Channel Clamp Voltage @ 15KV ESD HBM, T = 25°C (Notes 3, 4) Positive transients Negative transients			 V_P + 13.0V V_N - 13.0V
Channel Leakage Current, T = 25°C		±0.1µA	±1.0 µA
Channel Input Capacitance (Measured @ 1 MHz) V_P = 5V, V_N = 0V, V_{INPUT} = 2.5V (Note 4)		3pF	6pF
Package Power Rating SOIC Package MSOP Package			 350mW 200mW

Note 2: From I/O pins to V_P or V_N only. Bypass opacitor between V_P and V_N is not required. However, a 0.2 µF ceramic chip capacitor bypassing V_P to V_N is recommended if the lowest possible channel clamp voltage is desired.

Note 3: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge}$=100pF, $R_{Discharge}$=1.5KΩ, V_P=5.0V, V_N=GND.

Note 4: This parameter is guaranteed by design and characterization.

Note 5: Standard IEC 61000-4-2 with $C_{Discharge}$=150pF, and $R_{Discharge}$=330Ω, V_P=5V, V_N=GND.

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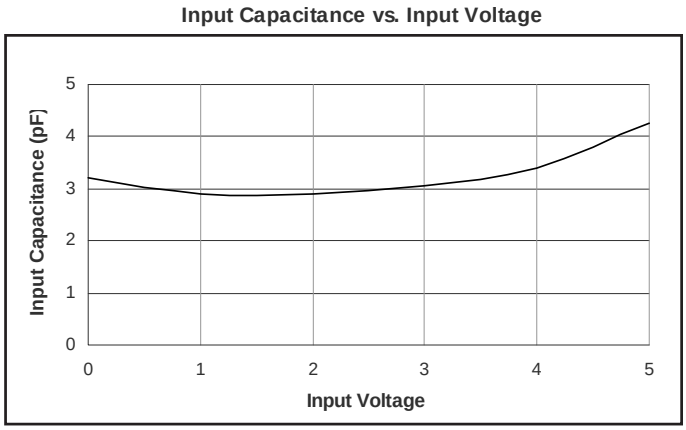

Typical variation of C_{IN} with V_{IN} (V_P=5V, V_N=0V)
(V_P = 5V, V_N = 0V, 0.1µF chip capacitor between V_P & V_N)

STANDARD PART ORDERING INFORMATION		
Package		Ordering Part Number
Pins	Style	Part Marking
8	SOIC	PACDN016S
8	MSOP	PACDN016M

When placing an order please specify desired shipping: Tubes or Tape & Reel.

Application Information

See also California Micro Devices Application note AP209, "Design Considerations for ESD protection."

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances to the Supply and Ground rails. Refer to Figure 1, which illustrates the case of a positive ESD pulse applied between an input channel and Chassis Ground. The parasitic series inductance back to the power supply is represented by L_1. The voltage V_Z on the line being protected is:

V_Z = Forward voltage drop of D_1 + L_1 x $d(I_{esd})/dt$ + V_{Supply}

where I_{esd} is the ESD current pulse, and V_{Supply} is the positive supply voltage.

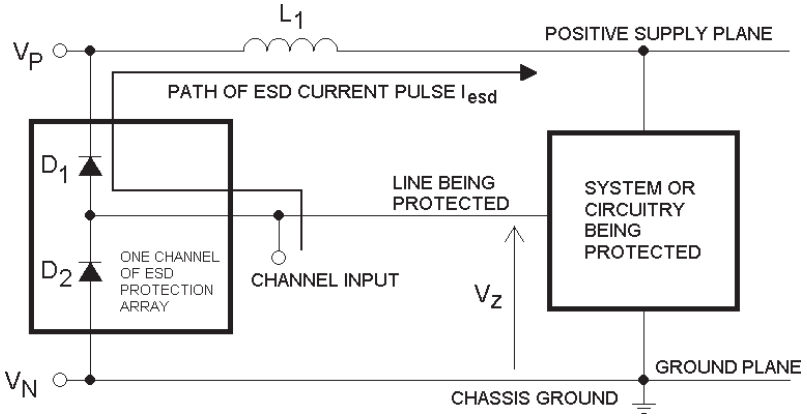

Figure 1

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC 61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1nS. Here $d(I_{esd})/dt$ can be approximated by $\Delta I_{esd}/\Delta t$, or $30/(1x10^{-9})$. So just 10nH of series inductance (L_1) will lead to a 300V increment in V_Z!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

Another consideration is the output impedance of the power supply for fast transient currents. Most power supplies exhibit a much higher output impedance to fast transient current spikes. In the V_Z equation above, the V_{Supply} term, in reality, is given by ($V_{DC} + I_{esd} \times R_{out}$), where V_{DC} and R_{out} are the nominal supply DC output voltage and effective output impedance of the power supply respectively. As an example, a R_{out} of 1 ohm would result in a 10V increment in V_Z for a peak I_{esd} of 10A.

To mitigate these effects, a Zener diode has been integrated into this Protection Array between V_P and V_N. This Zener diode clamps the maximum voltage of V_P relative to V_N at the breakdown voltage of the Zener diode. Although not strictly necessary, it is recommended that V_P be bypassed to the ground plane with a high frequency bypass capacitor. This will lower the channel clamp voltage, and is especially effective when V_P is much lower than the Zener breakdown voltage. The value of this bypass capacitor should be chosen such that it will absorb the charge transferred by the ESD pulse with minimal change in V_P. Typically a value in the 0.1 μF to 0.2 μF range is adequate for IEC-61000-4-2 level 4 contact discharge protection (8KV). For higher ESD voltages, the bypass capacitor should be increased accordingly. Ceramic chip capacitors mounted with short printed circuit board traces are good choices for this application. Electrolytic capacitors should be avoided as they have poor high frequency characteristics.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply and ground planes to minimize stray series inductance.

Figure 5