Ordering number : ENA1860

SANYO Semiconductors
DATA SHEET

LC88F5LA4ACS — CMOS IC FROM 96K byte, RAM 6K byte on-chip 16-bit 1-chip Microcontroller

Overview

The SANYO LC88F5LA4ACS is a 16-bit microcomputer that, centered around an Xstromy16 CPU, integrates on a single chip a number of hardware features such as 96K-byte flash ROM (onboard programmable), 6K-byte RAM, six 16-bit timers, a base timer serving as a time-of-day clock, a real time clock, two synchronous SIO interfaces with automatic transmission capability, a single master I^2C/synchronous SIO interface, a slave I^2C/synchronous SIO interface, two asynchronous SIO (UART) interfaces, a 4-channel 12-bit resolution AD converter, a watchdog timer, a system clock frequency divider, a 38-source (24 modules) 13-vector interrupt feature, and on-chip debugger feature.

Features

■Xstromy16 CPU
- 4G-byte address space
- General-purpose registers: 16 bits × 16registers

■Flash ROM
- Capable of onboard programming with a wide range of voltage levels (2.6 to 3.6V).
- Block-erasable in 128 or 1K byte units.
- Data written in 2-byte units.
- 98304 × 8 bits

■RAM
- 6144 × 8 bits

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■Minimum instruction cycle time (tCYC)
- 100ns (10MHz) V_{DD} = 2.6 to 3.6V
- 250ns (4MHz) V_{DD} = 2.2 to 3.6V

■Ports
- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1 bit units : 33 (P0n P1n, P20 to P25, P3n, P60 to P62)
- Oscillation/normal withstand voltage I/O ports : 2 (PC0, PC1)
- Oscillation pins : 2 (CF1, CF2)
- Reset pins : 1 (RESB)
- TEST pins : 1 (TEST)
- Power pins : 7 (V_{SS}1 to 2, V_{SS}A, V_{DD}1 to 3, V_{DD}A)

■Timers
- Timer 0: 16-bit timer that supports PWM/toggle outputs
  1) 5-bit prescaler
  2) 8-bit PWM × 2, 8-bit timer + 8-bit PWM mode selectable
  3) Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 1: 16-bit timer with capture registers
  1) 5-bit prescaler
  2) May be divided into 2 channels of 8-bit timer
  3) Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 2: 16-bit timer with capture registers
  1) 4-bit prescaler
  2) May be divided into 2 channels of 8-bit timer
  3) Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 3: 16-bit timer that supports PWM/toggle outputs
  1) 8-bit prescaler
  2) 8-bit timer × 2ch or 8-bit timer + 8-bit PWM mode selectable
  3) Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 4: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 0
- Timer 5: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 0
  * Prescaler 0 and 1 are consisted of 4 bits and can choose their clock source from OSC0 or OSC1.
- Base timer
  1) Clock may be selected from OSC0 (32.768kHz crystal oscillator) and frequency-divided output of system clock.
  2) Interrupts can be generated in 7 timing schemes.

■Real time clock
1) Calender with Jan. 1, 2000 to Dec.31, 2799 including automatic leap year calculation function.
2) Consisted of Independent second- minute-hour-day-month-year-century counters.
3) Programmable count-clock calibration function.

■Serial interfaces

- SIO0: 8-bit synchronous SIO
  1) LSB first/MSB first mode selectable
  2) Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  3) Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  4) Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  5) Interval function (intervals specifiable in 0 to 64 tSCK units)
  6) Wakeup function
- SIO1: 8-bit synchronous SIO
  1) LSB first/MSB first mode selectable
  2) Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  3) Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  4) Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  5) Interval function (intervals specifiable in 0 to 64 tSCK units)
  6) Wakeup function
- SMIIC0: Single master I^2C/8-bit synchronous SIO
  Mode 0: Single-master mode communication
  Mode 1: Synchronous 8-bit serial I/O (MSB first)
- SLIIC0: Slave I^2C/8-bit synchronous SIO
  Mode 0: I^2C slave mode communication
  Mode 1: Synchronous 8-bit serial I/O (MSB first)
  Note: usable only with the external clock source
- UART0
  1) Data length : 8 bits (LSB first)
  2) Start bits : 1 bit
  3) Stop bits : 1 bit
  4) Parity bits : None/even parity/odd parity
  5) Transfer rate : 4/8 cycle
  6) Baudrate source clock: P07 input signal used as a 1 cycle signal (T0PWMH can be used as a clock source) or Timer 4 cycle.
  7) Full duplex communication
  Note: The “cycle” refers to one period of the baudrate clock source.
- UART2
  1) Data length : 8 bits (LSB first)
  2) Start bits : 1 bit
  3) Stop bits : 1/2 bit
  4) Parity bits : None/even parity/odd parity
  5) Transfer rate : 8 to 4096 cycle
  6) Baudrate source clock : System clock/OSC0/OSC1/P25 input signal
  7) Wakeup function
  8) Full duplex communication
  Note: The “cycle” refers to one period of the baudrate clock source.

■AD converter
1) 12/8 bits resolution selectable
2) Analog input: 14 channels
3) Comparator mode

■Watchdog timer
1) Driven by the base timer + internal watchdog timer dedicated counter
2) Interrupt or reset mode selectable

■Interrupts (peripheral function)
- 38 sources (24 modules), 13 vector addresses

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Module
1	08000H	Watchdog timer (1)
2	08004H	Base timer (2)
3	08008H	Timer 0 (2)
4	0800CH	INT0 (1)
5	08014H	INT1 (1)
6	08018H	INT2 (1)/timer 1 (2)/UART2 (4)
7	0801CH	INT3 (1)/timer 2 (4)/SMIIC0 (1)/SLIIC1 (1)
8	08020H	INT4 (1)/timer 3 (2)
9	08024H	INT5 (1)/timer 4 (1)/SIO1 (2)
10	08030H	ADC (1)/timer 5 (1)
11	08034H	INT6 (1)
12	08038H	INT7 (1)/SIO0 (2)/SIO0(2)
13	0803CH	Port 0 (3)/RTC (1)

- 3 priority levels selectable.
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- A number enclosed in parentheses denotes the number of sources.

■Subroutine Stack: 6K-byte RAM area
- Subroutine calls that automatically save PSW, interrupt vector calls: 6 bytes
- Subroutine calls that do not automatically save PSW: 4 bytes

■Multiplication/division instructions
- 16 bits × 16 bits (18 tCYC execution time)
- 16 bits ÷ 16 bits (18 to 19 tCYC execution time)
- 32 bits ÷ 16 bits (18 to 19 tCYC execution time)

■Oscillator circuits
- RC oscillator circuit (internal): For system clock
- CF oscillator circuit (built-in Rf circuit): For system clock (OSC1)
- VMRC oscillator circuit: For system clock (OSC1)
- Crystal oscillator circuit (built-in Rf circuit): For low-speed system clock (OSC0)
- SLRC oscillator circuit (internal): For system clock (In the case of exception processing)

■System clock divider function
- Can run on low current.
- 1/1 to 1/128 of the system clock frequency can be set.

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Released by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) OSC1, RC and OSC0 oscillators automatically stop.
  2) There are the six ways of releasing the HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, INT2, INT3, INT4, INT5, INT6, and INT7 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt established at SIO0 or SIO1
     (5) Having an interrupt established at UART2
- HOLDX mode: Suspends instruction execution and the operation of the peripheral circuits except those which run on OSC0.
  1) OSC1 and RC oscillations automatically stop.
  2) OSC0 maintains the state that is established when the HOLDX mode is entered.
  3) There are seven ways of releasing the HOLDX mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, INT2, INT3, INT4, INT5, INT6, and INT7 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established at the base timer circuit
     (5) Having an interrupt established at SIO0 or SIO1
     (6) Having an interrupt established at UART2

     .

■On-chip debugger function

- Supports software debugging with the IC mounted on the target board.
- Supports source line debugging and tracing functions, and breakpoint setting and real time display.
- Single-wire communication

■Power supply voltage

- $V_{DD}1, 2$: 2.2 to 3.6V.
- $V_{DD}3$: (I/O) 1.6 to 3.6V.

* Voltage of $V_{DD}3$ must be lower than $V_{DD}1$.

■Package Form

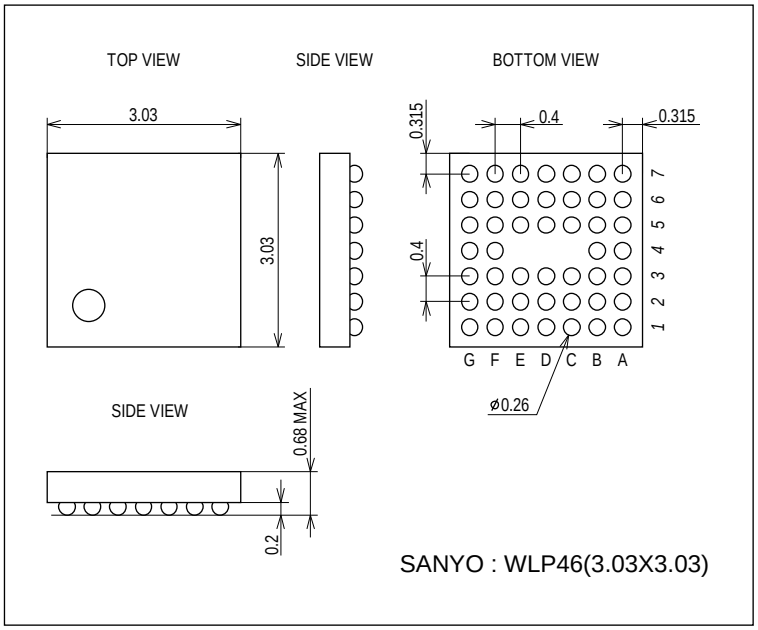
- WLP46 (3.03 × 3.03): Lead-free and halogen-free type

■Development Tools

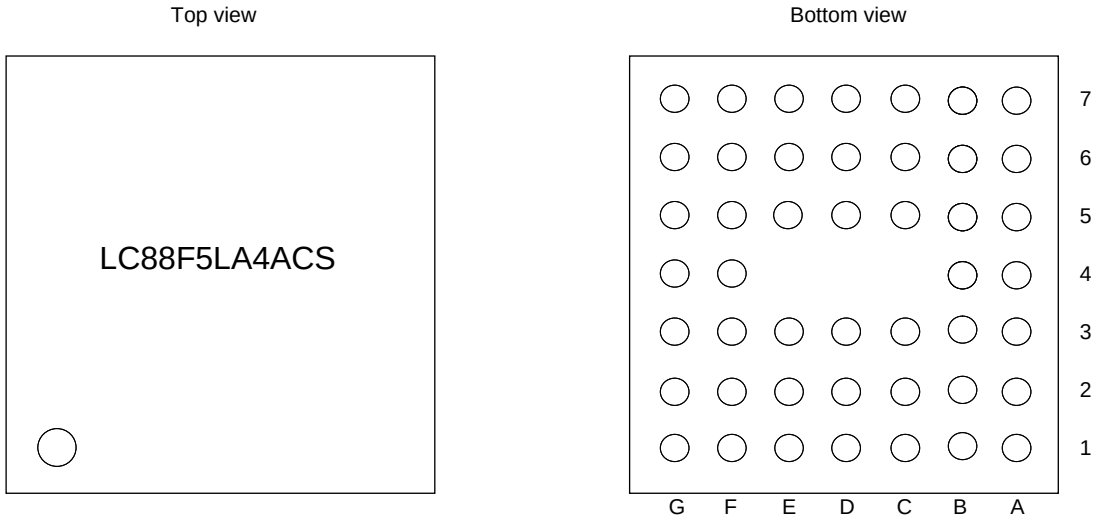
- On-chip debugger: EOCUIF1 + LC88F5LA4A

Package Dimensions

unit : mm (typ)
3404



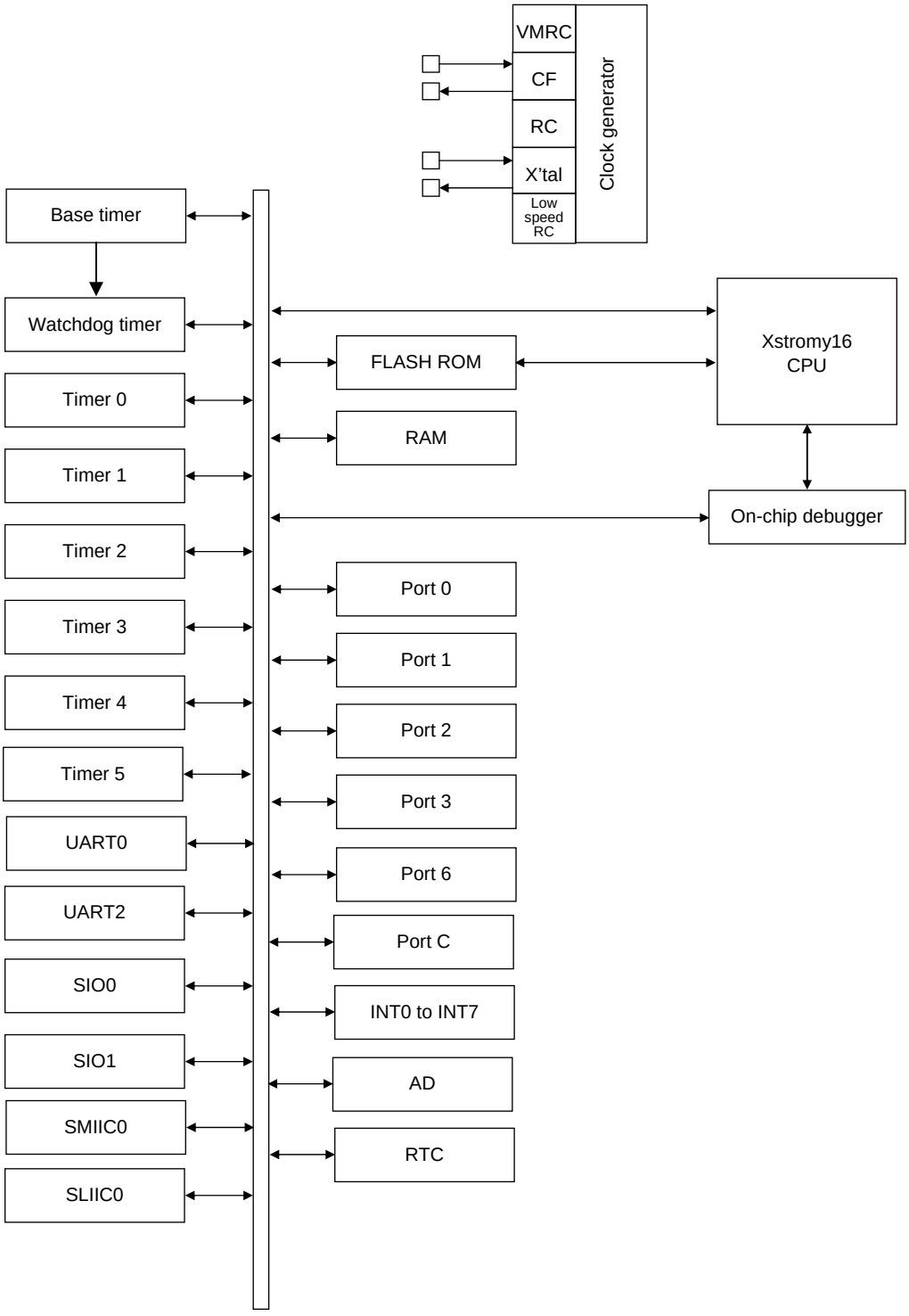
Pin Assignment



SANYO: WLP46 (3.03×3.03) (Lead-free and halogen-free type)

No.	Name	No.	Name	No.	Name
G1	TEST	B4	P04/P04INT	F7	P12/SCK0
E2	RESB	D3	P05/P05INT	F6	P13/U0TX
F1	$V_{SS}A$	A5	P06/T0PWML	G7	P14/T3OL/U0RX/INT2
E1	$V_{SS}1$	B5	P07/T0PWMH/U0BRG	E5	P15/T3OH/INT3
D2	PC0/XT1	A6	P37/T4O	G6	P16/U2RX
D1	PC1/XT2	C5	P36/SCK1	F5	P17/U2TX
C1	$V_{DD}1$	A7	P35/SI1/SB1	G5	P62
C2	$V_{DD}A$	B6	P34/SO1	F4	$V_{DD}3$
B1	CF1	B7	P33/SM0DA	G4	P20/INT4
A1	CF2	C6	P32/SM0CK	E3	P21/INT5
B2	P00/P0INT/AN0	C7	P31/INT1/SM0DO	G3	P22/SL0CK
A2	P01/P0INT/AN1	D6	$V_{DD}2$	F3	P23/SL0DA
B3	P60/AN2	D7	$V_{SS}2$	G2	P24/SL0DO/INT6
A3	P61/AN3	D5	P30/INT0	F2	P25/INT7/T5O
C3	P02/P0INT	E7	P10/SO0		
A4	P03/P0INT	E6	P11/SI0/SB0		

System Block Diagram



Pin Description

Pin Name	I/O	Description
$V_{SS}1$, $V_{SS}2$	-	- Power supply
$V_{SS}A$	-	- Power supply for AD
$V_{DD}1$, $V_{DD}2$	-	+ Power supply
$V_{DD}3$	-	+ Power supply for port2's I/O
$V_{DD}A$	-	+ Power supply for AD
Port 0 P00 to P07	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • HOLD release input (P00 to P03, P04, P05) • Port 0 interrupt input (P00 to P03, P04, P05) • Pin functions AN0 (P00) to AN1 (P01): AD converter input port P06: Timer 0L output P07: Timer 0L output/UART0 clock input
Port 1 P10 to P17	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P10: SIO0 data output P11: SIO0 data input/pulse input/output P12: SIO0 clock input/output P13: UART0 transmit P14: Timer 3L output/UART0 receive/ INT2 input/HOLD release/timer 2 event input/timer 2L capture input P15: Timer 3H output/ INT3 input/HOLD release/timer 2 event input/timer 2H capture input P16: UART2 receive P17: UART2 transmit Interrupt acknowledge type INT2, INT3: H level, L level, H edge, L edge, both edges
Port 2 P20 to P25	I/O	• 6-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P20: INT4 input/HOLD release input/timer 3 event input/timer 2L capture input/timer 2H capture input P21: INT5 input/HOLD release input/timer 3 event input/timer 2L capture input/timer 2H capture input P22: SLIIC0 clock input/output P23: SLIIC0 bus input/output/data input P24: SLIIC0 data output (used in 3-wire SIO mode)/ INT6 input/HOLD release input P25: Timer 5 output/ INT7 input/HOLD release input Interrupt acknowledge type INT4, INT5, INT6, INT7: H level, L level, H edge, L edge, both edges
Port 3 P30 to P37	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P30: INT0 input/HOLD release/timer 2L capture input P31: INT1 input/HOLD release/timer 2H capture input/SMIIC0 data output (used in 3-wire SIO mode) P32: SMIIC0 clock input/output P33: SMIIC0 bus input/output/data input P34: SIO1 data output P35: SIO1 data input/bus input/output P36: SIO1 clock input/output P37: Timer 4 output Interrupt acknowledge type INT0, INT1: H level, L level, H edge, L edge, both edges

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Pin Name	I/O	Description
Port 6 P60 to P62	I/O	• 3-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions AN2 (P60) to AN3 (P61): AD converter input port
Port C PC0 to PC1	I/O	• 2-bit I/O port • I/O specifiable in 1-bit units • Pin functions PC0: 32.768kHz crystal oscillator input (XT1) PC1: 32.768kHz crystal oscillator output (XT2)
TEST	I/O	• TEST pin • Used to communicate with on-chip debugger. • Connects an external 100kΩ pull-down resistor.
RESB	I	Reset pin
CF1	I	Ceramic resonator input pin
CF2	O	Ceramic resonator output pin

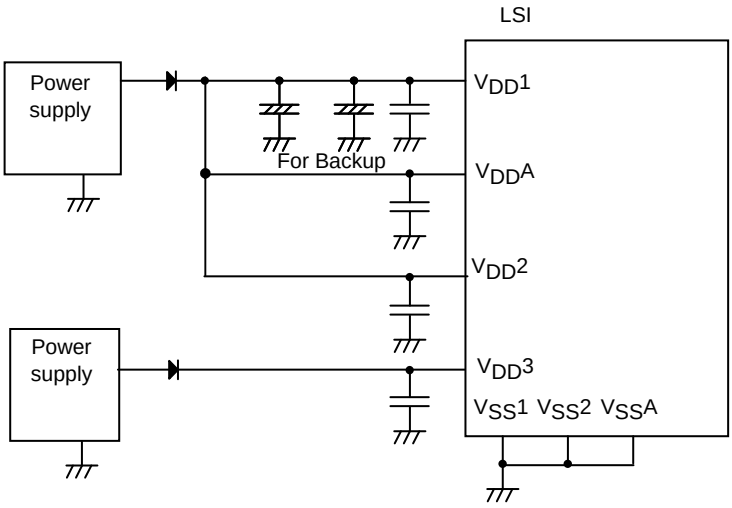
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

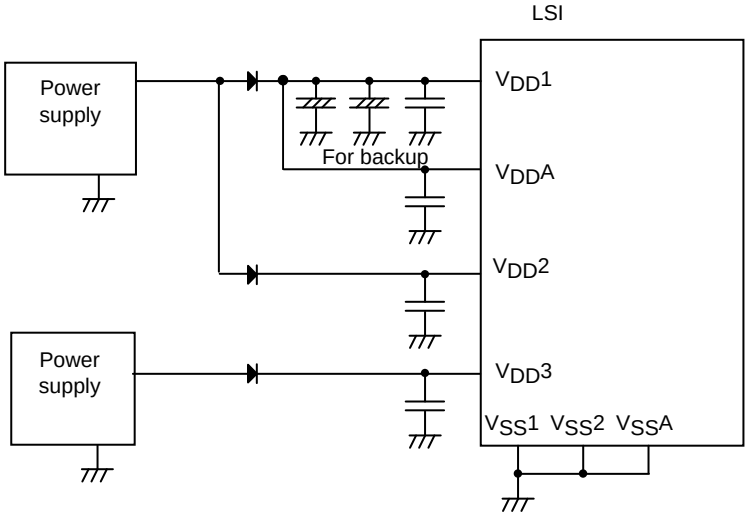
Port Name	Option Selected in Units of	Output Type	Pull-up Resistor
P00 to P07 P60 to P62	1 bit	CMOS	Programmable
P10 to P17 P20 to P25 P30 to P37		Able to program special functions' output type from CMOS output or Nch-opendrain	
PC0	-	N-channel open drain (32.768kHz crystal oscillator input)	None
PC1	-	Nch-open drain (32.768kHz crystal oscillator output)	None

* Make the following connection to minimize the noise input to the $V_{DD}1$ pin and prolong the backup time.
* Power supply must be $V_{DD}1 \leq V_{DD}3$.
* Be sure to electrically short the $V_{SS}1$, $V_{SS}2$ and $V_{SS}A$ pins.

Example 1: When data is being backed up in the HOLD mode, the H level signals to the output ports are fed by the backup capacitors.



Example 2: When data is being backed up in the HOLD mode, the H level output at any ports is not sustained and is unpredictable.



Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}A = 0V$

Parameter		Symbol	Applicable Pin /Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}A$	$V_{DD}1=V_{DD}2=V_{DD}A$		-0.3		+4.0	V
		$V_{DD}3$ max	$V_{DD}3$	$V_{DD}3 \leq V_{DD}$		-0.3		+4.0	
Input voltage		V_I(1)	CF1, RESB			-0.3		V_{DD} +0.3	
Input/output voltage		V_{IO}(1)	Ports 0, 1, 3 Port 6 PC0, PC1			-0.3		V_{DD} +0.3	
		V_{IO}(2)	Ports 2	$V_{DD}3 \leq V_{DD}$		-0.3		$V_{DD}3$ +0.3	
High level output current	Peak output current	IOPH (1)	P04 to P07, P62 Ports 1, 2, 3	CMOS output selected Per applicable pin		-7.5			mA
		IOPH (2)	P00 to P03 P60 to P61	Per applicable pin		-4.5			
	Average output current (Note 1-1)	IOMH (1)	P04 to P07, P62 Ports 1, 2, 3	CMOS output selected Per applicable pin		-5			
		IOMH (2)	P00 to P03 P60 to P61	Per applicable pin		-2.5			
	Total output current	ΣIOAH (1)	P60 to P61 P00 to P03	Total of currents at applicable pins		-10			
		ΣIOAH (2)	P04 to P07 P31 to p37	Total of currents at applicable pins		-15			
		ΣIOAH (3)	Port 1 P30, P62	Total of currents at applicable pins		-15			
		ΣIOAH (4)	P04 to P07, P62 Ports 1, 3	Total of currents at applicable pins		-30			
		ΣIOAH (5)	Port 2	Total of currents at applicable pins		-15			

Note 1-1: Average output current refers to the average of output currents measured for a period of 100ms.

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Parameter		Symbol	Applicable Pin /Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Low level output current	Peak output current	IOPL(1)	P04 to P07, P62 Ports 1, 2, 3	Per applicable pin				12.5	mA
		IOPL(2)	P00 to P03 P60 to P61 PC0 to PC1	Per applicable pin				7.5	
	Average output current (Note 1-1)	IOML(1)	P04 to P07, P62 Port 1, 2, 3	Per applicable pin				10	
		IOML(2)	P00 to P03 P60 to P61 PC0 to PC1	Per applicable pin				5	
	Total output current	ΣIOAL(1)	PC0 to PC1	Total of currents at applicable pins				10	
		ΣIOAL(2)	P60 to P61 P00 to P03	Total of currents at applicable pins				10	
		ΣIOAL(3)	P00 to P03 P60 to P61 PC0 to PC1	Total of currents at applicable pins				15	
		ΣIOAL(4)	P04 to P07 P31 to P37	Total of currents at applicable pins				30	
		ΣIOAL(5)	Ports 1, 2 P30, P62	Total of currents at applicable pins				60	
		ΣIOAL(6)	P04 to P07, P62 Ports 1, 2, 3	Total of currents at applicable pins				80	
Allowable power dissipation		Pd max	WLP46 (3.03×3.03)	Ta=-40 to +85°C With thermal resistance board (Note 1-2)				T.B.D	mW
Operating ambient temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: Average output current refers to the average of output currents measured for a period of 100ms.
Note 1-2: Thermal resistance board is used.

Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}A = 0V$

Parameter	Symbol	Applicable Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}A$	0.098µs≤tCYC≤66µs		2.6		3.6	V
			0.245µs≤tCYC≤66µs		2.2		3.6	
Memory sustaining supply voltage	VHD	$V_{DD}1=V_{DD}2=V_{DD}A$	RAM and register contents sustained in HOLD mode		1.8		3.6	
High level input voltage	$V_{IH}(1)$	Ports 0, 1, 3, 6		2.2 to 3.6	$0.7V_{DD}$		V_{DD}	
	$V_{IH}(2)$	CF1, RESB PC0, PC1		2.2 to 3.6	$0.75V_{DD}$		V_{DD}	
	$V_{IH}(3)$	P32, P33 I^2C side		2.2 to 3.6	$0.7V_{DD}$		V_{DD}	
	$V_{IH}(4)$	Port 2	$V_{DD}3$= 1.6V to 3.6V	2.2 to 3.6	$0.7V_{DD}3$		$V_{DD}3$	
Low level input voltage	$V_{IL}(1)$	Ports 0, 1, 3, 6		2.2 to 3.6	V_{SS}		$0.25V_{DD}$	
	$V_{IL}(2)$	CF1, RESB PC0, PC1		2.2 to 3.6	V_{SS}		$0.25V_{DD}$	
	$V_{IL}(3)$	P32, P33 I^2C side		2.2 to 3.6	V_{SS}		$0.3V_{DD}$	
	$V_{IL}(4)$	Port 2	$V_{DD}3$= 1.6V to 3.6V	2.2 to 3.6	V_{SS}		$0.3V_{DD}3$	
Instruction cycle time (Note 2-2)	tCYC			2.6 to 3.6	0.098		66	µs
				2.2 to 3.6	0.245		66	
External system clock frequency	FEXCF(1)	CF1	• CF2 pin open • System clock frequency division ratio = 1/1 • External system clock DUTY50±5%	2.6 to 3.6	0.1		10	MHz
				2.2 to 3.6	0.1		4	
			• CF2 pin open • System clock frequency division ratio = 1/2	2.6 to 3.6	0.2		20	
				2.2 to 3.6	0.2		8	

Note 2-1: V_{DD}≥2.6V must be maintained when making onboard programming into flash ROM.

Note 2-2: Relationship between tCYC and oscillation frequency is 1/FmCF when frequency division ratio is 1/1 and 2/FmCF when the ratio is 1/2.

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Parameter	Symbol	Applicable Pin /Remarks	Conditions	Specification			
			V_{DD}[V]	min	typ	max	unit
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	10MHz ceramic oscillator mode See Fig. 1.	2.2 to 3.6		10		MHz
	FmCF(2)	CF1, CF2	4MHz ceramic oscillator mode See Fig. 1.	2.2 to 3.6		4		
	FmMRC(1)		Multivaliable RC oscillation When SEL4M=0 center range setting (Note 2-4)	2.6 to 3.6	7.5	10	12.5	
	FmMRC(2)		Multivaliable RC oscillation When SEL4M=1 center range setting (Note 2-4)	2.2 to 3.6	2	4	6	
	FmRC		Internal RC oscillation	2.2 to 3.6	0.5	1.0	2.0	
	FmSLRC		Internal low-speed RC oscillation	2.2 to 3.6	18	30	45	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal oscillator mode See Fig. 2.	2.2 to 3.6		32.768		

Note 2-3: See Tables 1 and 2 for oscillator constant values.

Note 2-4: To change to a multivaliable RC oscillation as a system clock, wait more than 20μs oscllation stabilizing time after multivaliable RC oscillation is disabled to enabled.

Electrical Characteristics at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}A = 0V$

Parameter	Symbol	Applicable/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 3, 6 PC0, PC1 RESB	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (including output Tr. off leakage current)	2.2 to 3.6			1	μA
	$I_{IH}(2)$	CF1	$V_{IN}=V_{DD}$	2.2 to 3.6			15	
	$I_{IH}(3)$	Port 2	Output disabled Pull-up resistor off $V_{IN}=V_{DD}3$ $V_{DD}3$= 1.6V to 3.6V (including output Tr. off leakage current)	2.2 to 3.6			1	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 3, 6 PC0, PC1 RESB	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (including output Tr. off leakage current)	2.2 to 3.6	-1			
	$I_{IL}(2)$	CF1	$V_{IN}=V_{SS}$	2.2 to 3.6	-15			
	$I_{IL}(3)$	Port 2	Output disabled Pull-up resistor off $V_{IN}=V_{SS}3$ $V_{DD}3$= 1.6V to 3.6V (including output Tr. off leakage current)	2.2 to 3.6	-1			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 3, 6	I_{OH}=-0.6mA	2.6 to 3.6	V_{DD}-0.4			V
	$V_{OH}(2)$		I_{OH}=-0.4mA	2.2 to 3.6	V_{DD}-0.4			
	$V_{OH}(3)$	Port 2	I_{OH}=-0.6mA $V_{DD}3$= 2.6V to 3.6V	2.6 to 3.6	$V_{DD}3$-0.4			
	$V_{OH}(4)$		I_{OH}=-0.4mA $V_{DD}3$= 2.6V to 3.6V	3.0 to 5.5	$V_{DD}3$-0.4			
	$V_{OH}(5)$		I_{OH}=-0.2mA $V_{DD}3$= 1.6V to 3.6V	2.2 to 5.5	$V_{DD}3$-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 6 P30 to P31, P34 to P37	I_{OL}=3.0mA	2.6 to 3.6			0.4	
	$V_{OL}(2)$		I_{OL}=1.3mA	2.2 to 3.6			0.4	
	$V_{OL}(3)$	P32, P33	I_{OL}=3.0mA	2.2 to 3.6			0.4	
	$V_{OL}(4)$	P20 to P21, P24 to P25	I_{OL}=3.0mA $V_{DD}3$=1.6V to 3.6V	2.6 to 3.6			0.4	
	$V_{OL}(5)$		I_{OL}=1.3mA $V_{DD}3$=1.6V to 3.6V	2.2 to 3.6			0.4	
	$V_{OL}(6)$	P22, P23	I_{OL}=3.0mA $V_{DD}3$=1.6V to 3.6V	2.2 to 3.6			0.4	
	$V_{OL}(7)$		I_{OL}=3.0mA $V_{DD}3$=1.6V to 3.6V	2.6 to 3.6			0.32	
Pull-up resistor	Rpu(1)	Ports 0, 1, 3, 6	$V_{OH}=0.9V_{DD}$	2.2 to 3.6	18	55	150	kΩ
	Rpu(2)	Port 2	$V_{OH}=0.9V_{DD}$ $V_{DD}3$=2.2V to 3.6V	2.2 to 3.6	18	55	150	
	Rpu(3)		$V_{OH}=0.9V_{DD}$ $V_{DD}3$=1.6V to 2.2V	2.2 to 3.6	30	80	200	
Hysteresis voltage	VHYS(1)	RESB		2.2 to 3.6		$0.1V_{DD}$		V
	VHYS(2)	Port 2	$V_{DD}3$= 1.6V to 3.6V PnFSA=1 or other function is in input state	2.2 to 3.6		$0.1V_{DD}3$		
	VHYS(3)	Ports 0, 1, 3	PnFSA=1 or other function is in input state	2.2 to 3.6		$0.1V_{DD}$		
Pin capacitance	CP	All pins	Pins other than that under test $V_{IN}=V_{SS}$, f=1MHz, Ta=25°C	2.2 to 3.6		10		pF

Serial I/O Characteristics at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}A = 0V$

Serial I/O Characteristics (Wakeup Function Disabled) (Note 4-1-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK(1)	SCK0 (P12)	• See Fig. 6.	2.2 to 3.6	4			tCYC
		Low level pulse width	tSCKL(1)				2			
		High level pulse width	tSCKH(1)				2			
			tSCKHA(1)		• Automatic communication mode • See Fig. 6.		6			
			tSCKHBSY(1a)		• Automatic communication mode • See Fig. 6.		23			
			tSCKHBSY(1b)		• Mode other than automatic communication mode • See Fig. 6.		4			
	Output clock	Period	tSCK(2)	SCK0 (P12)	• CMOS output selected • See Fig. 6.	2.2 to 3.6	4			tCYC
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Automatic communication mode • CMOS output selected • See Fig. 6.		6			tCYC
			tSCKHBSY(2a)		• Automatic communication mode • CMOS output selected • See Fig. 6.		4		23	
			tSCKHBSY(2b)		• Mode other than automatic communication mode • See Fig. 6.		4			
Serial input	Data setup time		tsDI(1)	SI0 (P11), SB0 (P11)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.2 to 3.6	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0 (P10), SB0 (P11)	• (Note 4-1-2)	2.2 to 3.6			1tCYC +0.05	
	Output clock		tdDO(2)		• (Note 4-1-2)				1tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SIO0 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-2-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(3)	SCK0 (P12)	• See Fig. 6.	2.2 to 3.6	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
			tSCKHBSY(3)				2			
Serial input	Data setup time		tsDI(2)	SI0 (P11), SB0 (P11)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.2 to 3.6	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Input clock	Output delay time	tdD0(3)	SO0 (P10), SB0 (P11)	• (Note 4-2-2)	2.2 to 3.6			1tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-2-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig.6.

SIO1 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-3-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK(4)	SCK1 (P36)	• See Fig. 6.	2.2 to 3.6	4			tCYC
		Low level pulse width	tSCKL(4)				2			
		High level pulse width	tSCKH(4)				2			
			tSCKHA(4)		• Automatic communication mode • See Fig. 6.		6			
			tSCKHBSY(4a)		• Automatic communication mode • See Fig. 6.		23			
			tSCKHBSY(4b)		• Mode other than automatic communication mode • See Fig. 6.		4			
	Output clock	Period	tSCK(5)	SCK1 (P36)	• CMOS output selected • See Fig. 6.	2.2 to 3.6	4			tCYC
		Low level pulse width	tSCKL(5)				1/2			tSCK
		High level pulse width	tSCKH(5)				1/2			
			tSCKHA(5)		• Automatic communication mode • CMOS output selected • See Fig. 6.		6			tCYC
			tSCKHBSY(5a)		• Automatic communication mode • CMOS output selected • See Fig. 6.		4		23	
			tSCKHBSY(5b)		• Mode other than automatic communication mode • See Fig. 6.		4			
Serial input	Data setup time		tsDI(3)	SI1 (P35), SB1 (P25)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.2 to 3.6	0.03			µs
	Data hold time		thDI(3)				0.03			
Serial output	Input clock	Output delay time	tdD0(4)	SO1 (P34), SB1 (P35)	• (Note 4-3-2)	2.2 to 3.6			1tCYC +0.05	
	Output clock		tdDO(5)		• (Note 4-3-2)				1tCYC +0.05	

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SIO1 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-4-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(6)	SCK1 (P36)	• See Fig. 6.	2.2 to 3.6	2			tCYC
		Low level pulse width	tSCKL(6)				1			
		High level pulse width	tSCKH(6)				1			
			tSCKHBSY(6)				2			
Serial input	Data setup time		tsDI(4)	SI1 (P35), SB1 (P35)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.2 to 3.6	0.03			µs
	Data hold time		thDI(4)				0.03			
Serial output	Input clock	Output delay time	tdD0(6)	SO1 (P34), SB1 (P35)	• (Note 4-4-2)	2.2 to 3.6			1tCYC +0.05	

Note 4-4-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SMIIC0 Simple SIO Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(7)	SM0CK (P32)	See Fig. 6.	2.2 to 3.6	4			tCYC
		Low level pulse width	tSCKL(7)				2			
		High level pulse width	tSCKH(7)				2			
	Output clock	Period	tSCK(8)	SM0CK (P32)	• CMOS output selected • See Fig. 6.		4			
		Low level pulse width	tSCKL(8)				1/2			tSCK
		High level pulse width	tSCKH(8)				1/2			
Serial input	Data setup time		tsDI(5)	SM0DA (P33)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.2 to 3.6	0.03			µs
	Data hold time		thDI(5)				0.03			
Serial output	Output delay time		tdD0(7)	SM0DO (P34), SM0DA (P33)	• Specified with respect to falling edge of SIOCLK • Specified as interval up to time when output state starts changing. • See Fig. 6.	2.2 to 3.6			1tCYC +0.05	

Note 4-5-1: These specifications are theoretical values. Add margin depending on its use.

SMIIC0 I²C Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Clock	Input clock	Period	tSCL	SM0CK (P32)	• See Fig. 8.	2.2 to 3.6	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Period	tSCLx	SM0CK (P32)	• Specified as interval up to time when output state starts changing.	2.2 to 3.6	10			
		Low level pulse width	tSCLLx				1/2			tSCL
		High level pulse width	tSCLHx				1/2			
SM0CK and SM0DA pins input spike suppression time			tsp	SM0CK (P32) SM0DA (P33)	• See Fig. 8.	2.2 to 3.6			1	Tfilt
Bus release time between start and stop	Input		tBUF	SM0CK (P32) SM0DA (P33)	• See Fig. 8.	2.2 to 3.6	2.5			Tfilt
	Output		tBUFx	SM0CK (P32) SM0DA (P33)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			
Start/restart condition hold time	Input		tHD;STA	SM0CK (P32) SM0DA (P33)	• When SMIIC register control bit, SHDS=0 • See Fig. 8.	2.2 to 3.6	2.0			Tfilt
					• When SMIIC register control bit, SHDS=1 • See Fig. 8.		2.5			
	Output		tHD;STAx	SM0CK (P32) SM0DA (P33)	• Standard clock mode • Specified as interval up to time when output state starts changing.		4.1			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.0			
Restart condition setup time	Input		tSU;STA	SM0CK (P32) SM0DA (P33)	• See Fig. 8.	2.2 to 3.6	1.0			Tfilt
	Output		tSU;STAx	SM0CK (P32) SM0DA (P33)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			

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Parameter		Symbol	Applicable Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Stop condition setup time	Input	tSU;STO	SM0CK (P32) SM0DA (P33)	• See Fig. 8.	2.2 to 3.6	1.0			Tfilt
	Output	tSU;STOx	SM0CK (P32) SM0DA (P33)	• Standard clock mode • Specified as interval up to time when output state starts changing.		4.9			µs
				• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			
Data hold time	Input	tHD;DAT	SM0CK (P32) SM0DA (P33)	• See Fig. 8.	2.2 to 3.6	0			Tfilt
	Output	tHD;DATx	SM0CK (P32) SM0DA (P33)	• Specified as interval up to time when output state starts changing.		1		1.5	
Data setup time	Input	tSU;DAT	SM0CK (P32) SM0DA (P33)	• See Fig. 8.	2.2 to 3.6	1			Tfilt
	Output	tSU;DATx	SM0CK (P32) SM0DA (P33)	• Specified as interval up to time when output state starts changing.		1tSCL -1.5Tfilt			
SM0CK and SM0DA pins fall time	Input	tF	SM0CK (P32) SM0DA (P33)	• See Fig. 8.	2.2 to 3.6			300	ns
	Output	tF	SM0CK (P32) SM0DA (P33)	• When SMIIC register control bits, PSLW=1, PHV=1	2.8	20 +0.1Cb		250	
				• SM0CK, SM0DA port output FAST mode • Cb≤100pF	2.6 to 3.6			100	

Note 4-6-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-6-2: The value of Tfilt is determined by the values of the register SMIC0BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

250ns ≥ Tfilt >140ns

Note 4-6-3: Cb represents the total loads (in pF) connected to the bus pins. Cb ≤ 100pF

Note 4-6-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

250ns ≥ Tfilt >140ns

BRDQ (bit5) = 1

SCL frequency setting ≤ 100kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

250ns ≥ Tfilt >140ns

BRDQ (bit5) = 0

SCL frequency setting ≤ 400kHz

SLIIC0 Simple SIO Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(7)	SL0CK (P22)	See Fig. 8.	2.2 to 3.6	4			tCYC
		Low level pulse width	tSCKL(7)				2			
		High level pulse width	tSCKH(7)				2			
Serial input	Data setup time		tsDI(5)	SL0DA (P23)	• Specified with respect to rising edge of SIOCLK • See Fig. 8.	2.2 to 3.6	0.03			µs
	Data hold time		thDI(5)				0.03			
Serial output	Output delay time		tdD0(7)	SL0DO (P24), SL0DA (P23)	• Specified with respect to falling edge of SIOCLK • Specified as interval up to time when output state starts changing. • See Fig. 8.	2.2 to 3.6			1tCYC +0.05	

Note 4-7-1: These specifications are theoretical values. Add margin depending on its use.
Note 4-7-2: When not specified, $V_{DD}3$=1.6V to 3.6V ($V_{DD}3 \leq V_{DD}$)

SLIIC1 I²C Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Clock	Input clock	Period	tSCL	SL0CK (P22)	• See Fig. 8.	2.2 to 3.6	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
SL0CK and SL0DA pins input spike suppression time			tsp	SL0CK (P22) SL0DA (P23)	• See Fig. 8.	2.2 to 3.6			1	Tfilt
Bus release time between start and stop		Input	tBUF	SL0CK (P22) SL0DA (P23)	• See Fig. 8.	2.2 to 3.6	2.5			Tfilt
Start/restart condition hold time		Input	tHD;STA	SL0CK (P22) SL0DA (P23)	• When SLIIC register control bit, SHDS=0 • See Fig. 8.	2.2 to 3.6	2.0			Tfilt
					• When SLIIC register control bit SHDS=1 • See Fig. 8.		2.5			
Restart condition setup time		Input	tSU;STA	SL0CK (P22) SL0DA (P23)	• See Fig. 8.	2.2 to 3.6	1.0			Tfilt
Stop condition setup time		Input	tSU;STO	SL0CK (P22) SL0DA (P23)	• See Fig. 8.	2.2 to 3.6	1.0			Tfilt
Data hold time		Input	tHD;DAT	SL0CK (P22) SL0DA (P23)	• See Fig. 8.	2.2 to 3.6	0			Tfilt
		Output	tHD;DATx	SL0CK (P22) SL0DA (P23)	• Specified as interval up to time when output state starts changing.		1		1.5	
Data setup time		Input	tSU;DAT	SL0CK (P22) SL0DA (P23)	• See Fig. 8.	2.2 to 3.6	1			Tfilt
		Output	tSU;DATx	SL0CK (P22) SL0DA (P23)	• Specified as interval up to time when output state starts changing.		1tSCL -1.5Tfilt			

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Parameter		Symbol	Applicable Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
SM0CK and SM0DA pins fall time	Input	tF	SM0CK (P32) SM0DA (P33)	• See Fig. 8.	2.2 to 3.6			300	ns
	Output	tF	SM0CK (P32) SM0DA (P33)	• When SLIIC0 register control bits PSLW=1, PHV=1 When $V_{DD}3$=2.8V	2.8 to 3.6	20 +0.1Cb		250	
				• When SLIIC0 register control bits PSLW=1, PHV=1 When V_{DD}=1.8	2.2 to 3.6	20 +0.1Cb		250	
				• SL0CK, SL0DA port output FAST mode • Cb≤100pF	2.6 to 3.6			100	

Note 4-8-1: The value of Tfilt is determined by the values of the register SLIC0PCNT, bits 5 and 4 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

250ns ≥ Tfilt > 140ns

Note 4-8-2: Cb represents the total loads (in pF) connected to the bus pins. Cb ≤ 100pF

Note 4-8-3: When not specified, $V_{DD}3$=1.6V to 3.6V ($V_{DD}3 \leq V_{DD}$)

UART0 Operating Conditions at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}A = 0V$

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
			V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR0	U0RX (P13), U0TX (P14), U0BRG (P07)		2.2 to 3.6	4		8	tBGCYC

Note 4-9: tBGCYC denotes one cycle of the baudrate clock source.

UART2 Operating Conditions at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}A = 0V$

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
			V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR2	U2RX (P16), U2TX (P17)		2.2 to 3.6	8		4096	tBGCYC

Note 4-10: tBGCYC denotes one cycle of the baudrate clock source.

Pulse Input Conditions at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}A = 0V$

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0 (P30), INT1 (P31), INT2 (P14), INT3 (P15), INT4 (P20), INT5 (P21), INT6 (P24), INT7 (P25)	• Interrupt source flag can be set. • Event inputs for timers 2 and 3 are enabled.	2.2 to 3.6	2			tCYC
	tPIL(2)	RESB	Resetting is enabled.	2.2 to 3.6	10			µs

Note 4-11: When not specified, $V_{DD}3$=1.6V to 3.6V ($V_{DD}3 \leq V_{DD}$)

AD Converter Characteristics at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}A = 0V$

12-bit AD Conversion Mode

Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Resolution	NAD	AN0 (P00), AN1 (P01), AN2 (P60), AN3 (P61)		2.6 to 3.6		12		bit
Absolute accuracy	ETAD		(Note 6-1)	2.6 to 3.6			±16	LSB
Conversion time	TCAD12		Conversion time calculated	3.0 to 3.6	32		209	µs
				2.6 to 3.6	67		209	
Analog input voltage range	VAIN			2.6 to 3.6	$V_{SS}A$		$V_{DD}A$	V
Analog port input current	IAINH		VAIN=V_{DD}	2.6 to 3.6			1	µA
	IAINL		VAIN=V_{SS}	2.6 to 3.6	-1			

Conversion time calculation formula: TCAD12= ((52/(AD division ratio))+2) × tCYC

8-bit AD Conversion Mode

Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Resolution	NAD	AN0 (P00), AN1 (P01), AN2 (P60), AN3 (P61)		2.6 to 3.6		8		bit
Absolute accuracy	ETAD		(Note 6-1)	2.6 to 3.6			±1.5	LSB
Conversion time	TCAD8		Conversion time calculated	3.0 to 3.6	20		129	µs
				2.6 to 3.6	42		129	
Analog input voltage range	VAIN			2.6 to 3.6	$V_{SS}A$		$V_{DD}A$	V
Analog port input current	IAINH		VAIN=V_{DD}	2.6 to 3.6			1	µA
	IAINL		VAIN=V_{SS}	2.6 to 3.6	-1			

Conversion time calculation formula: TCAD8= ((32/(AD division ratio))+2) × tCYC

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy.
Note 6-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.

The conversion time is twice the normal value when one of the following conditions occurs:
- The first AD conversion is executed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

Consumption Current Characteristics at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}A=0V$

typ: 3.0V

Parameter	Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}A$ ≥$V_{DD}3$	• FmCF=10MHz ceramic oscillation mode • FmMRC=0MHz (oscillation stoped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 10MHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.6 to 3.6		3.89	7.2	mA
	IDDOP(2)		• FmCF=0Hz (oscillation stopped) • FmMRC=10MHz oscillator mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 10MHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.6 to 3.6		3.72	6.6	
	IDDOP(3)		• FmCF=0Hz (oscillation stopped) • FmMRC=4MHz oscillator mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 4MHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.2 to 3.6		2.28	3.2	
	IDDOP(4)		• FmCF=0Hz (oscillation stopped) • FmMRC=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to internal RC oscillation • 1/1 frequency division mode	2.2 to 3.6		0.62	1.8	
	IDDOP(5)		• FmCF=0Hz (oscillation stopped) • FmMRC=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 32.768kHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.2 to 3.6		24.4	65	µA

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}A$ ≥$V_{DD}3$	• HALT mode • FmCF=10MHz ceramic oscillation mode • FmMRC=0MHz (oscillation stoped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 10MHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.6 to 3.6		1.18	2.0	mA
	IDDHALT(2)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmMRC=10MHz oscillator mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 10MHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.6 to 3.6		1.05	1.8	
	IDDHALT(3)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmMRC=4MHz oscillator mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 4MHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.2 to 3.6		0.44	0.8	
	IDDHALT(4)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmMRC=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to internal RC oscillation • 1/1 frequency division mode	2.2 to 3.6		0.12	0.5	
	IDDHALT(5)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmMRC=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 32.768kHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.2 to 3.6		8.21	40	µA
HOLD mode consumption current	IDDHOLD(1)	$V_{DD}1$	HOLD mode • CF1=V_{DD} or open (external clock mode)	2.2 to 3.6		0.02	20	
HOLDX mode consumption current	IDDHOLD(2)		HOLDX mode • CF1=V_{DD} or open (external clock mode) • FmX'tal=32.768kHz crystal oscillator mode	2.2 to 3.6		5.2	35	

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

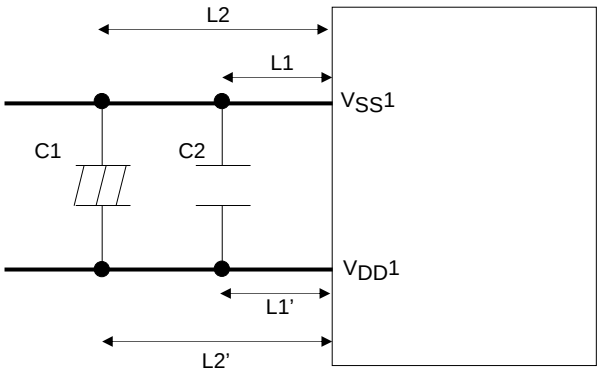
F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1$=$V_{SS}2$=$V_{SS}A$=0V

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Microcontroller erase current current is excluded.	2.6 to 3.6			7	mA
Onboard programming time	tFW(1)		• 128-/1K-byte erase operation	2.6 to 3.6			30	ms
	tFW(2)		• 2-byte programming operation	2.6 to 3.6			60	µs

Power Pin Treatment Conditions 1 ($V_{DD}1$, $V_{SS}1$)

Connect capacitors that meet the following conditions between the $V_{DD}1$ and $V_{SS}1$ pins:

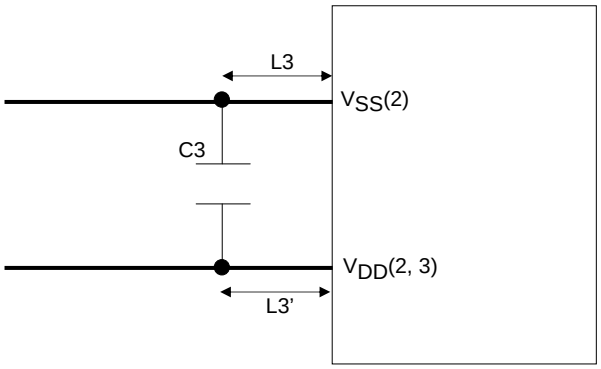
- Connect among the $V_{DD}1$ and $V_{SS}1$ pins and the capacitors C1 and C2 with the shortest possible lead wires, of the same length (L1=L1', L2=L2') wherever possible.
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel. The capacitance of C2 should be approximately 0.1μF or larger.
- The $V_{DD}1$ and $V_{SS}1$ traces must be thicker than the other traces.



Power Pin Treatment Conditions 2 ($V_{DD}(2, 3)$, $V_{SS}(2)$)

Connect capacitors that meet the following condition between the $V_{DD}(2)$ and $V_{SS}(2)$, $V_{DD}(3)$ and $V_{SS}(2)$ pins:

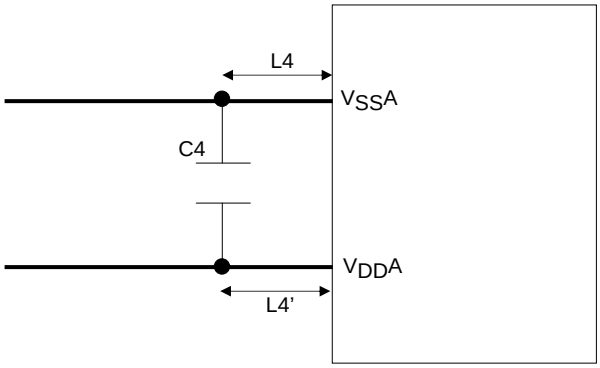
- Connect among the $V_{DD}(2, 3)$ and $V_{SS}(2)$ pins and the capacitor C3 with the shortest possible lead wires, of the same length (L3=L3') wherever possible.
- The capacitance of C3 should be approximately 0.1μF or larger.
- The $V_{DD}(2, 3)$ and $V_{SS}(2)$ traces must be thicker than the other traces.



Power Pin Treatment Conditions 3 ($V_{DD}A$, $V_{SS}A$)

Connect capacitors that meet the following condition between the $V_{DD}A$ and $V_{SS}A$ pins:

- Connect among the $V_{DD}A$ and $V_{SS}A$ pins and the capacitor C4 with the shortest possible lead wires, of the same length (L4=L4') wherever possible.
- The capacitance of C4 should be approximately 0.1μF or larger.
- The $V_{DD}A$ and $V_{SS}A$ traces must be thicker than the other traces.



Characteristics of a Sample OSC1 System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

Nominal Frequency	Vendor Name	Resonator	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [ms]	max [ms]	
10MHz	MURATA	CSTCE10M0G52-R0	(10)	(10)	OPEN	0	2.2 to 3.6	0.02	0.2	C1, C2 integrated type
8MHz		CSTCE8M00G52-R0	(10)	(10)	OPEN	0	2.2 to 3.6	0.02	0.2	C1, C2 integrated type
4MHz		CSTCR4M00G53-R0	(15)	(15)	OPEN	680	2.2 to 3.6	0.02	0.2	C1, C2 integrated type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the lower limit level of the operating voltage range (see Figure 4)

Characteristics of a Sample System Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	OPEN	0	2.2 to 3.6	0.9	2	Applicable CL value=12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 4).

Note: The traces to and from the components that are involved in oscillation should be kept as short as possible as the oscillation characteristics are affected by their trace pattern.

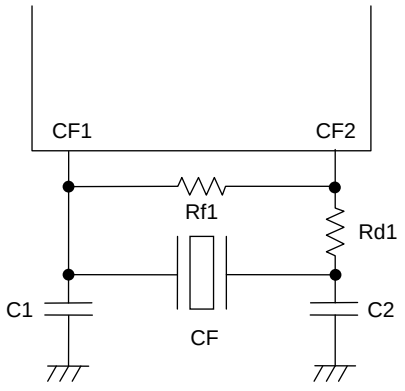


Figure 1 CF Oscillator Circuit

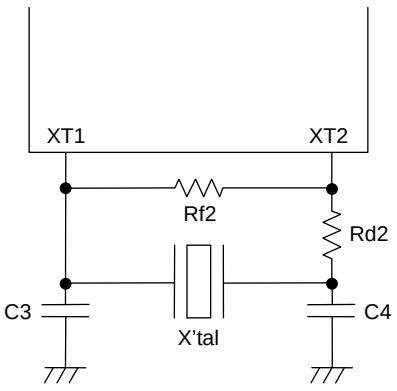


Figure 2 XT Oscillator Circuit

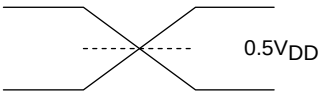
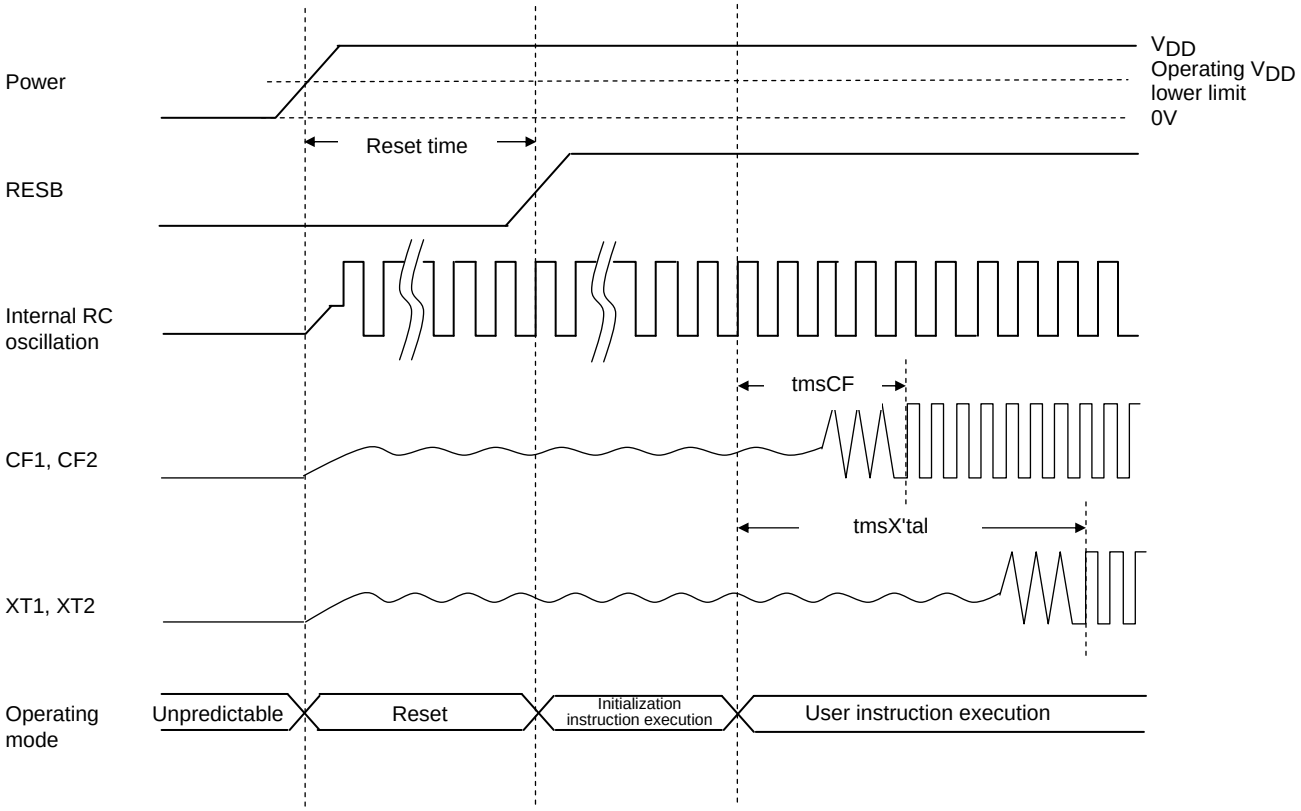
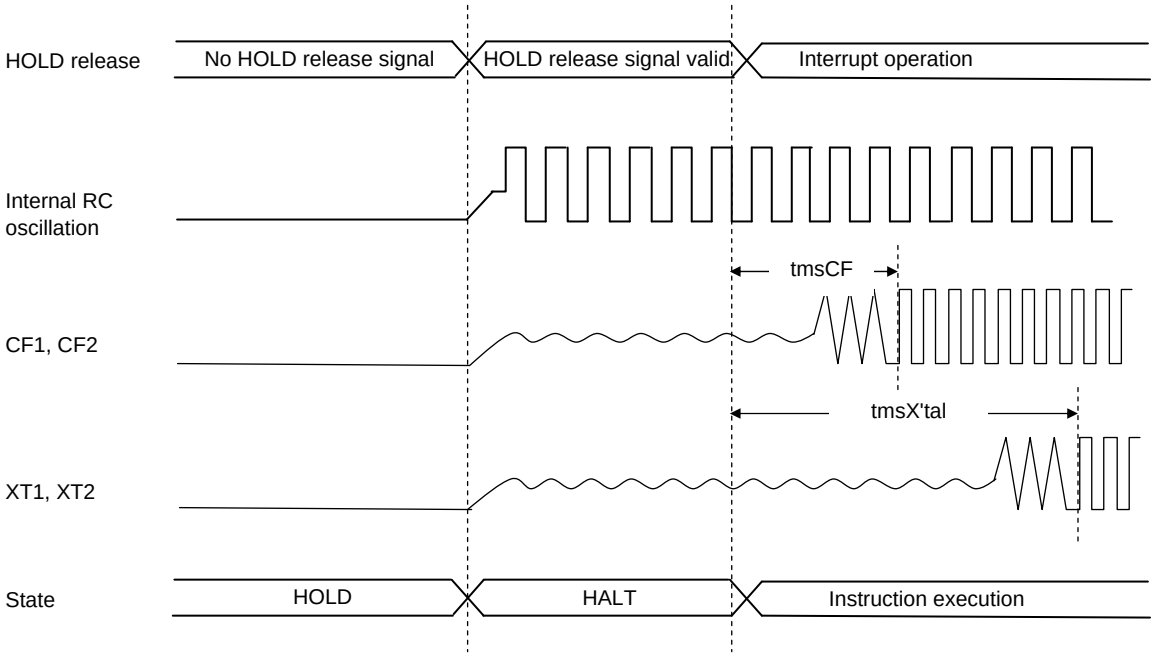


Figure 3 AC Timing Measurement Point

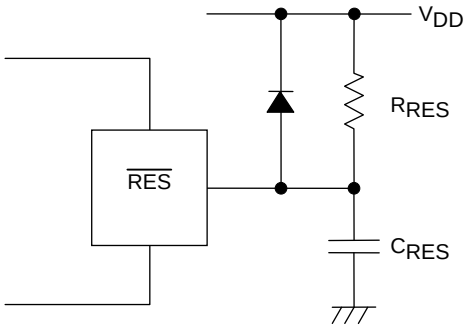


Reset Time and Oscillation Stabilization Time



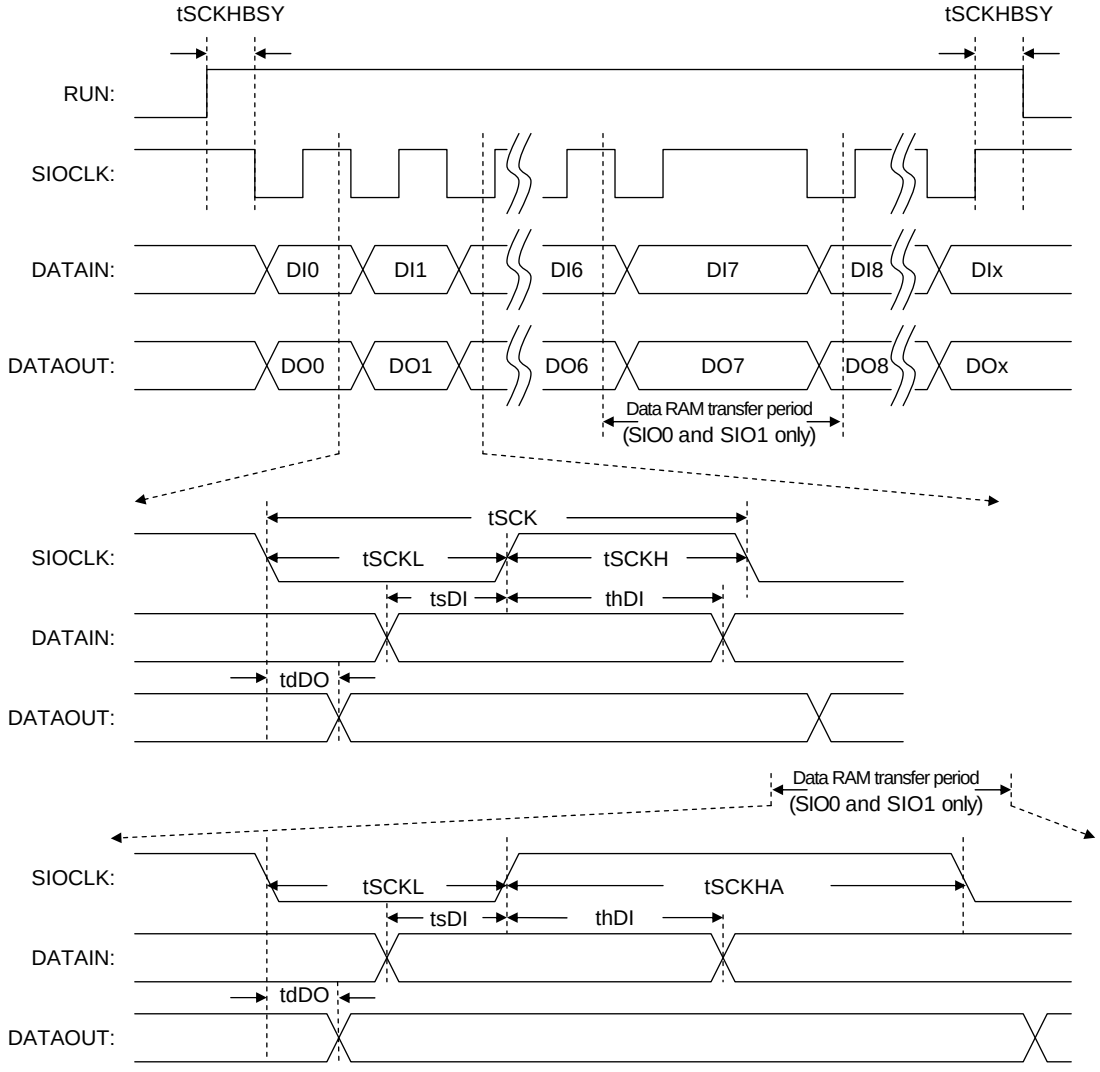
HOLD Release and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time Timing Charts



Note:
Reset signal must be present when power supply rises.
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for 10μs after the supply voltage gets stabilized.

Figure 5 Reset Circuit



* Remarks: DIx and DOx denote the last bits communicated; x = 0 to 32768

Figure 6 Serial I/O Waveforms

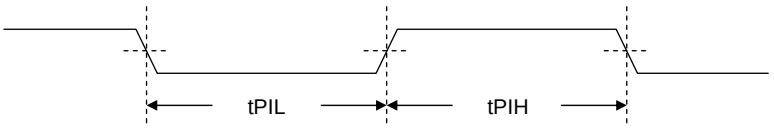
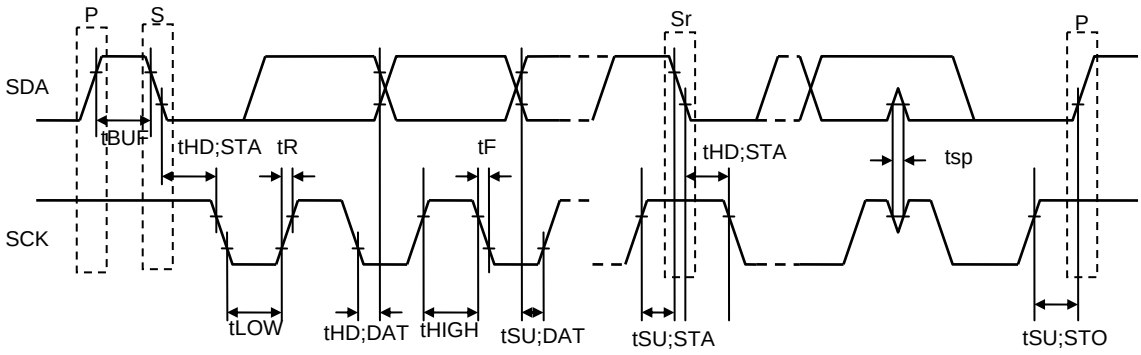


Figure 7 Pulse Input Timing Signal Waveform



S: Start condition
P: Stop condition
Sr: Restart condition

Figure 8 I^2C Timing

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