Integrated Device Technology, Inc.

# BiCMOS HIGH-SPEED STATIC RAM 72K (8K x 9-BIT)

**ADVANCE INFORMATION**
**IDT71B69**

## FEATURES:

- 8192-words x 9-bits organization
- Fast access time:
  - — Commercial: 12/15/20ns
  - — Military: 15/20ns
- Produced with advanced BiCEMOS™ high-performance technology
- JEDEC standard 28-pin DIP/SOJ and 32-pin LCC
- Single 5V power supply
- Inputs and outputs directly TTL compatible

## DESCRIPTION:

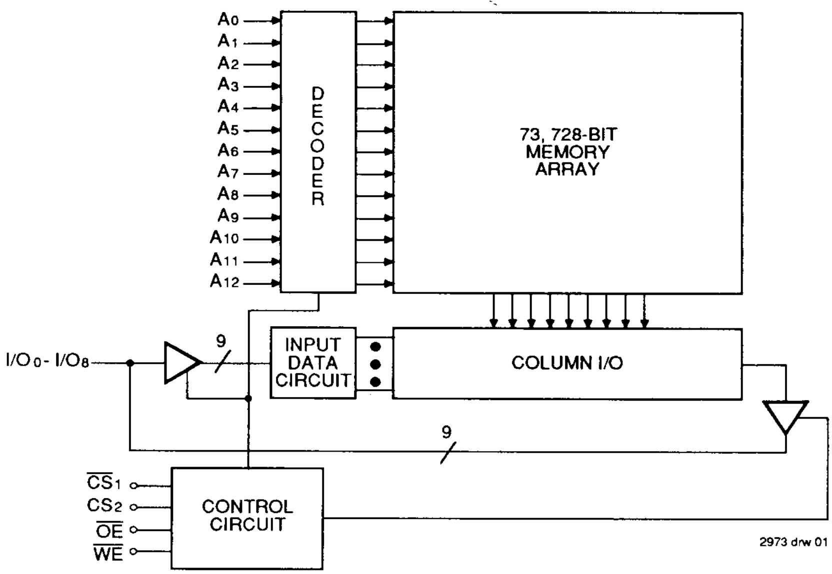
The IDT71B69 is a 73,728-bit high-speed static RAM, organized as 8K x 9. It is fabricated using IDT's high-performance, high-reliability BiCEMOS technology.

The IDT71B69 offers address access times as fast as 12ns. The ninth bit is optimal for systems using parity.

All inputs and outputs of the IDT71B69 are TTL-compatible. The device has 2 chip selects for simplified address decoding.

The IDT71B69 is packaged in an industry standard 300-mil 28-pin DIP/SOJ and 32-pin LCC.

## FUNCTIONAL BLOCK DIAGRAM

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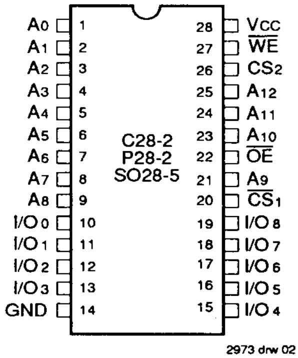
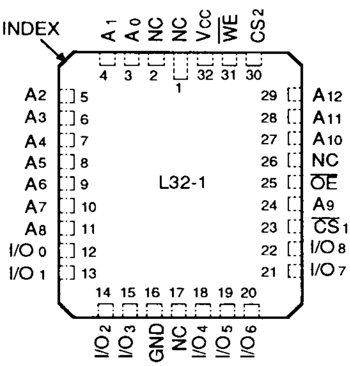
## PIN CONFIGURATIONS




DIP/SOJ
TOP VIEW




LCC
TOP VIEW

## TRUTH TABLE(1)

| CS2 | $\overline{CS}_1$ | $\overline{OE}$ | $\overline{WE}$ | I/O | Function |
|---|---|---|---|---|---|
| X | H | X | X | Hi-Z | Deselect chip |
| L | X | X | X | Hi-Z | Deselect chip |
| H | L | L | H | DOUT | Read |
| H | L | X | L | DIN | Write |
| H | L | H | H | Hi-Z | Output Disabled |

NOTE: 2973 tbl 01

1. H = VIH, L = VIL, X = Don't Care.

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Com'l. | Mil. | Unit |
|---|---|---|---|---|
| VTERM | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V |
| TA | Operating Temperature | 0 to +70 | -55 to +125 | °C |
| TBIAS | Temperature Under Bias | -55 to +125 | -65 to +135 | °C |
| TSTG | Storage Temperature | -55 to +125 | -65 to +135 | °C |
| IOUT | DC Output Current | 50 | 50 | mA |

NOTE: 2973 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade | Temperature | GND | Vcc |
|---|---|---|---|
| Military | -55°C to +125°C | 0V | 5V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5V ± 10% |

2973 tbl 02

## CAPACITANCE (TA = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| CIN | Input Capacitance | VIN = 0V | 8 | pF |
| COUT | Output Capacitance | VOUT = 0V | 8 | pF |

NOTE: 2973 tbl 03

1. This parameter is determined by device characterization, but is not production tested.

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Vcc | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| VIH | Input High Voltage | 2.2 | — | 6.0 | V |
| VIL | Input Low Voltage | -0.5(1) | — | 0.8 | V |

NOTE: 2973 tbl 05

1. 1.5V undershoots are allowed for 10ns once per cycle.

## DC ELECTRICAL CHARACTERISTICS[1]

($V_{CC}$ = 5.0V ± 10%)

| Symbol | Parameter | 71B69S12 | | 71B69S15 | | 71B69S20 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | |
| $I_{CC}$ | Dynamic Operating Current<br>$\overline{CS_1}$ = $V_{IL}$, $CS_2$ = $V_{IH}$, Outputs Open, $V_{CC}$ = Max., f = $f_{MAX}$[2] | 180 | — | 180 | — | 180 | 190 | mA |

2958 tbl 05

**NOTES:**
1. All values are maximum guaranteed values.
2. $f_{MAX}$ = 1/$t_{RC}$.

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Condition | IDT71B69S | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $\|I_{LI}\|$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = GND to $V_{CC}$ | — | 5 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CS_1}$ = $V_{IH}$, $CS_2$ = $V_{IL}$<br>$V_{OUT}$ = GND to $V_{CC}$ | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8mA, $V_{CC}$ = Min. | — | 0.4 | V |
| | | $I_{OL}$ = 10mA, $V_{CC}$ = Min. | — | 0.5 | |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4mA, $V_{CC}$ = Min. | 2.4 | — | V |

2973 tbl 08

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 3ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figures 1A, 1B & 1C |

2973 tbl 07

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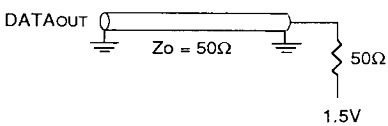
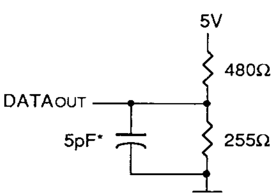



**Figure 1A. AC Test Load**




*Includes jig and scpe capacitance.

**Figure 1B.**

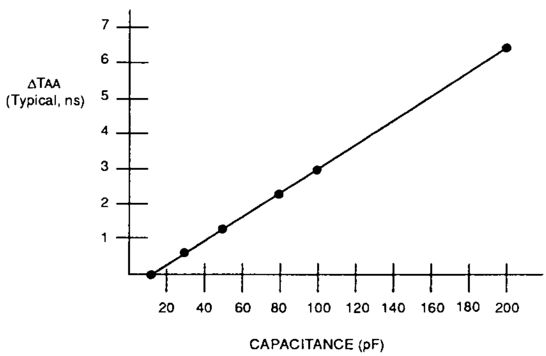


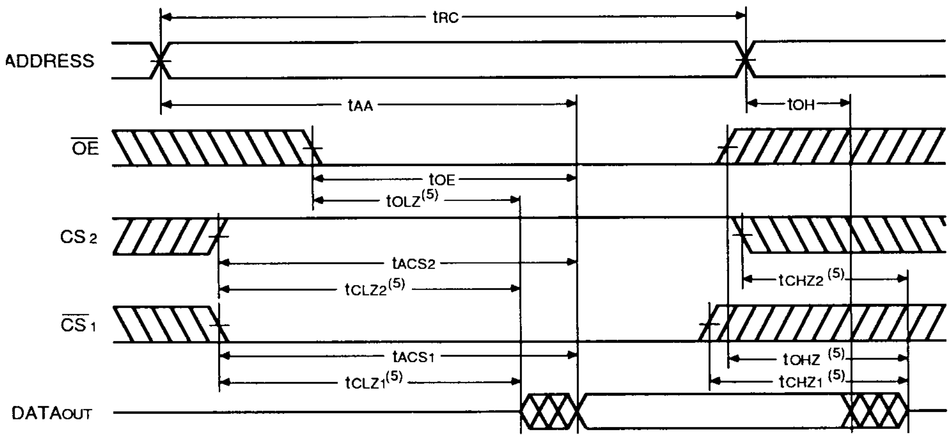

**Figure 1C. Lumped Capacitive Load, Typical Derating**

## AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

| Symbol | Parameter | 71B9S12[1] | | 71B69S15 | | 71B69S20 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Read Cycle** | | | | | | | | |
| tRC | Read Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| tAA | Address Access Time | — | 12 | — | 15 | — | 20 | ns |
| tACS1 | Chip Select-1 Access Time | — | 12 | — | 15 | — | 20 | ns |
| tACS2 | Chip Select-2 Access Time | — | 12 | — | 15 | — | 20 | ns |
| tCLZ1,2 | Chip Select to Output in Low Z[2] | 2 | — | 3 | — | 5 | — | ns |
| tOE | Output Enable to Output Valid | — | 6 | — | 7 | — | 9 | ns |
| tOLZ | Output Enable to Output in Low Z[2] | 2 | — | 3 | — | 3 | — | ns |
| tCHZ1,2 | Chip Select-1, 2 to Output in High Z[2] | — | 6 | — | 7 | — | 8 | ns |
| tOHZ | Output Disable to Output in High Z[2] | — | 5 | — | 6 | — | 8 | ns |
| tOH | Output Hold from Address Change | 3 | — | 3 | — | 5 | — | ns |
| **Write Cycle** | | | | | | | | |
| tWC | Write Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| tAW | Address Valid to End of Write | 10 | — | 12 | — | 15 | — | ns |
| tCW1 | Chip Select to End of Write ($\overline{CS}_1$) | 10 | — | 12 | — | 15 | — | ns |
| tCW2 | Chip Select to End of Write (CS2) | 10 | — | 12 | — | 15 | — | ns |
| tAS | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| tWP | Write Pulse Width | 9 | — | 12 | — | 15 | — | ns |
| tWR1 | Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$) | 0 | — | 0 | — | 0 | — | ns |
| tWR2 | Write Recovery Time (CS2) | — | 0 | — | 3 | — | 5 | ns |
| tWHZ | Write Enable to Output in High Z[2] | — | 6 | — | 7 | — | 8 | ns |
| tDW | Data Valid to End of Write | 6 | — | 9 | — | 10 | — | ns |
| tDH1 | Data Hold from Write Time ($\overline{CS}_1$, $\overline{WE}$) | 0 | — | 0 | — | 0 | — | ns |
| tDH2 | Data Hold from Write Time (CS2) | 0 | — | 0 | — | 0 | — | ns |
| tOW | Output Active from End of Write[2] | 2 | — | 3 | — | 5 | — | ns |

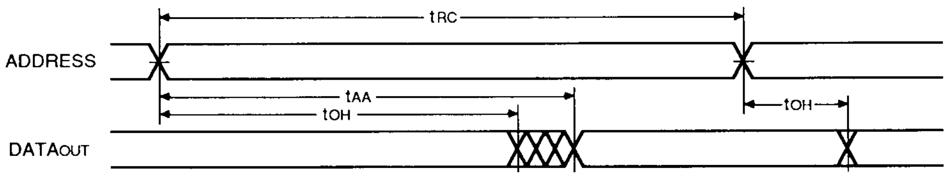
NOTES:
2973 tbl 09
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.

## TIMING WAVEFORM OF READ CYCLE NO. 1(1,3)



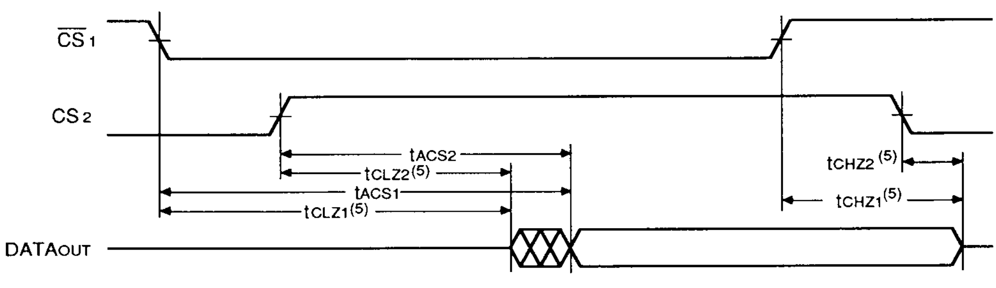

2973 drw 05

## TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)




2973 drw 06

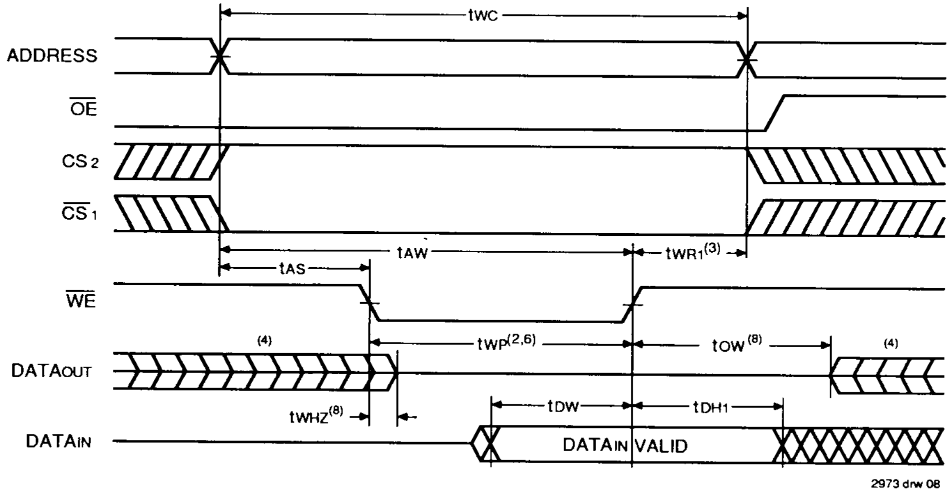
## TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



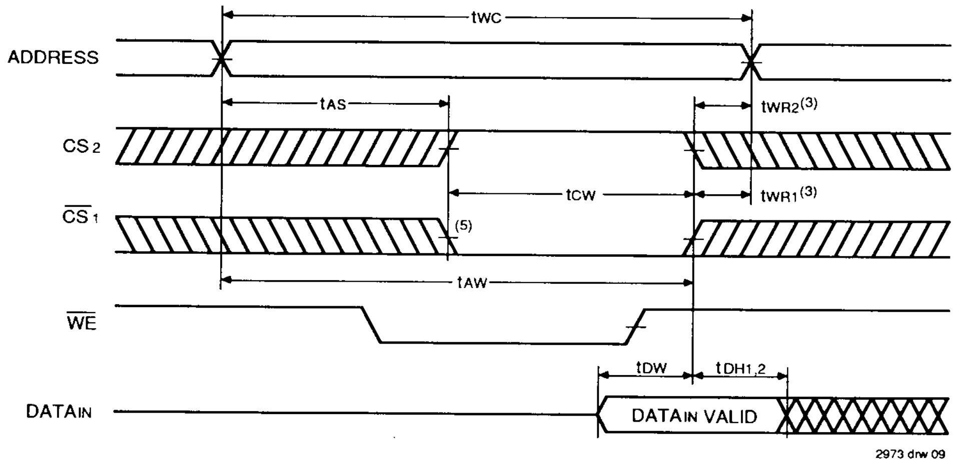

2973 drw 07

**NOTES:**
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and $CS_2$ transition high.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state.

## TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1)




## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1)




**NOTES:**

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap ($t_{WP}$) of a low $\overline{CS}_1$ and a high $CS_2$.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or $CS_2$ going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}_1$ low transition or $CS_2$ high transiton occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of $t_{WP}$ or ($t_{WHZ}$ +$t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified $t_{WR}$.
7. DATAOUT is the same phase of write data of this write cycle.
8. Transition is measured ±200mV from steady state.

## ORDERING INFORMATION

IDT XXXXX X XX X X

| Field | Code | Description |
|---|---|---|
| Process/Temperature Range | Blank | Commercial (0°C to +70°C) |
| Package | TP | Plastic DIP (300mil) |
| | TD | Ceramic DIP (300 mil) |
| | Y | Small Outline IC (J-Bend) |
| | L32 | 32-pin LCC |
| Speed (Speed in Nanoseconds) | 12 | Commercial Only |
| | 15 | Commercial Only |
| | 20 | Com'l. & Mil. |
| Power | S | Standard Power |
| Device Type | 71B69 | 72K (8K x 9-Bit) BiCMOS Static RAM |

2973 drw 10