Military Standard Products
UT69RH051 MicroController
Product Brief

**UNITED
TECHNOLOGIES
MICROELECTRONICS
CENTER**

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FEATURES

☐ Three 16-bit timer/counters
- High speed output
- Compare/capture
- Pulse width modulator
- Watchdog timer capabilities

☐ 256 bytes of on-chip data RAM

☐ 32 programmable I/O lines

☐ 7 interrupt sources

☐ Programmable serial channel with:
- Framing error detection
- Automatic address recognition

☐ TTL and CMOS compatible logic levels

☐ 64K external data and program memory space

☐ MCS®-51 fully compatible instruction set

☐ Flexible clock operation
- 1Hz to 20MHz with external clock
- 2MHz to 20MHz using internal oscillator with external crystal

☐ Radiation-hardened process and design; total dose irradiation testing MIL-STD-883 Method 1019
- Total dose: 1.0E6 rads(Si)
- Single event upset: <25.6E-6 errors/device-day
- Latchup immune

☐ Post-radiation AC/DC performance characteristics guaranteed to MIL-STD-883 Method 1019 testing at 1.0E6 rads (Si)

☐ Built on low-power, 1.2μ CMOS process

☐ Packaging options:
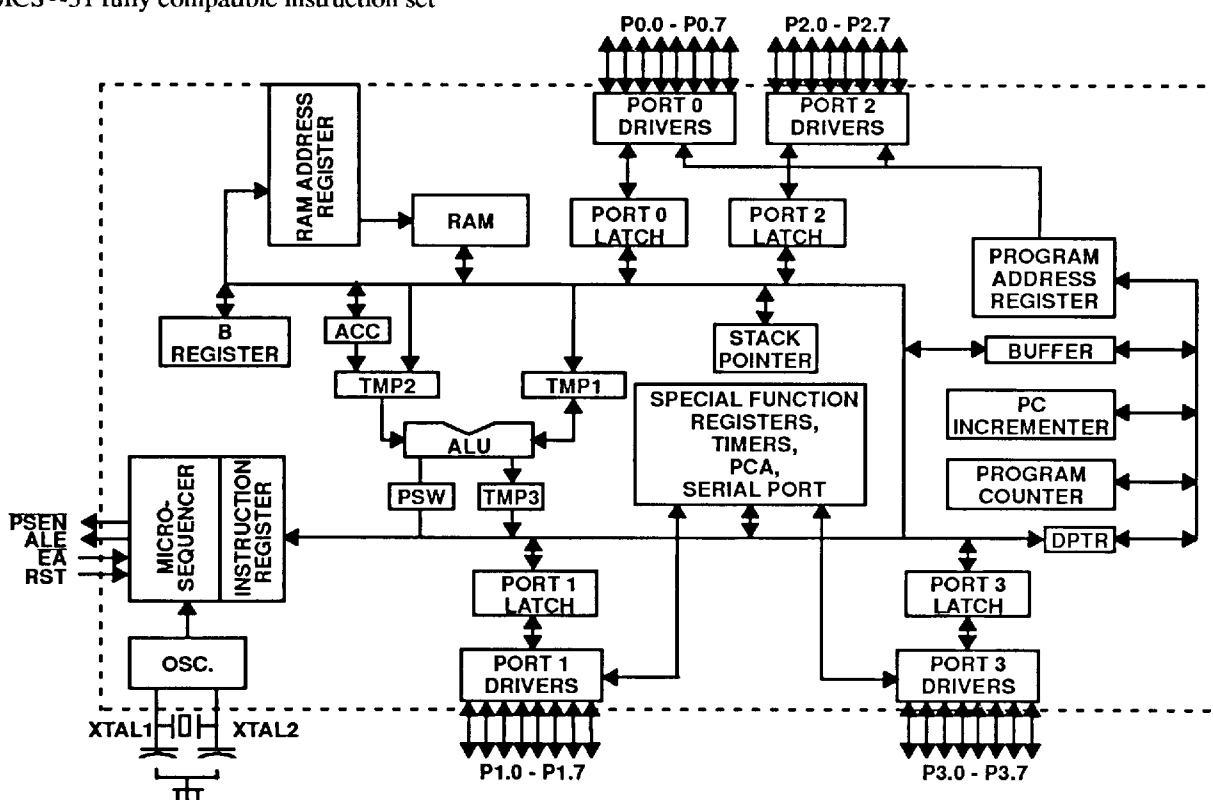- 40-pin DIP
- 44-lead flatpack

Figure 1. UT69RH051 MicroController Block Diagram

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1.0 INTRODUCTION

The UT69RH051 is a radiation-tolerant 8-bit microcontroller that is pin equivalent to the Intel 8XC51FC microcontroller. The UT69RH051's static design allows operation from 1Hz to 20MHz. This product brief will describe hardware and software interfaces to the UT69RH051.

2.0 SIGNAL DESCRIPTION

V_{DD}: +5V Supply voltage

V_{SS}: Circuit Ground

Port 0 (P0.0 - P0.7): Port 0 is an 8-bit port. Its pins are used as the low-order multiplexed address and data bus during accesses to external program and data memory. Port 0 pins use strong internal pullups when emitting 1's, and are TTL compatible.

Port 1 (P1.0 - P1.7): Port 1 is an 8-bit bidirectional I/O port with internal pullups. The output buffers can drive TTL loads. When the Port 1 pins have 1's written to them, they are pulled high by the internal pullups and can be used as inputs in this state. As inputs, any pins that are externally pulled low will source current because of the pullups. In addition, Port 1 pins have the alternate uses shown in table 1.

Port 2 (P2.0 - P2.7): Port 2 is an 8-bit port. Its pins are used as the high-order address bus during accesses to external Program Memory and during accesses to external Data Memory that uses 16-bit addresses (i.e., MOVX@DPTR). It uses strong internal pullups when emitting 1's in this mode. During operations that do not require a 16-bit address, Port 2 emits the contents of the P2 Special Function Registers (SFR). The pins have internal pullups and can drive TTL loads.

Port 3 (p3.0 - p3.7): Port3 is an 8-bit bidirectional I/O port with internal pullups. The output buffers can drive TTL loads. When the Port 3 pins have 1's written to them, they are pulled high by the internal pullups and can be used as inputs in this state. As inputs, any pins that are externally pulled low will source current because of the pullups. In addition, Port 3 pins have the alternate uses shown in table 2.

Table 1. Port 1 Alternate Functions

Port Pin	Alternate Name	Alternate Function
P1.0	T2	External clock input to Timer/ Counter 2
P1.1	T2EX	Timer/Counter 2 Capture/Reload trigger and direction control
P1.2	ECI	External count input to PCA
P1.3	CEX0	External I/O for PCA capture/ compare Module 0
P1.4	CEX1	External I/O for PCA capture/ compare Module 1
P1.5	CEX2	External I/O for PCA capture/ compare Module 2
P1.6	CEX3	External I/O for PCA capture/ compare Module 3
P1.7	CEX4	External I/O for PCA capture/ compare Module 4

Table 2. Port 3 Alternate Functions

Port Pin	Alternate Name	Alternate Function
P3.0	RXD	Serial port input
P3.1	TXD	Serial port output
P3.2	$\overline{INT0}$	External interrupt 0
P3.3	$\overline{INT1}$	External interrupt 1
P3.4	T0	External clock input for Timer 0
P3.5	T1	External clock input for Timer 1
P3.6	$\overline{WR}$	External Data Memory write strobe
P3.7	$\overline{RD}$	External Data Memory read strobe

RST: Reset Input. A high on this input for one oscillator period while the oscillator is running resets the device. All ports and SFRs reset to their default conditions. Internal data memory is undefined after reset. Program execution begins within 12 oscillator periods (one machine cycle) after the RST signal is brought low. RST contains an internal pulldown resistor to allow implementing power-up reset with only an external capacitor.

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ALE: Address Latch Enable. The ALE output is a pulse for latching the low byte of the address during accesses to external memory. In normal operation the ALE pulse is output every sixth oscillator cycle and may be used for external timing or clocking. However, during each access to external Data Memory (MOVX instruction), one ALE pulse is skipped.

$\overline{PSEN}$: Program Store Enable. This active low signal is the read strobe to the external program memory. $\overline{PSEN}$ is activated every sixth oscillator cycle except that two $\overline{PSEN}$ activations are skipped during external data memory accesses.

$\overline{EA}$: External Access Enable. This pin should be strapped to V_{SS} (Ground) for the UT69RH051.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

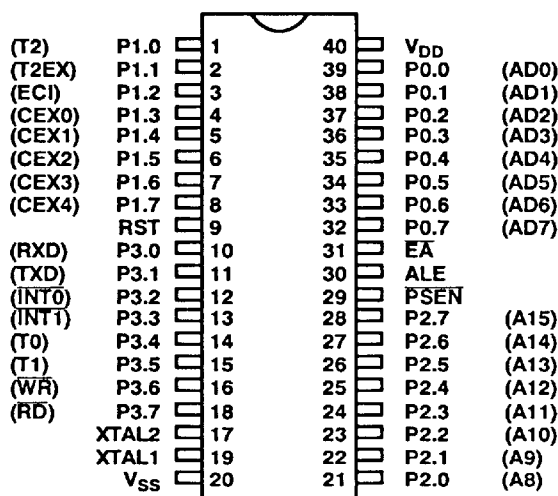|					
(T2)	P1.0	1	40	V_{DD}	
(T2EX)	P1.1	2	39	P0.0	(AD0)
(ECI)	P1.2	3	38	P0.1	(AD1)
(CEX0)	P1.3	4	37	P0.2	(AD2)
(CEX1)	P1.4	5	36	P0.3	(AD3)
(CEX2)	P1.5	6	35	P0.4	(AD4)
(CEX3)	P1.6	7	34	P0.5	(AD5)
(CEX4)	P1.7	8	33	P0.6	(AD6)
	RST	9	32	P0.7	(AD7)
(RXD)	P3.0	10	31	$\overline{EA}$	
(TXD)	P3.1	11	30	ALE	
($\overline{INT0}$)	P3.2	12	29	$\overline{PSEN}$	
($\overline{INT1}$)	P3.3	13	28	P2.7	(A15)
(T0)	P3.4	14	27	P2.6	(A14)
(T1)	P3.5	15	26	P2.5	(A13)
($\overline{WR}$)	P3.6	16	25	P2.4	(A12)
($\overline{RD}$)	P3.7	18	24	P2.3	(A11)
	XTAL2	17	23	P2.2	(A10)
	XTAL1	19	22	P2.1	(A9)
	V_{SS}	20	21	P2.0	(A8)

Figure 2. UT69RH051 Pin Connections

2.1 Hardware/Software Interface

2.1.1 Memory
The UT69RH051 has a separate address space for Program and Data Memory. Internally the UT69RH051 contains 256 bytes of Data Memory. It can address up to 64Kbytes of external Data Memory and 64Kbytes of external Program Memory.

2.1.1.1 Program Memory
There is no internal program memory in the UT69RH051. All program memory is accessed as external through ports P0 and P2. The $\overline{EA}$ pin must be tied to V_{SS} (ground) to enable access to external locations 0000_H through $7FFF_H$.

2.1.1.2 Data Memory
The UT69RH051 implements 256 bytes of internal data RAM. The upper 128 bytes of this RAM occupy a parallel address space to the SFRs. The CPU determines if the internal access to an address above 7FH is to the upper 128 bytes of RAM or to the SFR space by the addressing mode of the instruction. If direct addressing is used, the access is to the SFR space. If indirect addressing is used, the access is to the internal RAM. Stack operations are indirectly addressed so the upper portion of RAM can be used as stack space. Figure 3 shows the organization of the internal Data Memory.

The first 32 bytes are reserved for four register banks of eight bytes each. The processor uses one of the four banks as its working registers depending on the RS1 and RS0 bits in the PSW SFR. At reset, bank 0 is selected. If four register banks are not required, use the unused banks as general purpose scratch pad memory. The next 16 bytes (128 bits) are individually bit addressable. The remaining bytes are byte addressable and can be used as general purpose scratch pad memory. For addresses 0 - $7F_H$, use either direct or indirect addressing. For addresses larger than $7F_H$, use only indirect addressing.

In addition to the internal Data Memory, the processor can access 64 Kbytes of external Data Memory. The MOVX instruction accesses external Data Memory.

2.1.2 Special Function Registers
Table 3 contains the SFR memory map. Unoccupied addresses are not implemented on the device. Read accesses to these addresses will return unknown values and write accesses will have no effect.
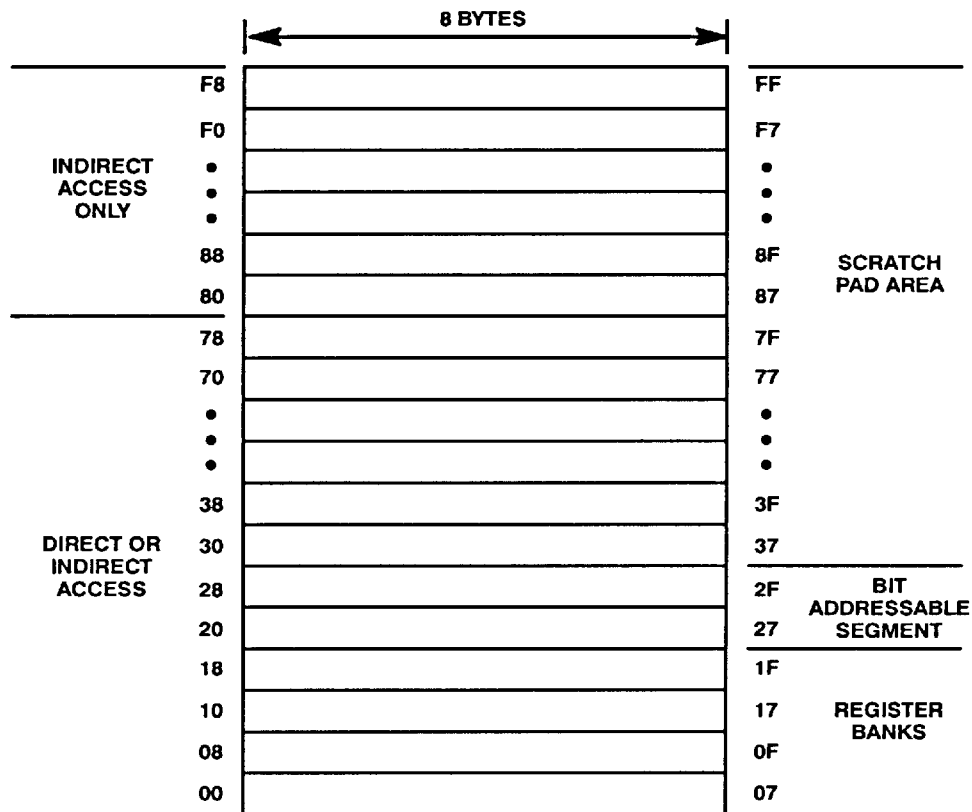
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Figure 3. Internal Data Memory Organization

2.1.3 Reset

The reset input is the RST pin. To reset, hold a the RST pin high for a minimum of 24 oscillator period while the oscillator is running. The CPU generates an internal reset from the external signal. The ports pins are driven to the reset state as soon as a valid high is detected on the RST pin.

While RST is high, $\overline{PSEN}$, ALE, and the port pins are pulled weakly high. All SFRs are reset to their reset values as shown in table 3. The internal Data Memory content is indeterminate.

The processor will begin operation one machine cycle after the RST line is brought low. A memory access occurs immediately after the RST line is brought low, but the data is not brought into the processor. The memory access repeats on the next machine cycle and actual processing begins at that time.

2.1.4 Instruction Set

The instruction set for the UT69RH051 is compatible to the Intel MCS-51 instruction set used on the 8XC51FC.

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Table 3. SFR Memory Registers

Addr									Addr
F8		CH 00000000	CCAP0H XXXXXXXX	CCAP1H XXXXXXXX	CCAP2H XXXXXXXX	CCAP3H XXXXXXXX	CCAP4H XXXXXXXX		FF
F0	B 00000000								F7
E8		CL 00000000	CCAP0L XXXXXXXX	CCAP1L XXXXXXXX	CCAP2L XXXXXXXX	CCAP3L XXXXXXXX	CCAP4L XXXXXXXX		EF
E0	ACC 00000000								E7
D8	CCON 00X00000	CMOD OOXXX000	CCAPM0 X00000000	CCAPM1 X00000000	CCAPM2 X00000000	CCAPM3 X00000000	CCAPM4 X00000000		DF
D0	PSW 00000000								D7
C8	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0									C7
B8	IP X0000000	SADEN 00000000							BF
B0	P3 11111111							IPH X00000000	B7
A8	IE 00000000	SADDR 00000000							AF
A0	P2 11111111								A7
98	SCON 00000000	SBUF XXXXXXXX							9F
90	P1 11111111								97
88	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8F
80	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 00XX00XX	87

Notes:
1. Values shown are the reset values of the registers.
2. X = undefined.

3.0 RADIATION HARDNESS

The UT69RH051 incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

RADIATION HARDNESS DESIGN SPECIFICATIONS [1]

PARAMETER	CONDITION	MINIMUM	UNIT
Total Dose	+25°C per MIL-STD-883 Method 1019	1.0E6	rads(Si)
Dose Rate Upset	$\leq 4\mu s$ pulsewidth	1.0E8	rads(Si)/sec
Dose Rate Survival	20ns pulsewidth	1.0E10	rads(Si)/sec
LET Threshold	-55°C to +125°C	36	MeV-cm^2/mg
Neutron Fluence	1MeV equivalent	1.0E14	n/cm^2

Note:
1. The UT69RH051 will not latchup during radiation exposure under recommended operating conditions.

4.0 ABSOLUTE MAXIMUM RATINGS [1]
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNITS
V_{DD}	DC Supply Voltage	-0.5 to 7.0	V
$V_{I/O}$	Voltage on Any Pin	-0.5 to V_{DD}+3V	V
T_{STG}	Storage Temperature	-65 to +150	°C
P_D	Maximum Power Dissipation	750	mW
T_J	Maximum Junction Temperature	175	°C
Θ_{JC}	Thermal Resistance, Junction-to-Case [2]	10	°C/W
I_I	DC Input Current	± 10	mA

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012.

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6.0 DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*
$V_{DD} = 5.0V \pm 10\%$; TA = -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level Input Voltage		-0.5	.8	V
V_{IH}	High-level Input Voltage (except XTAL2, RST, $\overline{EA}$)		2.0	V_{DD}+0.3	V
V_{IH1}	High-level Input Voltage (XTAL, RST)		3.85	V_{DD}+0.3	V
V_{OL}	Low-level Output Voltage[1] (Ports 1, 2 and 3)	I_{OL} = 100µA		0.3	V
		I_{OL} = 1.6mA		0.45	V
		I_{OL} = 3.5mA		1.0	V
V_{OL1}	Low-level Output Voltage[1] (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)	I_{OL} = 200µA		0.3	V
		I_{OL} = 3.2mA		0.45	V
		I_{OL} = 7.0mA		1.0	V
V_{OH}	High-level Output Voltage (Ports 1, 2, and 3 ALE/$\overline{PROG}$ and $\overline{PSEN}$)	I_{OH} = -10µA	4.2		V
		I_{OH} = -30µA	3.8		V
		I_{OH} = -60µA	3.0		V
V_{OH1}	High-level Output Voltage (Port 0 in External Bus Mode)	I_{OH} = -200µA	4.2		V
		I_{OH} = -3.2mA	3.8		V
		I_{OH} = -7.0mA	3.0		V
I_{IL}	Logical 0 Input Current (Ports 1, 2, and 3)	V_{IN} = 0.45V		-50	µA
I_{LI}	Input Leakage Current (Port 0)	V_{IN} = V_{IL} or V_{IH}		±10	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, and 3)	V_{IN} = 2V		-650	µA
C_{IO}	Pin Capacitance	@ 1MHZ, 25°C		10	pF
I_{CC}	Power Supply Current: (Running at 16MHz)	Note 2		52	mA

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883.
1. Under steady state (non-transient) conditions, I_{OL} must be limited externally as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port-
                         Port 0:   26mA
                  Ports 1, 2, & 3:   15mA
   Maximum total I_{OL} for all output pins: 71mA

   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
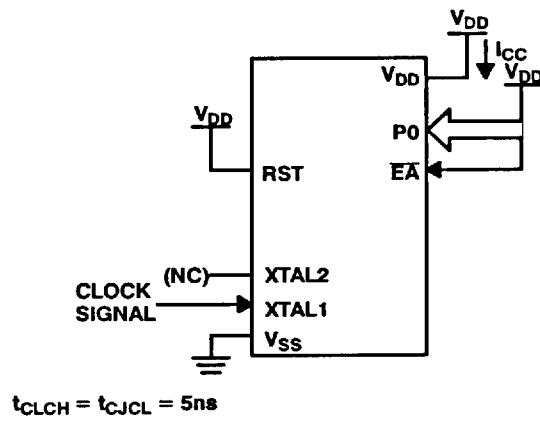2. See figures 4, 5, and 6 for test conditions.

$t_{CLCH} = t_{CJCL} = 5ns$

Figure 4. I_{DD} Test Condition, Active Mode
All other pins disconnected
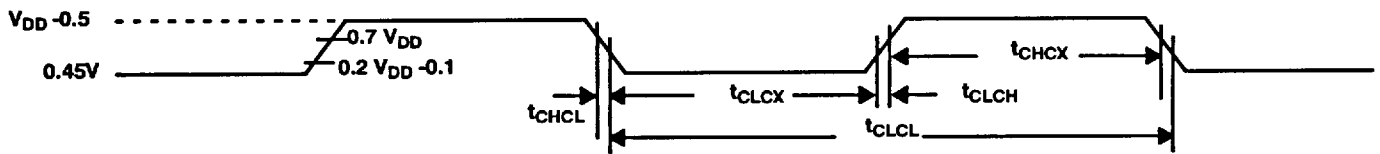
Figure 5. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
$t_{CLCH} = t_{CHCL} = 5ns$

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7.0 AC CHARACTERISTICS READ CYCLE (Post-Radiation)*
($V_{DD} = 5.0V \pm 10\%$; $-55°C < T_C < +125°C$)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{CLCL}	Clock Period	50		ns
$1/t_{CLCL}$	Oscillator Frequency		16	MHz
t_{LHLL}	ALE Pulse Width	$2\,t_{CLCL}-40$		ns
t_{AVLL}	Address Valid to ALE Low	$t_{CLCL}-40$		ns
t_{LLAX}	Address Hold after ALE Low	$t_{CLCL}-30$		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4\,t_{CLCL}-100$	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	$t_{CLCL}-30$		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3\,t_{CLCL}-45$		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3\,t_{CLCL}-105$	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		$t_{CLCL}-25$	ns
t_{AVIV}	Address to Valid Instruction In		$5\,t_{CLCL}-105$	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6\,t_{CLCL}-100$		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6\,t_{CLCL}-100$		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5\,t_{CLCL}-165$	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		$2\,t_{CLCL}-60$	ns
t_{LLDV}	ALE Low Valid Data In		$8\,t_{CLCL}-150$	ns
t_{AVDV}	Address to Valid Data In		$9\,t_{CLCL}-165$	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3\,t_{CLCL}-50$	$3\,t_{CLCL}+50$	ns
t_{AVWL}	Address Valid to $\overline{WR}$ Low	$4\,t_{CLCL}-130$		ns
t_{QVWX}	Data Valid Before $\overline{WR}$	$t_{CLCL}-50$		ns
t_{WHQX}	Data Hold After $\overline{WR}$	$t_{CLCL}-50$		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$7\,t_{CLCL}-150$		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	$t_{CLCL}-40$	$t_{CLCL}+40$	ns

Note:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

Figure 6. External Program Memory Read Timing Waveforms

Figure 7. External Data Memory Read Cycle Waveforms

Figure 8. External Data Memory Write Cycle Waveforms

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8.0 SERIAL PORT TIMING CHARACTERISTICS
($V_{DD} = 5.0V \pm 10\%$; $-55°C < T_C < +125°C$)

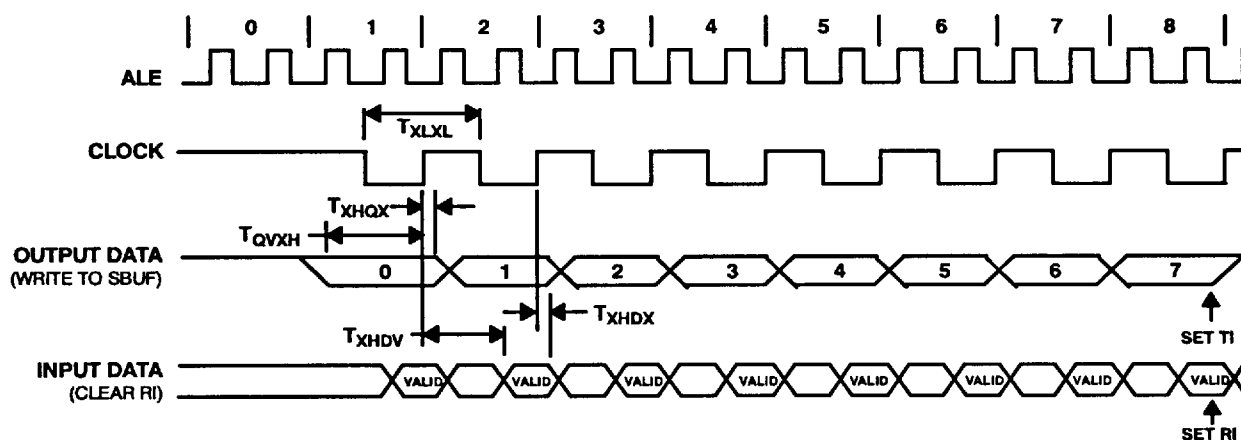| SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{XLXL}	Serial Port Clock Period	$12\ t_{CLCL}\text{-}10$	$12\ t_{CLCL}\text{+}10$	ns
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10\ t_{CLCL}\text{-}133$		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	$2\ t_{CLCL}\text{-}70$		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		$10\ t_{CLCL}\text{-}133$	ns

Figure 9. Serial Port Timing Waveforms

9.0 EXTERNAL CLOCK DRIVE TIMING CHARACTERISTICS

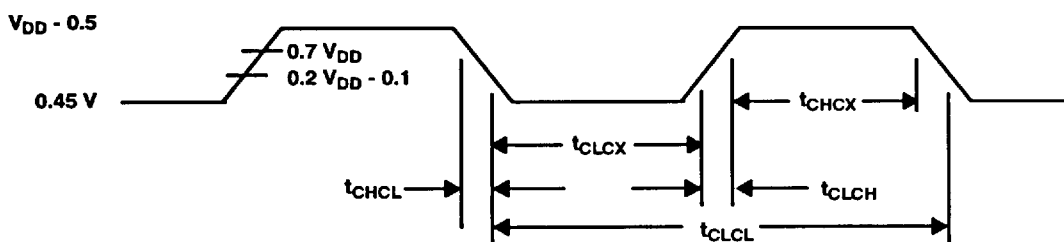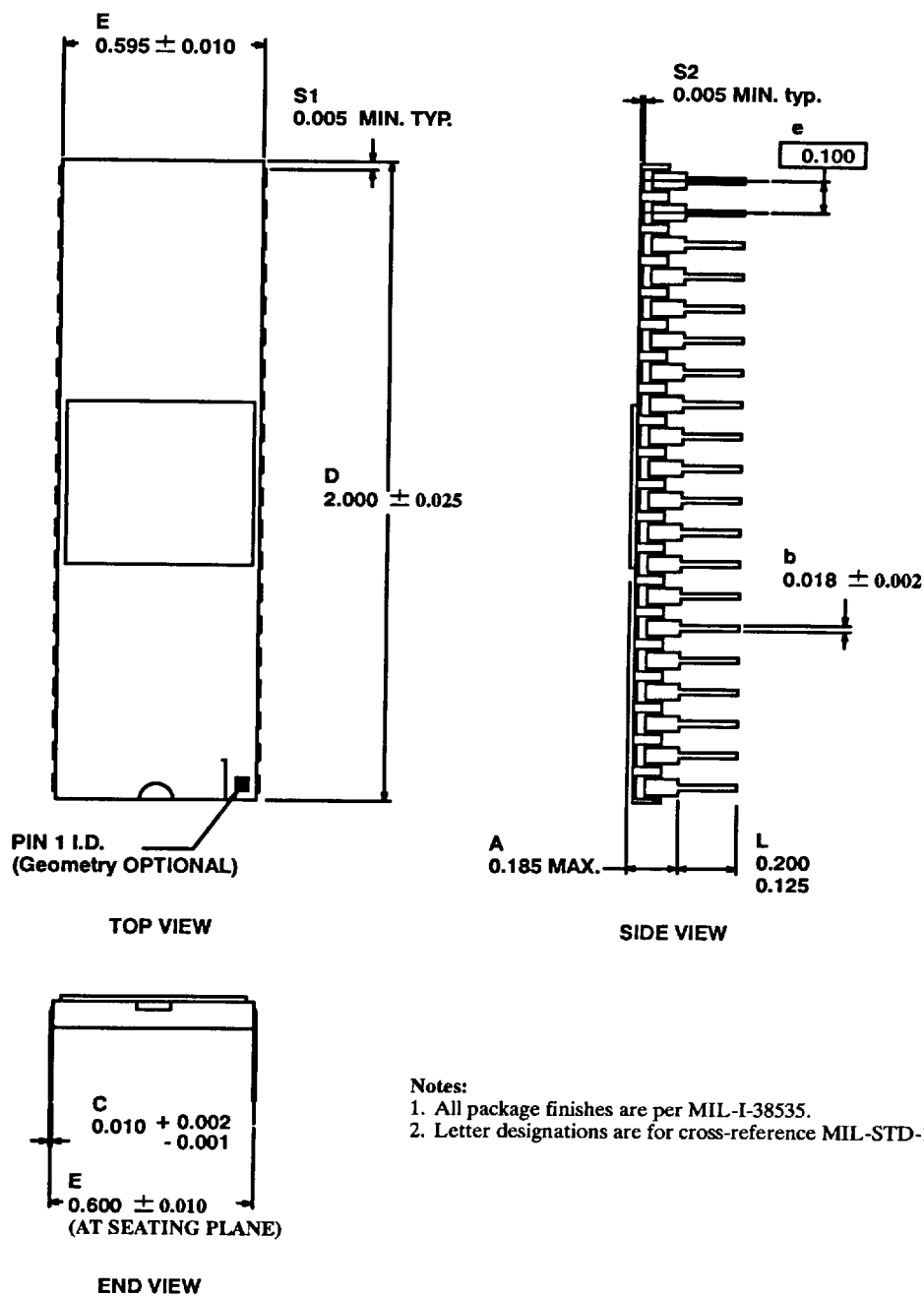| SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
$1/t_{CLCL}$	Oscillator Frequency		16	MHz
t_{CHCX}	High Time	20		ns
t_{CLCX}	Low Time	20		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Figure 10. External Clock Drive Timing Waveforms

10.0 PACKAGING

TOP VIEW

E
0.595 ± 0.010

S1
0.005 MIN. TYP.

D
2.000 ± 0.025

PIN 1 I.D.
(Geometry OPTIONAL)

SIDE VIEW

S2
0.005 MIN. typ.

e
0.100

b
0.018 ± 0.002

A
0.185 MAX.

L
0.200
0.125

END VIEW

C
0.010 + 0.002
      - 0.001

E
0.600 ± 0.010
(AT SEATING PLANE)

Notes:
1. All package finishes are per MIL-I-38535.
2. Letter designations are for cross-reference MIL-STD-1835.

Figure 11. 40-pin Side-Brazed DIP

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There are a few areas in which the UT69RH051 differs from the 8XC51FC. These differences will be covered in this section. In this discussion, 8XC51FC will be used generically to refer to all speed grades of the Intel 8XC51FC family, including the 20MHz 8XC51FC-1.

1.0 RESET

The UT69RH051 requires the RST input to be held high for at least 24 oscillator periods to guarantee the reset is completed in the chip. Also, the port pins are reset asynchronously as soon as the RST pin is pulled high. On the UT69RH051 all portions of the chip are reset synchronously when the RST pin is high during a rising edge of the input clock. When coming out of reset, the 8XC51FC takes 1 to 2 machine cycles to begin driving ALE and $\overline{PSEN}$ immediately after the RST is removed but the access during the first machine cycle after reset is ignored by the processor. The second cycle will repeat the access and processing will begin.

2.0 POWER SAVING MODES OF OPERATION

2.1 Idle Mode

Idle mode and the corresponding control bit in the PCON SFR have not been implemented in the UT69RH051. Setting the idle control bit will have no effect.

2.2 Power Down Mode

Power down mode and the corresponding control bit in the PCON register have not been implemented in the UT69RH051. Setting the power down control bit will have no effect. Also, the Power Off Flag in the PCON has not been implemented.

3.0 ON CIRCUIT EMULATION

The On Circuit Emulation mode of operation in the 8XC51FC has not been implemented in the UT69RH051.

4.0 OPERATING CONDITIONS

The operating voltage range for the 8XC51FC is 5V ± 20%. The operating temperature range is 0° to 70°C. On the UT69RH051, the operating voltage range is 5V ± 10%. The operating temperature range is -55° to +125°C.

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APPENDIX B
Impact of External Program ROM

The 8051 family of microcontrollers, including the 8XC51FC, use ports 0 and 2 to access external memory. In implementations with external program memory, these two ports are dedicated to the program ROM interface and can not be used as Input/Output ports. The UT69RH051 uses external program ROM, so ports 0 and 2 will not be available for I/O.