DS3LIM
DS3 Line Interface Module
NRZ Clock/Data Output
TXC-20049D

DATA SHEET

FEATURES

- Complete B3ZS analog to NRZ digital DS3 line interface unit in a compact 2.6 square-inch module
- Analog inputs and outputs are transformer coupled
- Speeds time to market for prototype development
- Eases parts inventory and acquisition
- Eases field maintenance
- Meets ANSI Standard T1.102

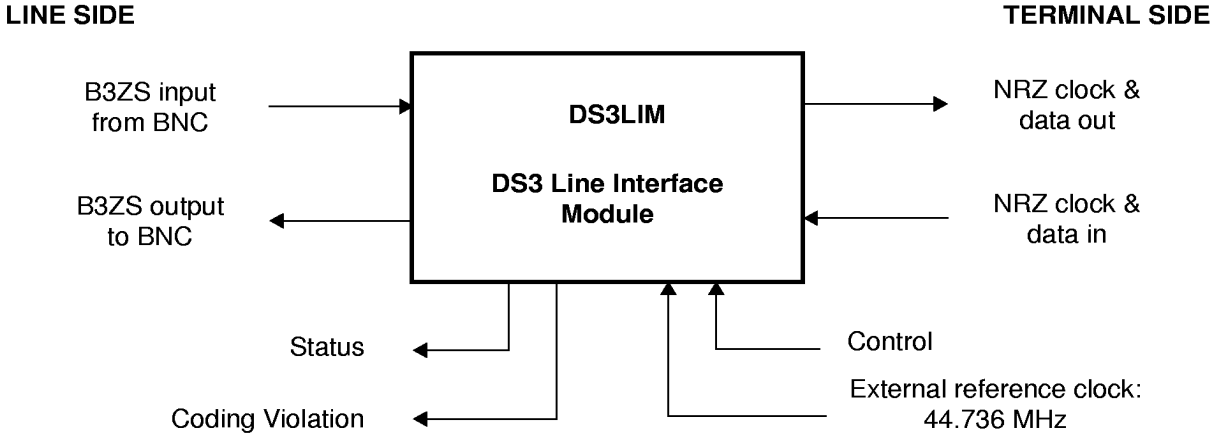
DESCRIPTION

TranSwitch's DS3 Line Interface Module (DS3LIM) is a complete and compact analog to digital interface serving B3ZS encoded DS3 signals. Sensitive analog circuitry provides compliant DS3 specified performance in signal recovery and transmission. With the module's platform design, engineers are freed from the laborious tasks of schematic capture, component placement, and trace routing. This results in a "single PASS" for printed circuit board design of the DS3 analog section.

Accumulative reduction in design time, design cycles, parts acquisition, unit building and testing mean an efficient format for reducing product time to market.

APPLICATIONS

- DS3 interface for quick "time to market" products



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BLOCK DIAGRAM

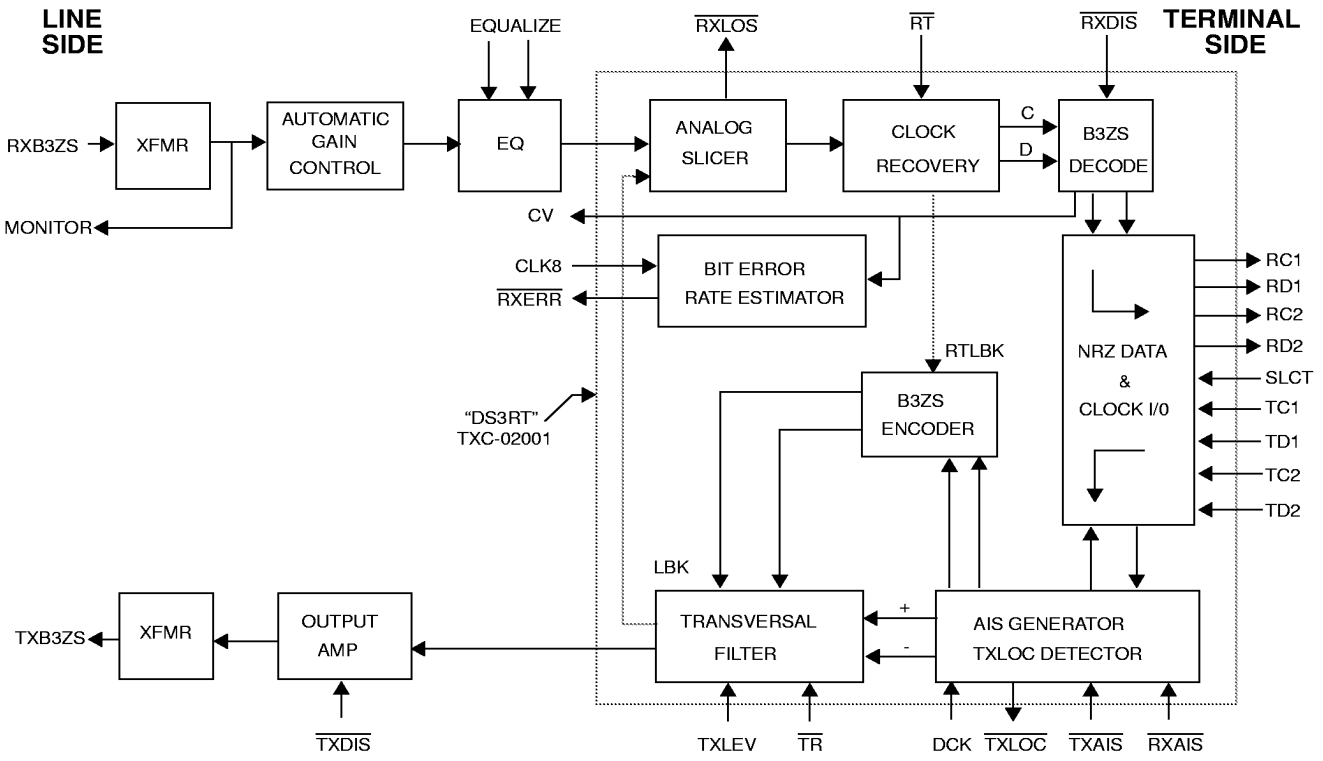


Figure 1. DS3LIM Block Diagram

BLOCK DIAGRAM DESCRIPTION

The DS3LIM receives a bipolar B3ZS encoded DS3 signal from a BNC or other connector. This signal is AC coupled into the DS3LIM through a 1:1 transformer (XFMR). From the transformer, the signal is terminated into 75Ω and placed into the input of an Automatic Gain Control (AGC) circuit. A Monitor pin is also provided to observe the received signal. The AGC provides the Equalizer Circuit (EQ) with a constant signal level. The equalizer is switched in and out to recover narrow or wide width DS3 signals respectively. From the equalizer circuit, the bipolar signal is AC coupled into the receiver Analog Slicer circuit of the TXC-02001 device. The line signal is monitored for transitions, and a loss of signal is provided on the signal pin labelled $\overline{\text{RXLOS}}$.

The Clock Recovery Block requires an external 44.736 MHz clock (DCK) with a stability of approximately ± 200 ppm. The stability of DCK must be increased to ± 20 ppm if the transmit or receive AIS features are used. The average time to recover the clock is approximately one millisecond when the line signal is applied.

The B3ZS (bipolar with 3-zero substitution) line coded data is decoded by the B3ZS Decode Block. Indications of coding violation errors, other than the normal B3ZS coding substitutions are provided on the signal pin CV. Bipolar coding errors can occur because of noise and other impairments on the line. In addition to providing an external indication of such errors, the measurement of these coding violations provides a close estimate for determining the Bit Error Rate (BER) performance of the line. An external 8 kHz clock (CLK8) is used by the Bit Error Rate Estimator Block to generate a 10-second sampling window for detecting a 10^{-6} or greater error rate. The 10^{-6} or greater error rate indication is provided on the signal pin labelled $\overline{\text{RXERR}}$.

The DS3LIM provides the capability to generate and insert a DS3 Alarm Indication Signal (AIS) into the NRZ receive data signal. A low placed on the $\overline{\text{RXAIS}}$ pin enables the AIS generator. This pin may be connected to the receive loss of signal ($\overline{\text{RXLOS}}$) pin to generate AIS.

Two receive output ports consisting of a clock and data signal are provided. The first receive output port is labelled RC1 and RD1; the second is labelled RC2 and RD2. Only one clock and data port can be active at a time. Data (RD1/RD2) is clocked out of the DS3LIM with respect to the falling edge of the receive clock (RC1/RC2). The selection of the receive output port is controlled by the state of the select pin (SLCT). The unused port is forced into a high impedance state. In addition, the two receive ports can be both disabled and forced into a high impedance state by placing a low on the $\overline{\text{RXDIS}}$ pin.

In the transmit direction, two transmit ports consisting of clock and data are also provided. The first transmit port is labelled TC1 and TD1; the second is labelled TC2 and TD2. Transmit input data (TD1/TD2) is clocked into the DS3LIM on positive transitions of the clock signal (TC1/TC2). Like the receiver section, the SLCT pin determines the transmit input port selection.

The transmit input clock signal is monitored by the AIS Generator $\overline{\text{TXLOC}}$ Detector Block. A transmit loss of clock alarm indication pin ($\overline{\text{TXLOC}}$) is provided. This block also provides the capability to generate and transmit a DS3 Alarm Indication Signal (AIS), which is independent of the transmit data. A low placed on the $\overline{\text{TXAIS}}$ pin enables the transmit DS3 AIS generator. The $\overline{\text{TXLOC}}$ pin may be connected to the $\overline{\text{TXAIS}}$ pin for generating AIS.

The incoming data is encoded by the B3ZS encoder. In the B3ZS line code, each block of three consecutive zeros is removed and replaced by either of two codes that contain bipolar violations. These replacement codes are B0V and 00V, where B represents a pulse that conforms to the bipolar rule and V represents a pulse violating the rule. The choice of these codes is made so that an odd number of bipolar conforming pulses (B) is transmitted between consecutive bipolar violation pulses (V). The encoded data is connected to the Transversal Filter Block.

The Transversal Filter uses a raised cosine tap delay line for shaping the signal to the limits specified for the DS3 pulse mask. The DS3 pulse mask is then amplified externally to the TXC-02001 device via a current amplifier to drive 75Ω coax. The DS3LIM also has the capability of de-activating its transmit output via the $\overline{\text{TXDIS}}$ pin. When $\overline{\text{TXDIS}}$ is set low, the output impedance of the TXB3ZS port becomes a high impedance state.

In addition to the alarms and control signals, the DS3LIM provides two loopback capabilities for testing transmit and receive loopback. Transmit loopback connects the data path from the transmitter output driver stage to the receiver input, and disables the external receiver input. Transmit loopback is activated by placing a low on the $\overline{\text{TR}}$ signal pin. Receive loopback connects the receive data path to the transmit output circuits and disables the NRZ transmit input. Receive loopback is activated by placing a low on the $\overline{\text{RT}}$ pin.

PIN DIAGRAM

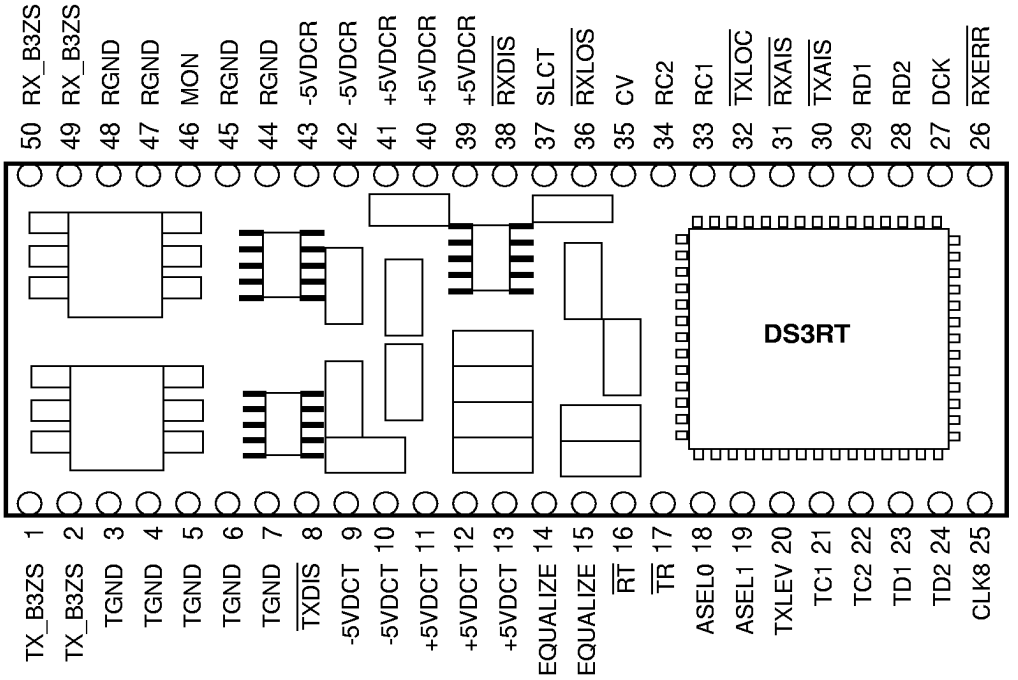


Figure 2. DS3LIM Pin Diagram

PIN DESCRIPTIONS

Symbol	Pin No.	I/O/P*	Type **	Name/Function
TX_B3ZS	1, 2	O		**Transmit DS3 B3ZS Output:** These pins are AC-coupled B3ZS encoded DS3 output signals. They may be applied directly to a 75Ω BNC connector. Under normal operation, this output has a 75Ω source impedance. When $\overline{\text{TXDIS}}$ is low, this output is placed into a high-impedance disabled condition.
TGND	3, 4, 5, 6, 7	P		**Transmit Ground:** Ground pin for transmit side circuitry.
$\overline{\text{TXDIS}}$	8	I	CMOS or TTL	**Transmit Disable:** An active low on this pin disables the DS3 transmitted signal. When left open, TX is enabled.
-5VDCT	9, 10	P		**Transmit -5VDC:** -5VDC inputs for transmit side circuitry.
+5VDCT	11, 12, 13	P		**Transmit +5VDC:** +5VDC inputs for transmit side circuitry.

* Note: I = Input; O = Output; P = Power
**Note: Electrical parameters of each type are defined in the next section of this Data Sheet.

Symbol	Pin No.	I/O/P	Type	Name/Function
EQUALIZE	14, 15	-	Passive	**Equalize:** These two pins are used to select equalization on the incoming receive signal. Left open, they select the EQ values for long cable (200' - 450'). If these two pins are shorted together, the EQ values are changed for short lengths of cable (0' - 200').
$\overline{RT}$	16	I	CMOSr	**Receive To Transmit Loopback:** An active low enables the receive loopback feature. This loopback connects the receive data path to the transversal filter, and disables the NRZ transmit input. (See Note 1)
$\overline{TR}$	17	I	CMOSr	**Transmit To Receive Loopback:** An active low enables the transmit loopback feature. This loopback connects a transmit data path at the output to the receive input, and disables the DS3 receive line signal. (See Note 1)
ASEL0 ASEL1	18 19	I I	CMOSr CMOSr	**Amplifier Select:** These two pins must have 10 kΩ, 5%, 1/8 W external pull-up resistors to VCC. No other connections should be made to these pins.
TXLEV	20	I	CMOSr	**Transmit Level:** This pin should be connected to ground for normal DSX-3 operation. Left open, a higher transmit level is provided.
TC1	21	I	TTLr	**Transmit Input Clock #1:** When a high is placed on the SLCT lead, TC1 is the input pin for the NRZ transmit clock. This clock has a 50% ± 5% duty cycle.
TC2	22	I	TTLr	**Transmit Input Clock #2:** When a low is placed on the SLCT lead, TC2 is the input pin for the NRZ transmit clock. This clock has a 50% ± 5% duty cycle.
TD1	23	I	TTL	**DS3 Transmit Input Data Port 1:** Data is clocked in on positive transitions of TC1. This port is enabled by placing an active high on the SLCT lead.
TD2	24	I	TTL	**DS3 Transmit Input Data Port 2:** Data is clocked in on positive transitions of TC2. This port is enabled by placing an active low on the SLCT lead.
CLK8	25	I	TTL	**Eight kHz Clock Input:** This clock is required for generating a 10-second time base that is used for the error rate measurement only. The clock duty cycle should be 50% ± 10%. When not used, this pin should be tied to VCC via a 10 KΩ resistor.
$\overline{RXERR}$	26	O	TTL2mA	**Receive Error Rate:** An active low indication occurs when the number of bipolar coding errors causes the bit error rate to exceed 10^{-6}. The indication is present for the 10-second sampling window.This output is only valid when an 8 kHz clock is applied to the CLK8 pin.

Note 1: Setting $\overline{RT}$ and $\overline{TR}$ low simultaneously will cause invalid outputs at the receive terminal and transmit line ports.

Symbol	Pin No.	I/O/P	Type	Name/Function
DCK	27	I	TTL	**External Clock**: An external 44.736 MHz clock having a stability of ± 200 ppm (± 20 ppm if the AIS feature is used), and a duty cycle of 50% ± 5% is required for DS3 operation. The external clock is used by the receiver for clock recovery, and by the transmitter for the transversal filter. If the duty cycle is relaxed, the transmitted mask may not meet DS3 pulse mask requirements.
RD2	28	O	TTL4mA	**DS3 Receive Output Data Port 2:** Data is clocked out on positive transitions of RC2. This port is enabled by placing an active low on the SLCT lead. When this port is disabled by placing a high on the SLCT or a low on the $\overline{\text{RXDIS}}$ control leads, the output goes to a high impedance state.
RD1	29	O	TTL4mA	**DS3 Receive Output Data Port 1:** Data is clocked out on positive transitions of RC1. This port is enabled by placing an active high on the SLCT lead. When this port is disabled by placing a low on the SLCT or a low on the $\overline{\text{RXDIS}}$ control leads, the output goes to a high impedance state.
$\overline{\text{TXAIS}}$	30	I	TTLr	**Transmit AIS:** An active low placed on this pin disables the transmit data input, and causes a DS3 alarm indication signal to be generated and sent as transmitted data on the TXB3Z output. (See Note 2)
$\overline{\text{RXAIS}}$	31	I	CMOSr	**Receive AIS:** An active low placed on this pin disables receive data, and causes a DS3 alarm indication signal to be generated and sent on the RD1 or RD2 pins. (See Note 2)
$\overline{\text{TXLOC}}$	32	O	TTL2mA	**Transmit Loss of Clock:** An active low alarm occurs when the input transmit clock is stuck high or low for a time exceeding 500 clock cycles. Recovery occurs on the first clock transition. This alarm lead may be connected to the $\overline{\text{TXAIS}}$ pin for generating a transmit DS3 AIS.
RC1	33	O	CMOS8mA	**DS3 Receive Output Clock Port 1:** This port is enabled by placing an active high on the SLCT lead. When this port is disabled by placing a low on the SLCT or a low on the $\overline{\text{RXDIS}}$ control leads, the output goes to a high impedance state.
RC2	34	O	CMOS8mA	**DS3 Receive Output Clock Port 2:** This port is enabled by placing an active low on the SLCT lead. When this port is disabled by placing a high on the SLCT or a low on the $\overline{\text{RXDIS}}$ control leads, the output goes to a high impedance state.

Note 2: DS3 AIS is defined as a valid M-frame with proper subframe structure. The data payload is a 1010 ... sequence starting with a 1 after each overhead bit. Overhead bits are as follows: F0=0, F1=1, M0=0, M1=1; C-bits are set to 0; X-bits are set to 1; and P-bits are set for valid parity.

Symbol	Pin No.	I/O/P	Type	Name/Function
CV	35	O	TTL2mA	**Coding Violation:** A positive pulse having a duration of one clock cycle is provided on this pin whenever an illegal B3ZS coding violation occurs.
$\overline{\text{RXLOS}}$	36	O	TTL2mA	**Receive Loss of Signal:** An active low alarm is generated when a positive or negative data transition does not occur for 128 or more clock cycles. Recovery occurs on the first positive or negative transition.
SLCT	37	I	CMOSr	**Select Port 1 or 2:** The ports are enabled and disabled according to the following table:
$\overline{\text{RXDIS}}$	38	I	CMOSr	**Receive Disable Ports 1 and 2:** An active low placed on this pin disables port 1 (RD1 and RC1), and port 2 (RD2 and RC2). The data and clock signal leads are forced to a high impedance state.
+5VDCR	39, 40, 41	P		**Receive +5VDC:** +5VDC input for receive side circuitry.
-5VDCR	42, 43	P		**Receive -5VDC:** -5VDC input for receive side circuitry.
RGND	44, 45, 47, 48	P		**Receive Ground:** Ground pins for receive side circuitry.
MON	46	O		**DS3 Received Signal Monitor Point:** This output is directly tied to the terminating resistor after transformer coupling. Care must be taken to ensure very short trace lengths to the MON buffer, or oscillation of the AGC may occur. If a monitor output is not required, it is suggested that this pin be left open.
RX_B3ZS	49, 50	I		**Receive DS3 B3ZS Input:** These pins are the AC-coupled B3ZS encoded DS3 input signal. They may come directly from a 75 ohm BNC connector.

Select	High	Low
RD1	Enabled	High Z
RC1	Enabled	High Z
TD1	Enabled	High Z
TC1	Enabled	High Z
RD2	High Z	Enabled
RC2	High Z	Enabled
TD2	High Z	Enabled
TC2	High Z	Enabled

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}		7.0	V
Supply voltage	V_{EE}		-7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		1.5	W
Ambient operating temperature	T_A	0	70	°C
Storage temperature range	T_S	-55	150	°C

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
V_{EE}	-5.25	-5.0	-4.75	V	
I_{DD}			200	mA	V_{DD} = 5.25V
I_{EE}			100	mA	V_{EE} = 5.25V
P_{DD}			1.0	W	V_{DD} = 5.25V
P_{EE}			0.5	W	V_{EE} = 5.25V

INPUT, OUTPUT, AND I/O PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Input Parameters For TTLr

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		50	120	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Note: Input has a 100K (nominal) internal pull-up resistor.

Input Parameters For CMOSr

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		50	120	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Note: Input has a 100K (nominal) internal pull-up resistor.

Output Parameters For TTL2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -1.0$ mA
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 2.0$ mA
I_{OL}			2.0	mA	
I_{OH}			-1.0	mA	
t_{RISE}	5.5	12.5	18.2	ns	$C_{LOAD} = 15$pF
t_{FALL}	2.3	4.4	6.5	ns	$C_{LOAD} = 15$pF

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0 mA
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0 mA
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.8	6.5	9.2	ns	C_{LOAD} = 15 pF
t_{FALL}	1.3	2.3	3.4	ns	C_{LOAD} = 15 pF

Output Parameters For CMOS8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -8.0 mA
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0 mA
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}	1.3	2.4	3.8	ns	C_{LOAD} = 25 pF
t_{FALL}	1.1	1.8	2.5	ns	C_{LOAD} = 25 pF

Receiver Sensitivity

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	180		1000	mVp	

Input Parameters For Transformer Coupling

Parameter	Min	Typ	Max	Unit	Test Conditions
Return Loss		- 26		dB	22.368 MHz; 25°C
Isolation Voltage			300	Vrms	
Turns Ratio		1:1			
Input Impedance	67.5	75	82.5	ohms	

Output Parameters For Transformer Coupling

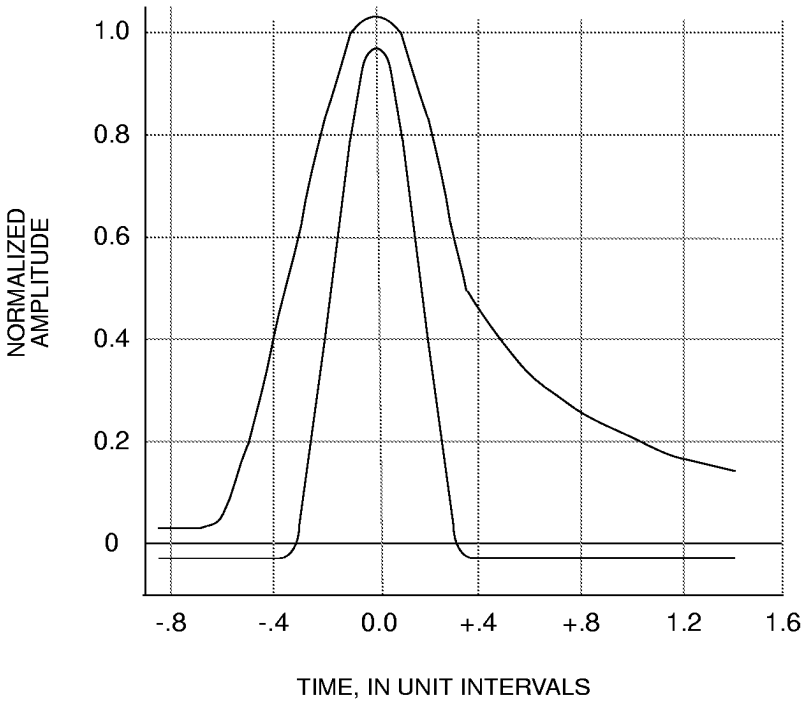
Parameter	Min	Typ	Max	Unit	Test Conditions
Isolation Voltage			300	Vrms	
Turns Ratio		1:1			
Output Impedance ($\overline{TXDIS}$ = 1)	67.5	75	82.5	ohms	
Output Impedance ($\overline{TXDIS}$ = 0)	100k	200k		ohms	

TIMING CHARACTERISTICS

Detailed timing diagrams for the DS3LIM are illustrated in Figures 3 through 5. All output times are measured with maximum load capacitance appropriate for the pin type. Timing parameters are measured at (V_{OH} - V_{OL})/2 or (V_{IH} - V_{IL})/2 as applicable.

Line Side Timing Characteristics

The line side signal characteristics are designed so that the output mask terminated into a test load of 75Ω ± 5% using ATT 734A coaxial cable will meet the DSX-3 isolated pulse template shown below for cable distances between 0 and 450 feet. The pulse amplitude is between 360 and 850 millivolts measured at the center of the pulse.



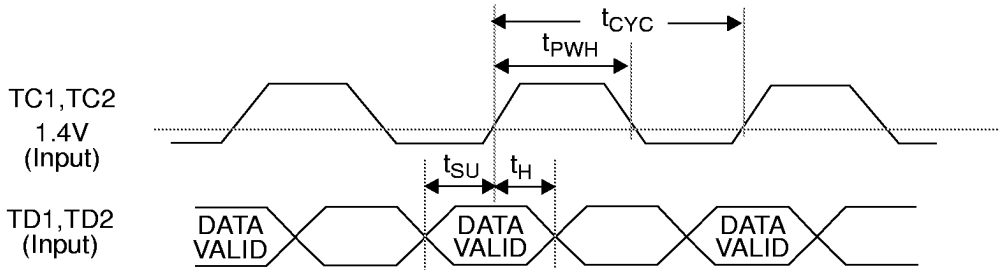
DSX-3 PULSE TEMPLATE BOUNDARIES

CURVE	TIME UNIT INTERVALS	NORMALIZED AMPLITUDE
MAXIMUM CURVE	$-0.85 \le T \le -0.68$	0.03
	$-0.68 \le T \le 0.36$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.34}\right)\right]+0.03$
	$0.36 \le T \le 1.4$	$0.08 + 0.407e^{-1.84(T-0.36)}$
MINIMUM CURVE	$-0.85 \le T \le -0.36$	-0.03
	$-0.36 \le T \le 0.36$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.18}\right)\right]-0.03$
	$0.36 \le T \le 1.4$	-0.03

Figure 3. DSX-3 Isolated Pulse Template and Equations

Terminal Side Timing Characteristics

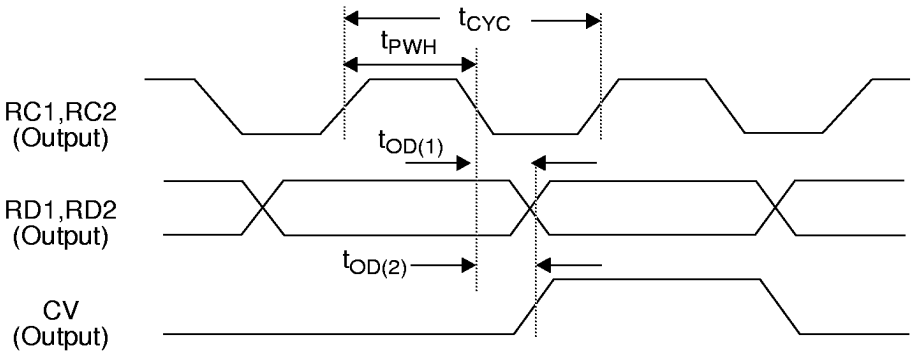
Figure 4. NRZ Transmit Input



Parameter	Symbol	Min	Typ	Max	Unit
TC1, TC2 clock period	t_{CYC}		22.35		ns
TC1, TC2 high time	t_{PWH}	10			ns
TC1, TC2 duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TD1, TD2 set-up time to TC1↑, TC2↑	t_{SU}	3			ns
TD1, TD2 hold time after TC1↑, TC2↑	t_H	2			ns

Note: TC1, TC2 symmetry is measured about the 1.4VDC threshold in order to assure symmetric output waveforms.

Figure 5. NRZ Receive Output



Parameter	Symbol	Min	Typ	Max	Unit
RC1, RC2 clock period	t_{CYC}		22.35		ns
RC1, RC2 high time	t_{PWH}	10			ns
RC1, RC2 duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
$\overline{RD1}$, $\overline{RD2}$ output delay after RC1↓, RC2↓ ($\overline{RXAIS}$ = 1)	$t_{OD(1)}$	-5		5	ns
$\overline{RD1}$, $\overline{RD2}$ output delay after RC1↓, RC2↓ ($\overline{RXAIS}$ = 0)	$t_{OD(1)}$	-5		6.5	ns
CV output delay after RC1↓, RC2↓	$t_{OD(2)}$	-5		5	ns

Note: RC1, RC2 symmetry is measured about the 50% amplitude point.

Operation

Interfering Tone Tolerance

The DS3LIM will properly recover the clock and provide an error-free output in the presence of a 2^{23} -1 encoded DS3 interfering tone up to -16 db below the level of the DS3 input signal.

Jitter Transfer

Transfer of jitter through an individual unit of digital equipment is characterized by the relationship between the applied input jitter and the resulting output jitter as a function of frequency. Bellcore Technical Reference TR-TSY-000499, Issue 3, December 1989 further describes and defines jitter transfer.

In a looped back configuration (through the receive path and externally looped back through the transmit path), in the absence of applied input jitter the amount of jitter introduced by the DS3LIM is maximum 0.02 Unit Intervals (UIs) of peak-to-peak jitter over a jitter frequency range of 20 Hz to 1 Mz.

With applied input jitter, the maximum output jitter is the applied input jitter plus the above jitter introduced by the DS3LIM.

Jitter Generation

Jitter generation is the process whereby jitter appears at the output port of an individual unit of digital equipment in the absence of applied input jitter.

Bellcore Technical Reference TR-TSY-000499, Issue 3, December 1989 specifies the maximum jitter generation to be 1.0 UI of peak-to-peak at the output of the terminal receiver for Category I equipment.

In a looped back configuration (through the transmit path and externally looped back through the receive path), the jitter generation within the DS3LIM is maximum 0.02 UI peak-to-peak for all frequencies specified in the standard.

Jitter Tolerance

Input jitter tolerance is the maximum amplitude of sinusoidal jitter at a given jitter frequency, which, when modulating the signal at an equipment port, results in no more than two errored seconds cumulative, where these errored seconds are integrated over successive 30-second measurement intervals, and the jitter amplitude is increased in each succeeding measurement interval.

Requirements on input jitter tolerance are specified in terms of compliance with a jitter mask, which represents a combination of points. Each point corresponds to minimum amplitude of sinusoidal jitter at a given jitter frequency which, when modulating the signal at an equipment input port, results in two or fewer errored seconds in a 30-second measurement interval. Bellcore Technical Reference TR-TSY-000499, Issue 3, December 1989 specifies the minimum requirement mask for Category II equipment. The mask is shown in Figure 6 (next page).

Jitter tolerance within the DS3LIM is well within the acceptance range as specified by the mask. Figure 6 on the next page shows the measured DS3LIM jitter tolerance and the Bellcore minimum jitter tolerance requirement mask.

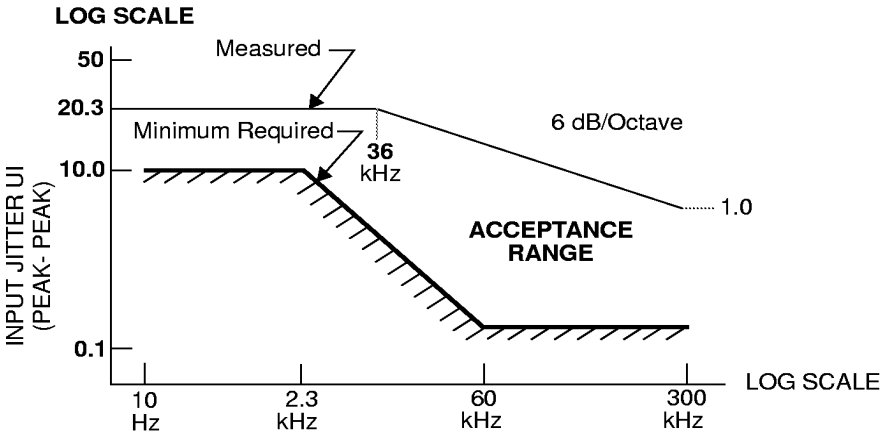


Figure 6. DS3LIM Jitter Tolerance at 44.736 Mbit/s

POWER SUPPLY

The recommended power supply connections to the DS3LIM are shown below in Figure 7.

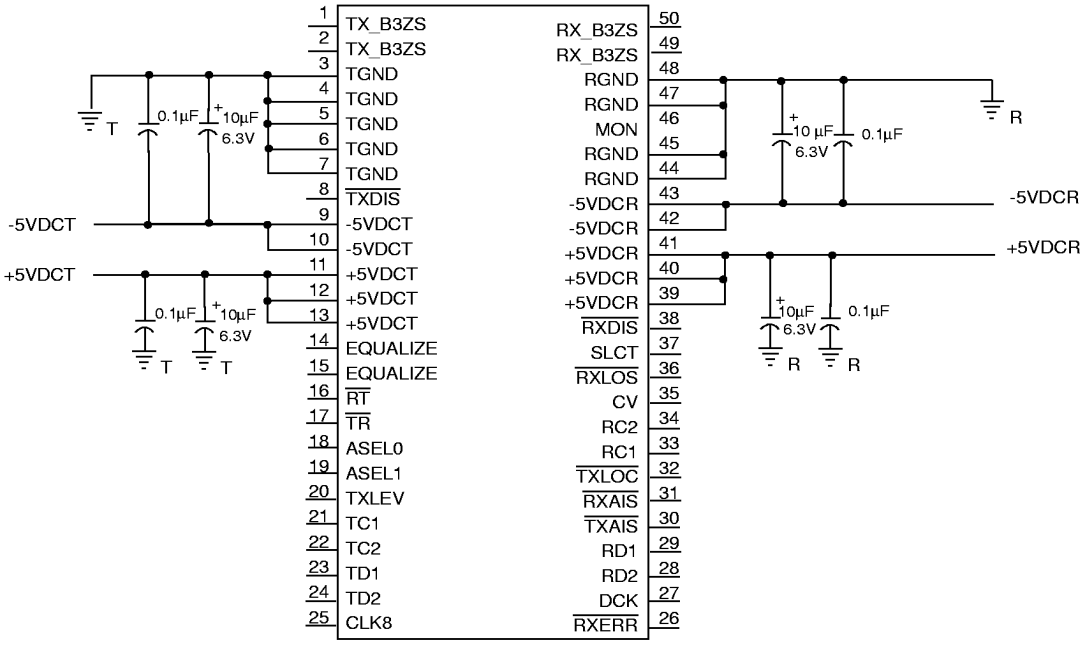


Figure 7. Power Supply Connections

PACKAGING

The DS3 Line Interface Module consists of a compact multi-layer printed circuit board, surface mounted components mounted on top and bottom layers, and 50 pins on 0.1 inch centers in a DIP configuration. The outline drawing is shown below in Figure 8.

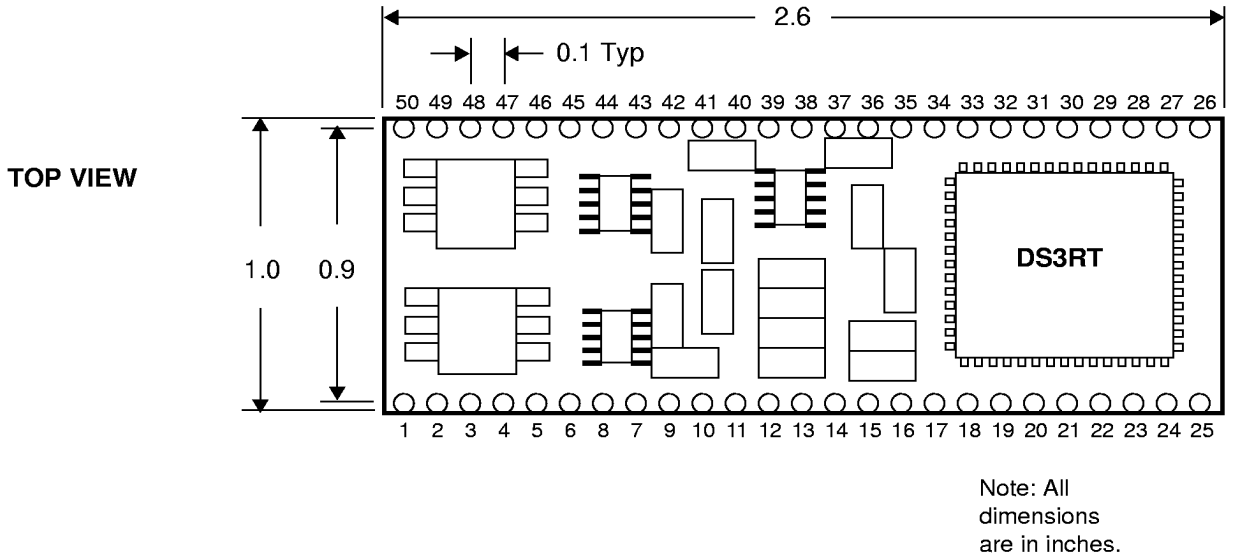


Figure 8. DS3LIM Outline Drawing

The DS3LIM can be installed with or without a socket on the motherboard as shown in Figures 9 and 10. All dimensions are in inches.

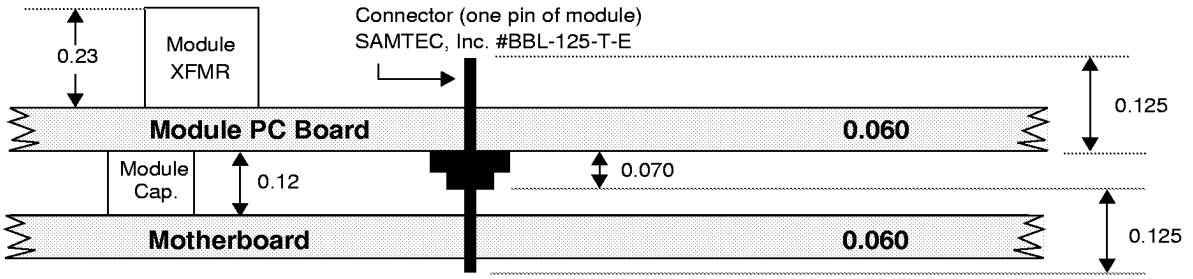


Figure 9. Installation Without Motherboard Socket

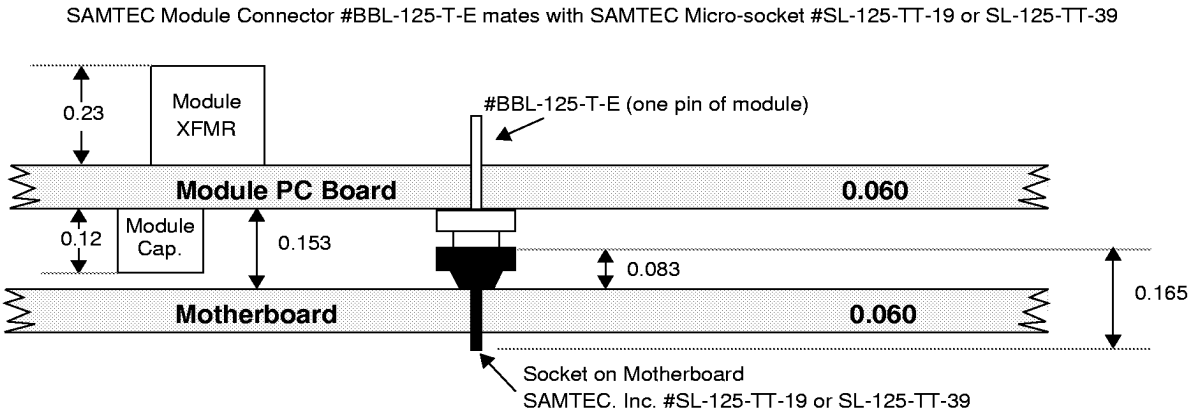


Figure 10. Installation With Motherboard Socket

Notes:
1. All dimensions in inches.
2. Drawings not to scale.
3. SAMTEC, Inc.
   P.O. Box 1147
   New Albany, Indiana 47151-1147 USA
   Phone: 812-944-6733
   Fax: 812-948-5047
   TWX: 810-540-4095
   Telex: 333-918

ORDERING INFORMATION

Part Number: TXC-20049-DCMM	DS3 Line Interface Module NRZ Clock/Data Output 50-Pin Dual In-Line Package

RELATED PRODUCTS

TXC-21049, DS3LIM Evaluation Board. A complete, ready-to-use test bed for the test and evaluation of the DS3LIM Line Interface Module. The module plugs into a socket on the evaluation board, input and output signals are terminated via BNC connectors, and all functions of the module are selectable via jumper insertion/extraction on the evaluation board.

TXC-03301, M13 VLSI Device (DS3/DS1 Mux/Demux). This single-chip multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals.

TXC-03303, M13E VLSI Device. Extended feature version of the TXC-03301 (M13).

TXC-03375, M12 VLSI Device (DS2/DS1 Mux/Demux). Multiplexes four DS1 signals into one DS2 signal, and in the other direction demultiplexes one DS2 signal into its four constituent DS1 signals.

TXC-03401, DS3F VLSI Device (DS3 Framer). Maps broadband payloads into the DS3 frame format. Operates in either the C-bit parity or M13 operating modes.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

CCITT:

Publication Services of ITU
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated DS3LIM Data Sheet that have technical differences relative to the superseded DS3LIM Data Sheet:

Updated DS3LIM Data Sheet: Edition 3, April 1994

Superseded DS3LIM Data Sheet: Edition 2, September 1992

The page numbers indicated below of the updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date on all pages.
Various	Changed name of pin number 35 (BPV) to CV (for Coding Violation).
1	Added NRZ Clock/Data Output to the Heading.
1	Added ANSI Standard to Features List.
1	Modified Description.
1	Replaced BPV error pulse with Coding Violation in the I/O diagram.
2-3	Added new Figure 1, Block Diagram, and Block Diagram Description.
4-7	Enhanced the pin descriptions.
8	Deleted the Operating junction temperature from the Absolute Maximum Ratings.
8	Added Test Conditions to I_{EE} and P_{EE}.
10	Added three new tables: Input Parameters for Transformer Coupling, Output Parameters for Transformer Coupling, and Receiver Sensitivity.
11	Improved accuracy of Figure 3.
12	Revised Figures 4 and 5 Timing Diagrams.
13-14	Revised.
16	Added Figures 9 and 10 to Packaging section.
17	Corrected part number in Ordering Information section and added Related Products section.
18	Added Standards Documentation Sources.