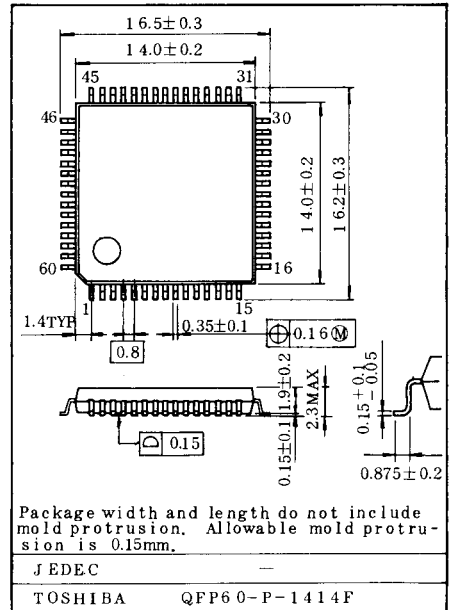# TA8443F

PLL-PWM 3-PHASE HALL MOTOR PRE-DRIVER

TA8443F is 3-phase hall motor pre-driver with
PLL controller and PWM controller.
8 bit D/A converter system has been employed
for each of the speed control system (AFC) and
the phase control system (APC).
TA8443F contains two error amplifiers, adjustable
oscillator, dead-time control comparator, pulse-
steering flip-flop, and output-control circuit.

- This is multi-chip IC with TC9203, TA76494 and
  TA7712.

- Start/stop, CW/CCW and brake function are
  provided.

- Package is QFP-60.

- For further details, refer to each technical
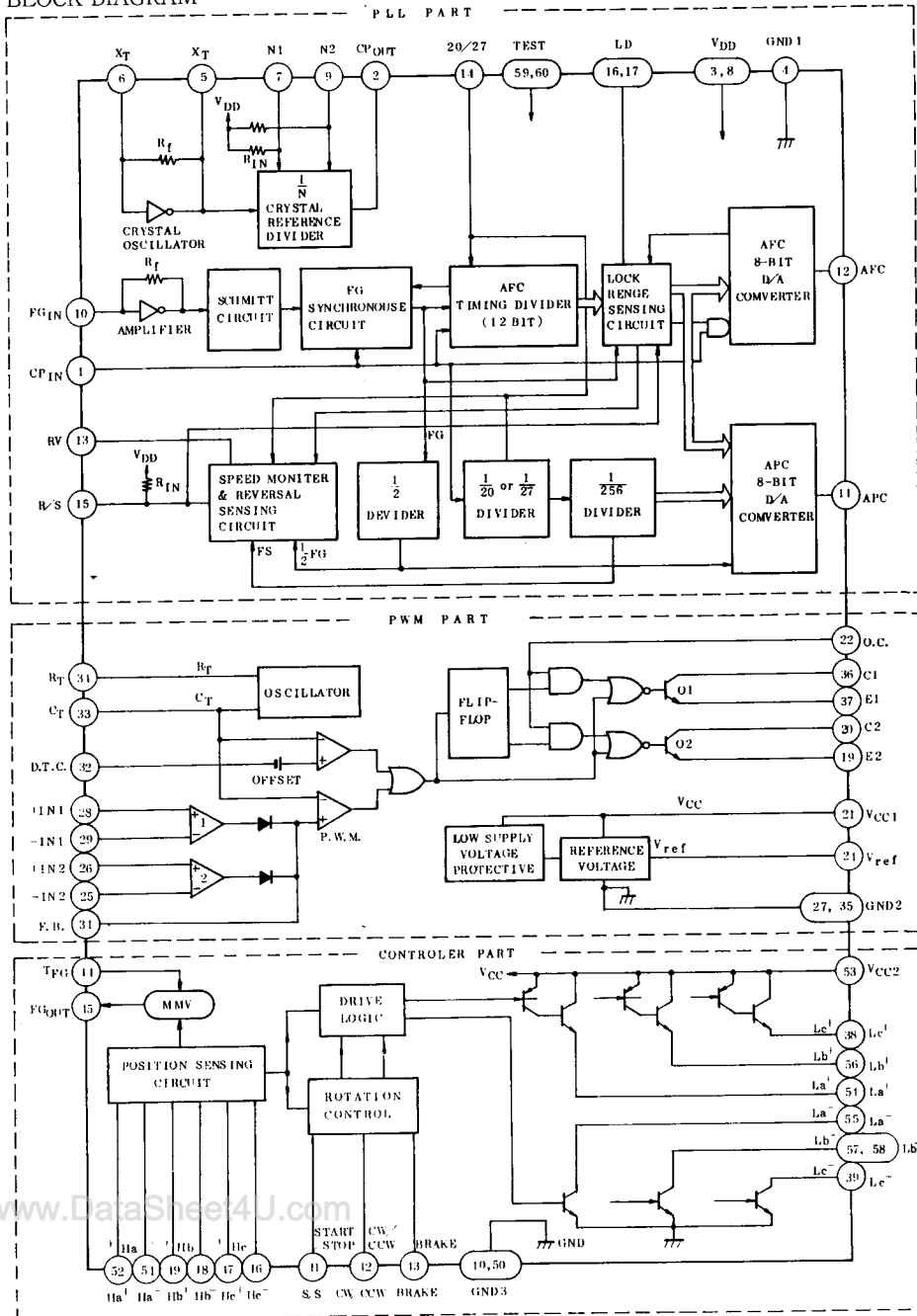 data.

Unit in mm

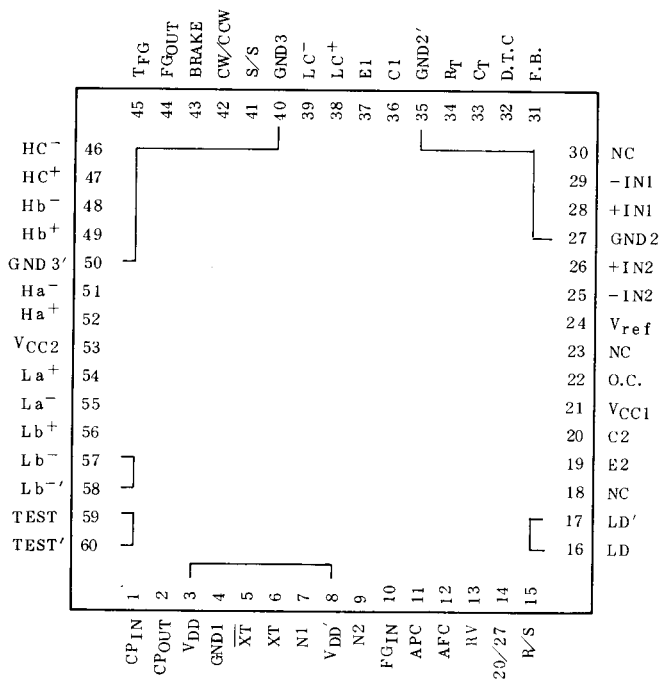Package width and length do not include
mold protrusion. Allowable mold protru-
sion is 0.15mm.

JEDEC	—
TOSHIBA	QFP60-P-1414F

MAXIMUM RATINGS (Ta=25°C)

BLOCK	CHARACTERISTIC	SYMBOL	RATING	UNIT
PULL part (TC9203)	Supply Voltage	V_{DD}	$-0.3 \sim 7.0$	V
	Input Voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V
PWM part (TA76494)	Supply Voltage	V_{CC1}	30	V
	Amplifier Input Voltage	V_{ICM}	$V_{CC}+0.3$	V
	Collector Output Voltage	V_{CER}	30	V
	Collector Output Current	I_C	250	mA
Controller part (TA7712)	Power Supply Voltage	V_{CC2}	8.0	V
	Output Current	I_O	± 25	mA
	Position Sensing Circuit Input Voltage (Tj=25°C)	V_H	± 500	mV
TA8443F	Power Dissipation	P_D	810	mW
	Operating Temperature	T_{opr}	$-30 \sim 75$	°C
	Storage Temperature	T_{stg}	$-55 \sim 1$	°C

—483—

BLOCK DIAGRAM

PLL PART

X_T 6 | X_T 5 | N1 7 | N2 9 | CP_{OUT} 2 | 14 20/27 | TEST 59,60 | LD 16,17 | V_{DD} 3,8 | GND 1 4

V_{DD}

R_f

R_{IN}

$\frac{1}{N}$ CRYSTAL REFERENCE DIVIDER

CRYSTAL OSCILLATOR

R_f

FG_{IN} 10

AMPLIFIER

SCHMITT CIRCUIT

FG SYNCHRONOUSE CIRCUIT

AFC TIMING DIVIDER (12 BIT)

LOCK RENGE SENSING CIRCUIT

AFC 8-BIT D/A CONVERTER

12 AFC

CP_{IN} 1

RV 13

V_{DD}

R_{IN}

R/S 15

SPEED MONITER & REVERSAL SENSING CIRCUIT

FG

$\frac{1}{2}$ DEVIDER

$\frac{1}{20}$ or $\frac{1}{27}$ DIVIDER

$\frac{1}{256}$ DIVIDER

APC 8-BIT D/A CONVERTER

11 APC

FS $\frac{1}{2}$FG

PWM PART

22 O.C.

R_T 31 | R_T

C_T 33 | C_T | OSCILLATOR

FLIP-FLOP

O1

36 C1
37 E1

O2

30 C2
19 E2

D.T.C. 32

OFFSET

+IN1 28
-IN1 29

1

P.W.M.

+IN2 26
-IN2 25

2

V_{CC}

21 V_{CC1}

LOW SUPPLY VOLTAGE PROTECTIVE

REFERENCE VOLTAGE

V_{ref}

24 V_{ref}

F.B. 34

27, 35 GND2

CONTROLER PART

T_{FG} 11

FG_{OUT} 15

MMV

DRIVE LOGIC

V_{CC}

53 V_{CC2}

POSITION SENSING CIRCUIT

ROTATION CONTROL

Lc' 38 Lc'
Lb' 56 Lb'
La' 51 La'
La 55 La
Lb 57, 58 Lb
Lc 39 Lc

GND

Ha' 52 | Ha 51 | Hb' 49 | Hb 48 | Hc' 47 | Hc 46 | START STOP 11 | CW CCW 12 | BRAKE 13 | 10,50 GND3

Ha' Ha Hb' Hb Hc' Hc | S.S | CW CCW | BRAKE | GND

www.DataSheet4U.com

PIN CONNECTION

Top pins (left to right, 45–31): TFG, FGOUT, BRAKE, CW/CCW, S/S, GND3, LC⁻, LC⁺, E1, C1, GND2′, Rт, Cт, D.T.C, F.B.

Left side pins:
- HC⁻ 46
- HC⁺ 47
- Hb⁻ 48
- Hb⁺ 49
- GND3′ 50
- Ha⁻ 51
- Ha⁺ 52
- Vcc2 53
- La⁺ 54
- La⁻ 55
- Lb⁺ 56
- Lb⁻ 57
- Lb⁻′ 58
- TEST 59
- TEST′ 60

Right side pins:
- 30 NC
- 29 −IN1
- 28 +IN1
- 27 GND2
- 26 +IN2
- 25 −IN2
- 24 Vref
- 23 NC
- 22 O.C.
- 21 Vcc1
- 20 C2
- 19 E2
- 18 NC
- 17 LD′
- 16 LD

Bottom pins (left to right, 1–15): CPIN, CPOUT, VDD, GND1, $\overline{XT}$, XT, N1, VDD′, N2, FGIN, APC, AFC, RV, 20/27, R/S

NC : No−connection

⌈ : inner short

POWER DISSIPATION

$P_D - Ta$

P_D (W) vs Ta (°C)

www.DataSheet4U.com
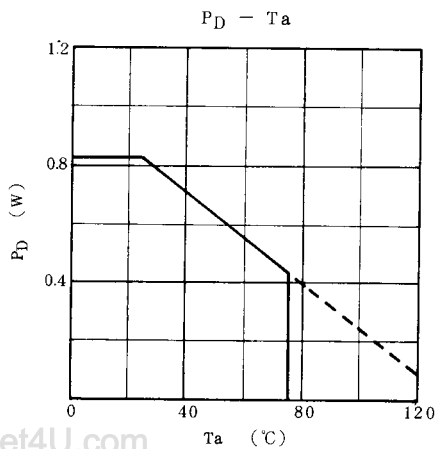
ELECTRICAL CHARACTERISTICS

PLL PART   (Unless otherwise specified, V_{DD}=5V, Ta=25°C)

CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage			V_{DD}	-		*	4.5	5.0	5.5	V
Operating Supply Current			I_{DD}	-	X'tal=8MHz CP_{IN}=CP_{OUT}	*	-	5.0	12.0	mA
Operating Frequency Range		X_T	f_{XT}	-		*	1.0	~	8.0	MHz
		CP_{IN}	f_{CP}	-	Square wave	*	0.05	~	4.0	
		FG_{IN}	f_{FG}	-	V_{IN}=0.5Vp-p Sine wave	*	-	~	10	kHz
Input Operating Voltage		FG_{IN}	V_{IN} FG	-	f_{FG}=10kHz Sine wave	*	0.5	~	V_{DD}-0.5	Vp-p
AFC, APC D/A Converter	Ladder Resistor		R_L	-			30	50	75	kΩ
	Max. Deviation				V_{DD}=4.5~5.5V		-	±2.5	±6.5	LSB
	Resolution			-			-	V_{DD}/256	-	V
	Temperature Drift						-	±1	-	LSB
Pullup Resistor			R_{IN}	-	N1,N2,20/27,R/S	*	10	30	50	kΩ
Input Voltage	"H" Level		V_{IH}	-	N1,N2,20/27,R/S CP_{IN}	*	V_{DD}×0.8	~	V_{DD}	
	"L" Level		V_{IL}				0	~	V_{DD}×0.2	
Input Leak Current			I_{IH}/I_{IL}	-	CP_{IN}	*	-	-	±1.0	μA
Output Current	"H" Level		I_{OH}	-	RV, LD CP_{OUT}	V_{OH}=4V	-0.5	-1.0	-	mA
	"L" Level		I_{OL}			V_{OL}=1V	0.5	1.0	-	
Amplifier Feedback Resistor		XT	R_f	-			100	200	400	kΩ
		FG_{IN}					300	500	800	

*: Guaranteed within the range of V_{DD}=4.5V~5.5V, Ta=-30~75°C.

PWM PART (V$_{CC1}$=15V, f=10kHz unless otherwise noted)

• REFERENCE SECTION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	V$_{ref}$	I$_{ref}$=1mA, Ta=25°C	4.75	5	5.25	V
Input Regulation	REG$_{IN}$	7V$\leq$V$_{CC1}\leq$I$_{ref}$=1mA, Ta=25°C		8	25	mV
Output Regulation	REG$_L$	1mA$\leq$I$_{ref}\leq$10mA, Ta=25°C		1	15	mV
Output Voltage Change with Temperature	V$_{ref}$/ T	−30°C$\leq$Ta$\leq$+75°C I$_{ref}$=1mA		0.01	0.03	%/°C
Short-circuit Output Current Note 2	I$_{short}$	V$_{ref}$=0		50		mA

• OSCILLATOR SECTION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Frequency	f$_{OSC}$	C$_T$=0.01µF, R$_T$=12k		10		kHz
Standard Deviation of Frequency Note 3		All values of V$_{CC}$, C$_T$, R$_T$, Ta constant		10		%
Frequency Change with Voltage		7V$\leq$V$_{CC1}\leq$40V, C$_T$=0.01µF Ta=25°C, R$_T$=12k		1		%
Frequency Change with Temperature		0°C$\leq$Ta$\leq$70°C, C$_T$=0.01µF, R$_T$=12k		1	2	%

• DEAD-TIME CONTROL SECTION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Bias Current		0$\leq$V$_I\leq$5.25V		−2	−10	µA
Maximum Duty Cycle, Each Output		V$_I$=0	45	49		%
Input Threshold Voltage		Zero Duty Cycle		3	3.3	V
		Maximum Duty Cycle	0			V

• PWM COMPARATOR SECTION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Threshold Voltage		Zero Duty Cycle		4	4.5	V
Input Sink Current		V$_{(pin 3)}$=0.7V	0.3	0.7		mA

• ERROR-AMPLIFIER SECTION

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage		V_{IO}	$V_{OAMP}=2.5V$		2	10	mV
Input Offset Current		I_{IO}	$V_{OAMP}=2.5V$		25	250	nA
Input Bias Current			$V_{OAMP}=2.5V$		0.2	1	μA
Common-mode Input Voltage Ragne	Low Level	V_{ICM}	$7V \leqq V_{CC1} \leqq 40V$	-0.3			V
	High Level			$V_{CC}-2$			
Open-loop Voltage Amplification		A_V	$V_{OAMP}=0.5V \sim 3.5V$, Ta=25°C	60	80		dB
Unity-gain Bandwidth			Ta=25°C	500	830		kHz
Common-mode Rejection Ratio		CMR	$V_{CC1}=40V$, Ta=25°C	65	80		dB
Output Sink Current			$V_{OAMP}=0.7V$	0.3	0.7		mA
Output Source Current			$V_{OAMP}=3.5V$	-2	-10		mA

• OUTPUT SECTION

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Collector Off-state Current		I_{CER}	$V_{CE}=40V$, $V_{CC}=40V$			100	A
Emitter Off-state Current			$V_{CC1}=V_C=40V$, $V_E=40V$			-100	A
Collector-emitter Saturation Voltage	Common-emitter	$V_{CE}(sat)$	$I_C=200mA$, $V_E=0V$		0.95	1.3	V
	Emitter follower	$V_{CE}(ON)$	$I_E=-200mA$, $V_C=15V$		1.6	2.5	V
Output Voltage Rise Time		t_{r1}	$V_{CC1}=15V$, $R_L=150$, Ta=25°C $I_C=100mA$, Common-emitter		100	200	ns
Output Voltage Fall Time		t_{f1}			70	200	ns
Output Voltage Rise Time		t_{r2}	$V_{CC1}=15V$, $R_L=150$, Ta=25°C $I_E=100mA$, Common-follower		100	200	ns
Output Voltage Fall Time		t_{f2}			70	200	ns

• SUPPLY CURRENT

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Standby Supply Current	$I_{CC}(SB)$	$V_{CC1}=15V$, All other inputs and outputs open		8	12.5	mA
Average Supply Current	$I_{CC}(BI)$	$V_{(pin 4)}=2V$		10		mA

Note 1: All typical values except for temperature coefficients are at Ta=25°C.

Note 2: Duration of the short-circuit should not exceed one second.

Note 3: Standard deviation is a measure of the statistical distribution about the mean as derived from the formula.

$$\sigma = \sqrt{\frac{\sum\limits_{n=1}^{N} (Xn - \overline{X})^2}{N-1}}$$

CONTROLLER PART (Unless otherwise specified, V_{CC2}=5V, Ta=25°C)

CHARACTERISTIC				SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Power Supply Voltage				V_{CC2} opr	–		4.75	5.00	5.25	V
Power Supply Current				I_{CC1}	–	Stop State	–	3.4	6.0	mA
				I_{CC2}		Output Open	–	17.0	26.0	
Saturation Voltage		Upper Side		$V_{SAT\ U-1}$	–	R_L=200Ω	–	1.3	2.0	V
				$V_{SAT\ U-2}$		R_L=2kΩ	–	1.0	1.3	
		Lower Side		$V_{SAT\ L-1}$		R_L=200Ω	–	0.8	1.2	
				$V_{SAT\ L-2}$		R_L=2kΩ	–	0.18	0.4	
Leak Current		Upper Side		$I_{L\ U}$	–		–	–	100	μA
		Lower Side		$I_{L\ L}$			–	–	100	
Position Sensing Input	Common Mode Voltage Range			CMR H	–		2.0	–	4.5	V
	Input Sensitivity			V_H			20	–	–	mV
	Input Hysteresis			V_{H-Hye}			2	7	15	
START Input. (RUN)	Operation Input Voltage	"H"	$V_{IN\ R(H)}$		–		4.0	–	–	V
		"L"	$V_{IN\ R(L)}$		–		–	–	1.0	
	Input Current	"L"	$I_{IN\ R}$		–	$V_{IN\ R}$=1.0V	–	–	200	μA
CW/CCW Input (FWD/REV)	Operation Input Voltage	"H"	$V_{IN\ C(H)}$		–		4.0	–	–	V
		"L"	$V_{IN\ C(L)}$		–		–	–	1.0	
	Input Current	"L"	$I_{IN\ C}$		–	$V_{IN\ C}$=1.0V	–	–	200	μA
BRAKE Input (BRAKE)	Operation Input Voltage	"H"	$V_{IN\ B(H)}$		–		4.0	–	–	V
		"L"	$V_{IN\ B(L)}$		–		–	–	1.0	
	Input Current	"L"	$I_{IN\ B}$		–	$V_{IN\ N}$=1.0V	–	–	200	μA
FG Output	Output Current	"H"	I_{FGH}		–		80	–	–	μA
	Output Voltage	"L"	V_{FGL}		–	I_{FG}=0.3mA	–	–	0.4	V
	Pulse Width		τ_{FG}		–	C=0.1μF, R=10kΩ	0.9	1.0	1.1	ms

TOSHIBA CORPORATION

TA8443F

PLL PART OPERATION

1. Crystal oscillation terminals (XT, $\overline{XT}$)

    - The crystal oscillator is used by connecting as shown below.
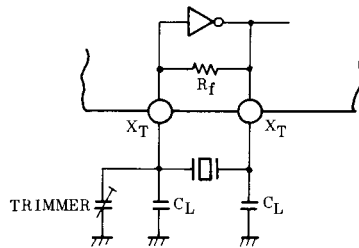
    - C_L of 10~30pF is appropriate.

    - Crystal oscillation frequency is calculated by the following equation according to number of FG pulses of a motor to be used.

    $$f_{\overline{X}} = \frac{R}{60} \times FG' \times 128 \times (20 \text{ or } 27) \times N \quad (Hz)$$

    (Note) (20 or 27): 20 at 20/27="H" or Open.
                                   27 at 20/27="L".

    f_X: Crystal oscillation frequency, FG': number of FG pulse generated per revolution of motor, R: revolution of motor per minute, N: Ratio of frequency division of the crystal reference frequency divider.

    (Refer to Item 9.)

    - Maximum operating frequency is above 8MHz and crystals up to 8MHz can be used.

2. Reference frequency input/output terminals (CP$_{IN}$, CP$_{OUT}$)

    - Divided output $\frac{f_X}{N}$ from the crystal reference frequency divider is available at CP$_{OUT}$, which is normally connected CP$_{IN}$.

    - When an external oscillator (CR oscillator, etc.) is connected to CP$_{IN}$, motor speed can be finally adjusted.

3. FG pulse input terminal (FG_{IN})

   - This is the input terminal of FG pulse that shows the motor speed.
     This FG pulse becomes comparision frequency.

   - This terminal has built-in Amplifier and Schmitt circuit.
     FG pulses are applied through capacitor coupling and small amplitude is enough
     for proper operation.

4. Lock range switching terminal (20/27)

   - This terminal is for switching rock range of motor, with a pull-up resistor and
     chattering preventive circuit.

   (TRUTH TABLE)

20/27	DIVIDED FREQUENCY	LOCK RANGE
L	1/27	+3.4~-3.9% of reference cycle
H or NC	1/20	+4.6~-5.3% of reference cycle

5. APC, AFC output terminal (APC, AFC)

   - AFC (speed control output) is a F-V converter for FG frequency, and is con-
     sisting of a 8 bit D/A converter.

   - APC (phase control output) is a phase comparator (ϕ-V converter) that compares
     phase difference ϕ between 1/2 FG and reference frequency FS', and is also
     consisting of a 8 bit D/A converter.

   - Both APC and AFC perform the following 3 operations according to FG_{IN} frequency.

     a. When FG_{IN} frequency is within the lock range:
         Both APC and AFC perform the normal operation for FG_{IN}.

     b. When FG_{IN} frequency is below the lock range (under speed):
         APC and AFC outputs are both fixed at "H" level.

     c. When FG_{IN} frequency is above the lock range (over speed):
         APC and AFC outputs are both fixed at "L" level.

   - When a motor is in STOP state (P/S=H or NC), both AFC and APC are fixed "L"
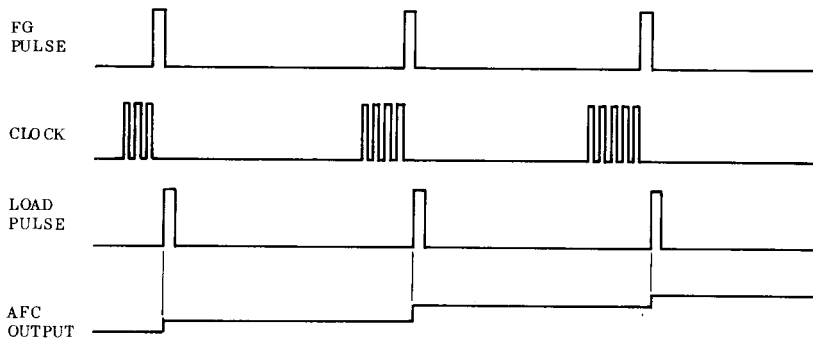   level.

AFC Output change status for FG_{IN} frequency
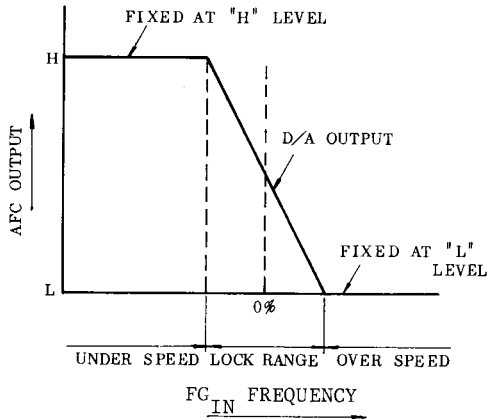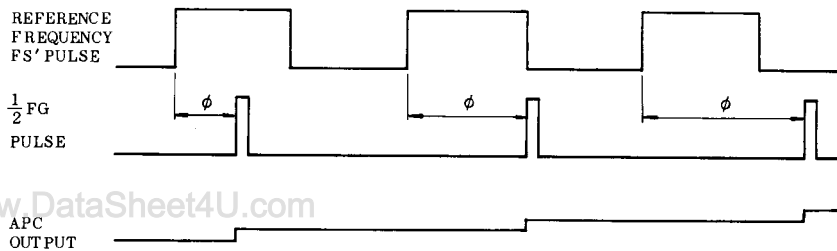
APC Output change status for phase difference ϕ

AFC OUTPUT

FIXED AT "H" LEVEL

H

D/A OUTPUT

FIXED AT "L" LEVEL

L

0%

UNDER SPEED | LOCK RANGE | OVER SPEED

FG_{IN} FREQUENCY

APC OUTPUT WITHIN LOCK RANGE

H

D/A OUTPUT

L

0   π 2π

PHASE DIFFERENCE ϕ
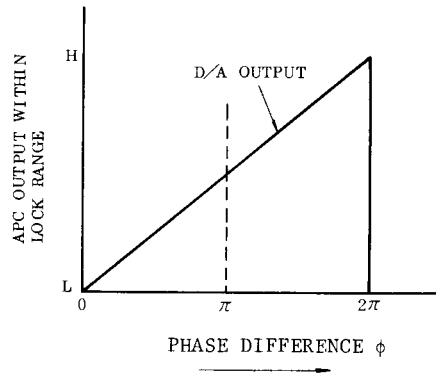
- AFC and APC timing chart within lock range.

    a. AFC (SPEED CONTROL SYSTEM)

FG PULSE

CLOCK

LOAD PULSE

AFC OUTPUT

    b. APC (PHASE CONTROL SYSTEM)

REFERENCE FREQUENCY FS' PULSE

$\frac{1}{2}$ FG PULSE

ϕ ϕ ϕ

APC OUTPUT

6. Lock detecting terminal (LD)

   - This terminal is the lock detecting output and is placed at "H" level when FG_{IN} frequency is within the lock range and otherwise, placed at "L" level.

7. RUN/STOP input terminal (R/S)

   - RUN/STOP signals of the motor are input to this terminal.

   - This terminal has a pull-up resistor and a chattering preventive circuit.

   - During RUN (R/S=L), AFC, APC and LD perform the above-mentioned operations for FG_{IN} frequency, and during STOP (R/S=H or NC), AFC, APC and LD are all fixed at "L" level.

8. Reverse signal output terminal (RV)

   - At the switching of lock range from 1/20 to 1/27 or the operating from RUN to STOP, reverse signal for braking the motor is output through this terminal.

   - Change of RV output status

PREVIOUS STATUS	RV OUTPUT CHANGE TO "H" LEVEL	RV OUTPUT CHANGE TO "L" LEVEL
During normal rotation (during lock) at 1/20.	When the lock range is switched from 1/20 to 1/27.	When the motor speed is locked at 1/27, or when FG_{IN} 1/8FS, or when the lock range is switched from 1/27 to 1/20.
During normal rotation (during lock) at 1/20 or 1/27.	When the operation is switched from RUN to STOP.	When FG_{IN} 1/8FS or when the operation is switched from STOP to RUN.

   - In other cases than above, RV output is not changed and fixed at "L" level.

   - Further, if FG frequency rises up to 1.5 times of normal rotation at 1/20 (2 times of normal rotation at 1/27), RV output is reset.

9. Reference divided frequency switching terminal (N1, N2)

- Divided frequency 1/N of the crystal reference frequency divider can be switched to 1/5, 1/6 or 1/12 by number of FG pulses or a crystal used.

- This terminal has a built-in pull-up resistor.

(TRUTH TABLE)

N1	N2	1/N
H	H	1/5
L	H	1/6
H	L	1/12

1/N: CRYSTAL REFERENCE DIVIDED FREQUENCY

(Note) Don't use mode, N1=N2="L", because this mode is test mode.

CAUTION IN APPLICATION

- APC and AFC terminals are for the 8-bit D/A converter outputs, which are directly output from the R-2R ladder type resistor network as shown in the following diagram. Impedance of these outputs becomes equal to the ladder resistor value R_L. Therefore, input impedance at the receiving side of these terminals shall be designed accordingly.

$$R_L = 30 \sim 75k\Omega \ (TYP \ 50k\Omega)$$
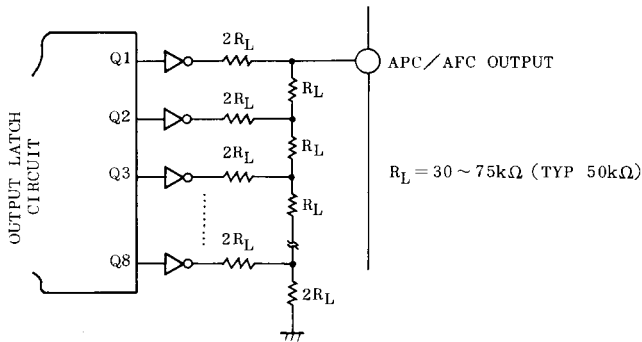
- A filter for an externally mounted differential amplifier on an application circuit shall be selected to meet the response characteristic of a motor to be used.
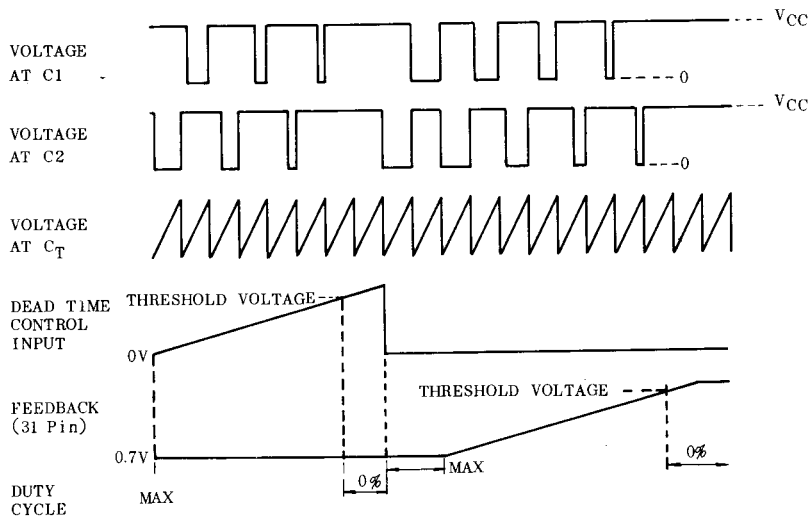
PWM PART OPERATION

The uncommitted output transistors provide either common-emitter or emitter-follower output capability.

Push-pull or single-ended output operation may be selected through the output-control function.

The architecture of the TA8443F prohibits the possibility of either output being pulsed twice during push-pull operation.
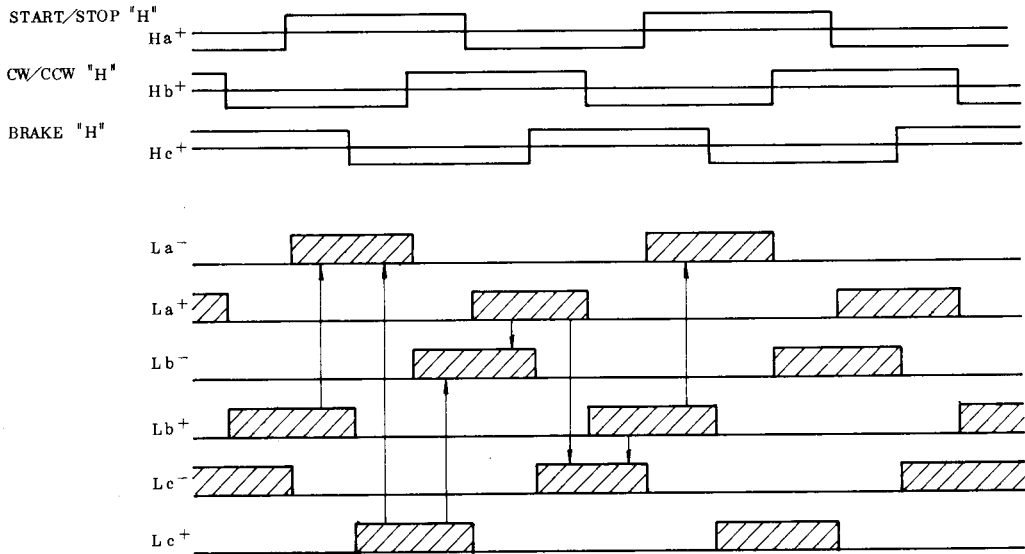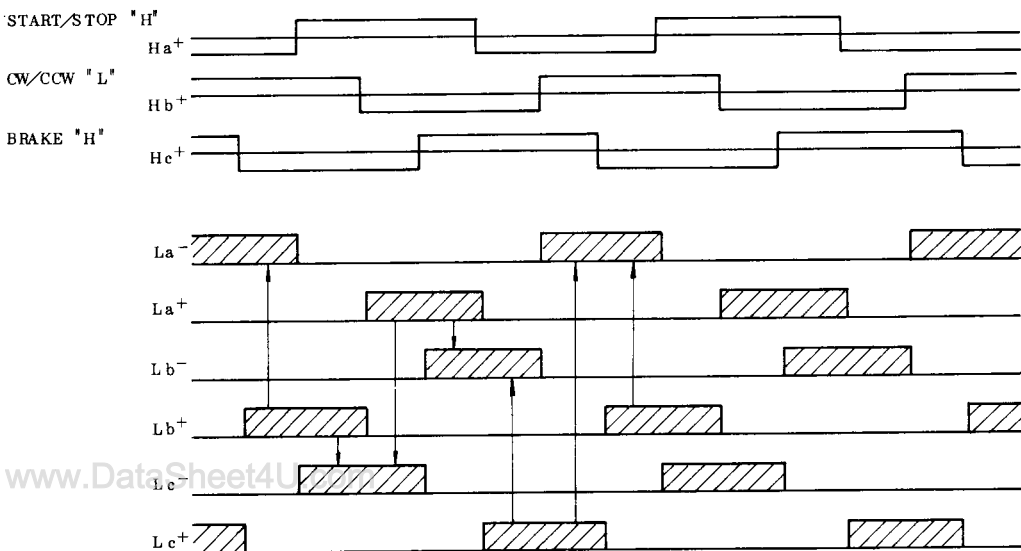
VOLTAGE WAVEFORMS

VOLTAGE AT C1

VOLTAGE AT C2

VOLTAGE AT C_T

DEAD TIME CONTROL INPUT

FEEDBACK (31 Pin)

DUTY CYCLE

TA8443F

CONTROLLER PART OPERATION

1. TIMING CHART

FORWARD ROTATION (Position sensing signal advances Ha → Hb → Hc.)

START/STOP "H" Ha+

CW/CCW "H" Hb+

BRAKE "H" Hc+

La−

La+

Lb−

Lb+

Lc−

Lc+

REVERSE ROTATION (Position sensing signal advances Ha → Hc → Hb.)

START/STOP "H" Ha+

CW/CCW "L" Hb+

BRAKE "H" Hc+

La−

La+

Lb−

Lb+

Lc−

Lc+

TOSHIBA CORPORATION

2. APPLICATION OF CONTROLLER PART

Like a video disk player, TA8443P is provided with the stopping function which in a short time, stops the motor having a large inertia, and makes the quick disk-change possible. To make the frequency generator (FG) unnecessary which was formerly required for fetching the rotation signal, the signal from the position sensing input is ORed and is output to FG output pin (44 pin). Therefore, for FG output, three position sensing outputs (Ha, Hb, Hc) are ORed, and the rotation speed signal of the frequency of six times that of one output can be fetched resulting in making it possible to obtain a sufficient controlling characteristic with the F/V (Frequency-Voltage) conversion method of mono-stable type.

(1) Operation of FG Output (44 pin) and T_{FG} (45 pin)

In Fig. 1, Q1 and Q3 are the mono-stable mulit-vibrator to which gate (Q2 base) the signal from each position sensing input of Ha, Hb and Hc is input after ORed and shaped in waveform by FE. The pulse width of MMV made by Q1 and Q2 is determined by R2 and C2 to be connected to TFG (45 pin), and the square wave having the pulse width to be determined by C2 and R2 is output. Of course, this frequency is proportional to the rotation signal and this frequency is six times the frequency of each position sensing. (6 per 1 electrical rotation) F/V conversion operation is made through connecting FG_0 output to LPF for integration. However, if R2 is made variable, the conversion gain can be controlled.
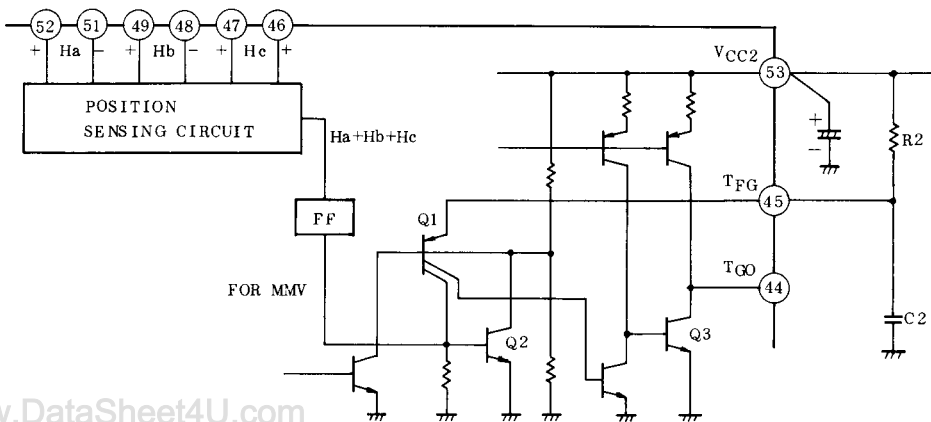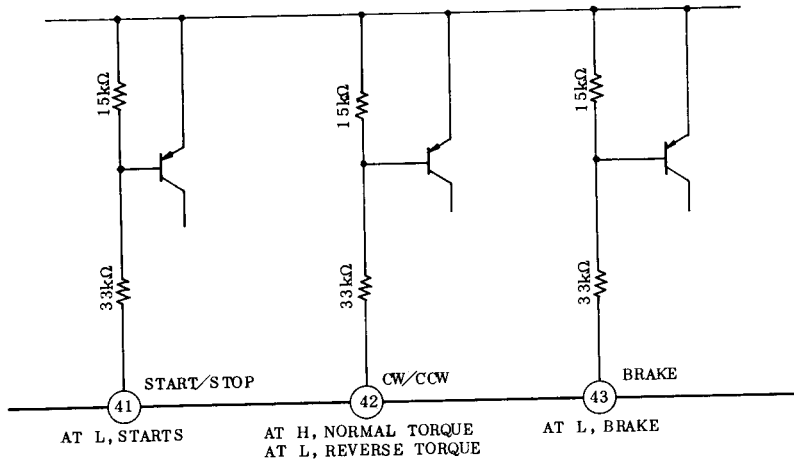

Fig. 1

(2) Each Control Input

START/STOP   CW/CCW   BRAKE

41   42   43

AT L, STARTS   AT H, NORMAL TORQUE   AT L, BRAKE
              AT L, REVERSE TORQUE

Fig. 2

START/STOP	CW/CCW	BRAKE	OUTPUT
H	H	H	Normal torque mode
H	L	H	Reverse torque mode
H/L	H/L	L	BRAKE mode
L	H/L	H	STOP mode

Note: In STOP mode, ③⑧ , ③⑨ , ⑤④ , ⑤⑤ , ⑤⑥ and ⑤⑦ pins of output are all made OFF. In BRAKE mode, ③⑨ , ⑤⑤ and ⑤⑦ pins of output are made ON. (sweep-out mode)

(3) Output Circuit

As shown in the block diagram, in the output circuit, the Darlington emitters of PNP and NPN are provided on the upper side, and the lower side is made as the open collector of NPN.

Connect the external transistor in the same manner as that of the application circuit.

CHARACTERISTIC DATA OF PLL PART

$f_{MAX}(X_T) - V_{DD}$

$f_{MAX}(X_T) - Ta$

$f_{MAX}(CP_{IN}) - V_{DD}$

$f_{MAX}(CP_{IN}) - Ta$

$I_{DD} - V_{DD}$

$V_{IN}(FG_{IN}) - V_{DD}$

TOSHIBA CORPORATION

TA8443F

APPLICATION CIRCUIT