SUMMIT MICROELECTRONICS, Inc.

SMP9410

Preliminary Information [1] *see last page*

Quad 10-Bit Nonvolatile DACPOT™

FEATURES

- **Four Programmable 10-Bit Nonvolatile DACs**
  - **INL ±1LSB, DNL ±1LSB, 1024 Steps Each**
- **Power on Recall at any Value**
- **Parallel or Independent Operation of DACs**
- **Excellent Temperature Stability - ±15ppm/°C**
  - **Industrial Temperature range**
- **1.25V Precision Voltage Reference**
- **I²C Serial Bus Interface**
- **Very Small QFN package • 5mm square**

APPLICATIONS

- **Laser bias/modulation current adjustment**
- **Power supply trimming/margining**
- **Potentiometer replacement**

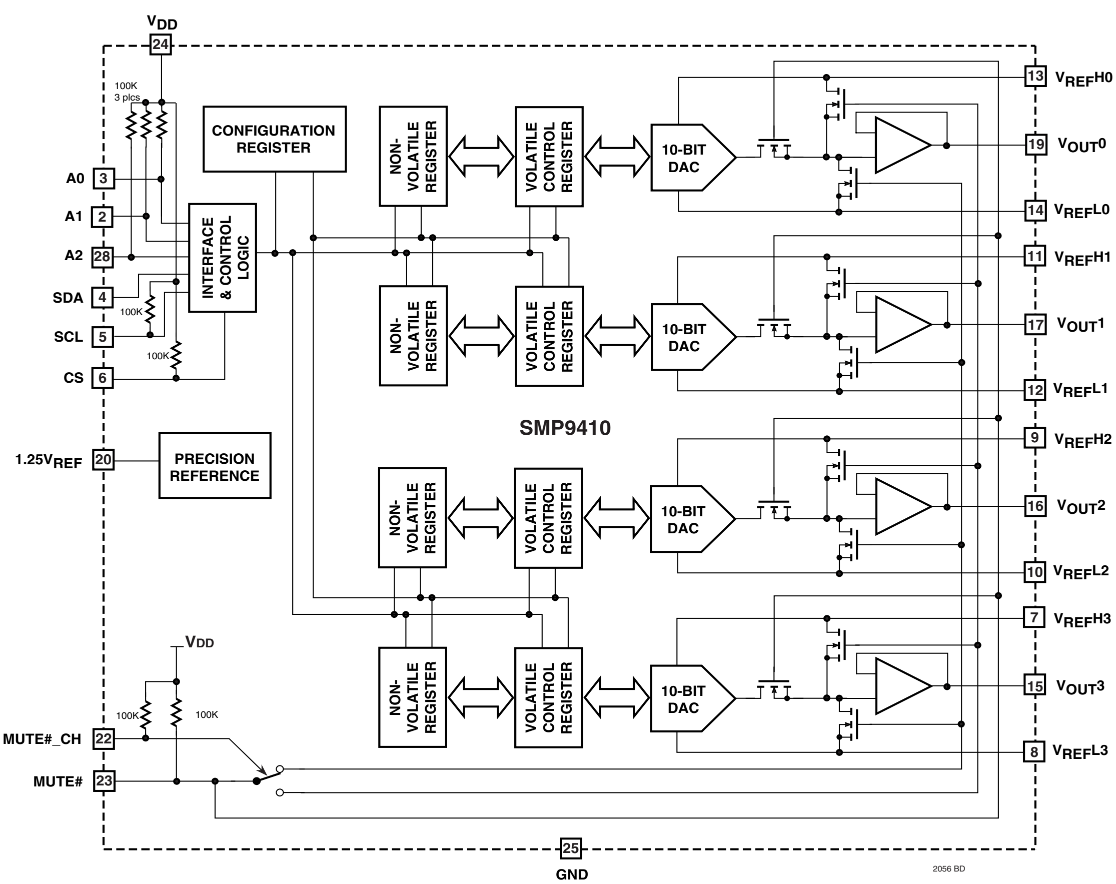
INTRODUCTION

The SMP9410 is a quad 10 bit (1024 steps) Non Volatile D-to- A converter or DACPOT™. The device will recall any analog voltage on power up, making it ideal for high accuracy and temperature stable calibration purposes and can operate from a single +2.7V to +5.5V supply. Internal precision buffers swing rail-to-rail with an input voltage range from ground to the positive supply.

The part integrates four 10-bit DACs and associated circuits: an enhanced unity gain operational amplifier output, a 10-bit volatile data latch, a 10-bit nonvolatile data register, and I²C bus industry standard 2-wire serial interface. The SMP9410 is available in a very small 5mm square Quad Flat package with No leads (QFN) for small form factor designs.

Programming of configuration, control and calibration values by the user can be simplified with the interface adapter and Windows GUI software obtainable from Summit Microelectronics.

FUNCTIONAL BLOCK DIAGRAM



Note: Pin numbers are for the QFN.

DEVICE OPERATION

INTRODUCTION

The device has four 10-Bit digital to analog converters that are comprised of a resistor network that converts a digital input into an equivalent analog output voltage in proportion to the applied reference voltages. The voltage differential between each $V_{REF}L$ and $V_{REF}H$ input pair sets the range and full-scale output voltage for their respective DAC.

Each DAC has a 10-Bit nonvolatile register that can hold a 'set-and-forget' value that can be recalled whenever the device is powered-on.

Each DAC has a 10-Bit volatile register that holds the current digital value. The register can be set to any value by the serial interface; commanded to load the zero scale value, full scale value or mid-scale value; or can recall a preset value stored in a nonvolatile register.

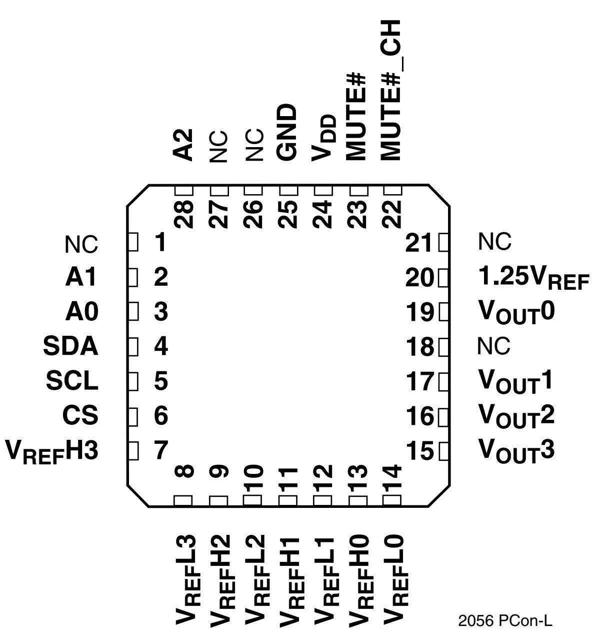
The device also has a nonvolatile configuration register that is accessible over the 2-wire bus. The configuration register is used to select the device type identifier and the DAC power-on state.

The device uses the industry standard I^2C 2-wire serial protocol. The bus is designed for two-way, two-line serial communication between different integrated circuits. The two lines are the SCL (serial clock) and SDA (serial data). Both lines should be pulled up to the positive supply through a resistor. The protocol defines devices as being either Masters or Slaves. The SMP9410 will always be a Slave because it does not initiate any communications or provide a clock output.

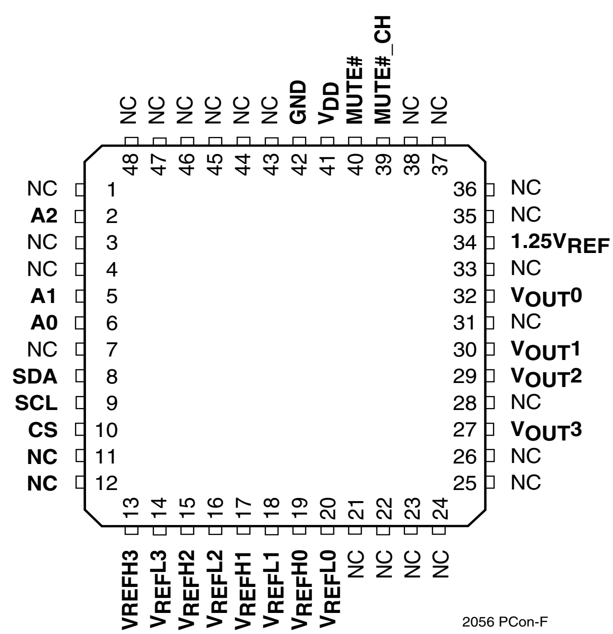
PIN CONFIGURATION

TOP VIEW

QFN



TQFP



PIN DESCRIPTIONS

Pin #	Type	Pin Name	Pin Description Note: Pin numbers are from LPCC.
1,18,21,26,27	NC	NC	No Connect. NC pins are not connected
3,2,28	I	A0, A1, A2	The address inputs for the serial interface logic. Setting them high or low will determine the device's bus address that is contained within the serial bus data stream. These pins have internal 100KΩ pull-up resistors to V_{DD}
4	I/O	SDA	The bidirectional pin used to transfer data in and out of the device.
5	I	SCL	The serial interface clock. It is used to clock the data in and out. This pin has an internal 100KΩ pull-up resistor to V_{DD}
6	I	CS	Chip Select input (VIH = selected) This pin has an internal 100KKΩ pull-up resistor to V_{DD}
13,11,9,7	I	V_{REF}H0, V_{REF}H1, V_{REF}H2, V_{REF}H3	The higher of the voltage reference inputs. V_{REF}H must be equal to or less than V_{DD} and greater than V_{REF}L.
14,12,10, 8	I	V_{REF}L0, V_{REF}L1, V_{REF}L2, V_{REF}L3	The lower of the voltage reference inputs. V_{REF}L must be equal to or greater than ground and less than V_{REF}H.
19,17,15,16	O	V_{OUT}0, V_{OUT}1, V_{OUT}2, V_{OUT}3	The voltage output of the DACs. It is buffered by a unity-gain follower that can slew up to 1V/µs.
20	O	1.25V_{REF}	A 1.25V output reference voltage.
22	I	MUTE#_CH	The MUTE#_CHoice input sets the V_{OUT} levels when MUTE# is asserted low (MUTE_CH# high = V_{REF}H, MUTE_CH# low = V_{REF}L). This pin has an internal 100KΩ pull-up resistor to V_{DD}
23	I	MUTE#	Forces the VOUT levels to be equal to either the VREFH or VREFL level, according to the value of MUTE#_CH (VIL = mute). This pin has an internal 100KΩ pull-up resistor to V_{DD}
24	PWR	V_{DD}	Power supply input.
25	PWR	GND	Power supply return.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... –55°C to 125°C
Storage Temperature .... –65°C to 150°C
Terminal Voltage with Respect to GND:
V_{DD} .... –0.3V to 6.0V
All Others .... –0.3V to 6.0V
Output Short Circuit Current…………………..……….100mA
Lead Solder Temperature (10 secs)....................300 °C
Junction Temperature.......................................150°C
ESD Rating per JEDEC……………………..………..2000V
Latch-Up testing per JEDEC……………..…......+/- 100mA

Note * - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature .... –40°C to 85°C
Voltage .... 2.7V to 5.5V

Package Thermal Resistance

θ_{JA} 48 Pin TQFP = 80°C/W, 28 Pin QFN= 80°C/W
θ_{JC} 48 Pin TQFP = 40°C/W, 28 Pin QFN= 32°C/W
Moisture Classification Level 1 (MSL 1) per J-STD- 020

RELIABILITY CHARACTERISTICS

Data Retention……………………..……..…..100 Years
Endurance……………………..……….100,000 Cycles

DC OPERATING CHARACTERISTICS

(Over Recommended Operating Conditions; Voltages are relative to GND)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Power						
I_{DD}	Power supply current	NV write V_{DD} = 5.5V			3	mA
		NV write V_{DD} = 2.7V			3	mA
	Standby or quiescent	V_{DD} = 5.5V; Excluding current through DACs			1	mA
		V_{DD} = 2.7V; Excluding current through DACs			1	mA
	Power down	V_{DD} = 5.5V; Total current including DACs			1	mA
		V_{DD} = 2.7V; Total current including DACs			1	mA
V_{DD}	Supply voltage		2.7		5.5	V
V_{IH}	SDA, SCL, CS, MUTE#, MUTE#_CH, A0, A1, A2		$0.7 \times V_{DD}$			V
V_{IL}					$0.3 \times V_{DD}$	V
V_{OL}	SDA	I_{OL} = 3mA			0.4	V
I_{LI}	Input leakage	V_{IN} = 0 to V_{DD}		100		µA
I_{LO}	Output leakage	V_{OUT} powered down in high impedance mode			10	µA
W_{END}	Write endurance	Number of NV store operations	1×10^6			NV stores
t_{DR}	Data retention	NV data retention	100			Years

2056 Elect TableA

DC OPERATING CHARACTERISTICS (CONTINUED)

(**Over Recommended Operating Conditions; Voltages are relative to GND**)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Static Performance						
N	Resolution		10			Bits
INL	Relative Accuracy	$V_{REF}H = 5V, V_{REF}L = 0V$	–2	±1	2	LSB
DNL	Differential nonlinearity	$V_{REF}H = 5V, V_{REF}L = 0V$ Guaranteed monotonic	–1	±0.5	1	LSB
VZSE	Zero scale error	Data = 000_{HEX}	0		15	mV
VFS	Full scale voltage	Data = $3FF_{HEX}$			$V_{REF}H$ –1LSB	V
TCV	Full scale temperature coefficient			±15		ppm
	Offset error		–0.2		+0.2	%VFS
	Gain error		–0.5		+0.5	%
Matching Performance						
	Linearity matching error			±1		LSB
Analog Output						
I_{OUT}	Output current@Half Scale	Data = 200_{HEX}, ΔV_{OUT} = ±3LSB, $V_{REF}H_X=V_{DD}=5V$	-0.25		+0.25	mA
LDREG	Load regulation @ halfscale	Data = 200_{HEX}, RL = 1kΩ to ∞		1	3	LSB
C_L	Capacitive load	No oscillation		500		pF
Dynamic Characteristics						
BW	–3dB bandwidth	R = 10kΩ		100		kHz
THD	Total harmonic distortion	VA = $1V_{RMS}$, f = 1kHz		0.08		%
	Channel-to-channel isolation	f = 1kHz, V_{IN} = $100mV_{PP}$ on $V_{REF}H$		–60		dB
	Digital cross-talk			–60		dB
Reference Voltages						
$V_{REF}H$		$V_{REF}H > V_{REF}L$			V_{DD}	V
$V_{REF}L$		$V_{REF}L < V_{REF}H$	GND			V
$1.25V_{REF}$			1.2	1.25	1.3	V

2056 Elect TableB

AC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions**)

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time (1)	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.3	3.5	µs
t_{DH}	Data Out hold time	SCL low (cycle n+1) to SDA change	0.3		µs
t_R	SCL and SDA rise time (1)			1000	ns
t_F	SCL and SDA fall time (1)			300	ns
$t_{SU:DAT}$	Data In setup time		250		ns
$t_{HD:DAT}$	Data In hold time		0		ns
TI	Noise filter SCL and SDA (1)	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

Note (1) These values are guaranteed by design. Refer to the timing diagram in Figure 4.

2056 Table01

Table 1. Data/Clock Timing

DEVELOPMENT HARDWARE & SOFTWARE

PROGRAMMING CONNECTION

The end user can obtain the Summit SMX3200 programming system for device prototype development. The SMX3200 system consists of a programming Dongle, cable and Windows GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 is available from the website (www.summitmicro.com).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus. The Windows GUI software will generate the data and send it in I2C serial bus format so that it can be directly downloaded to the SMP9410 via the programming Dongle and cable. An example of the connection interface is shown in Figure 1. When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval.

Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

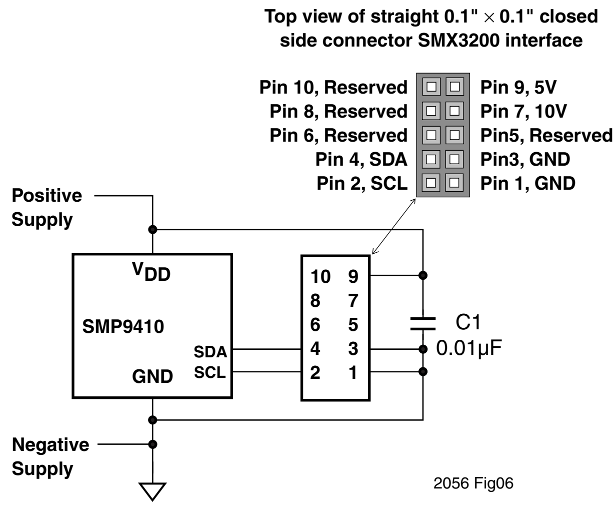


Figure 1. SMX3200 Programmer connections for the SMP9410.

APPLICATIONS INFORMATION

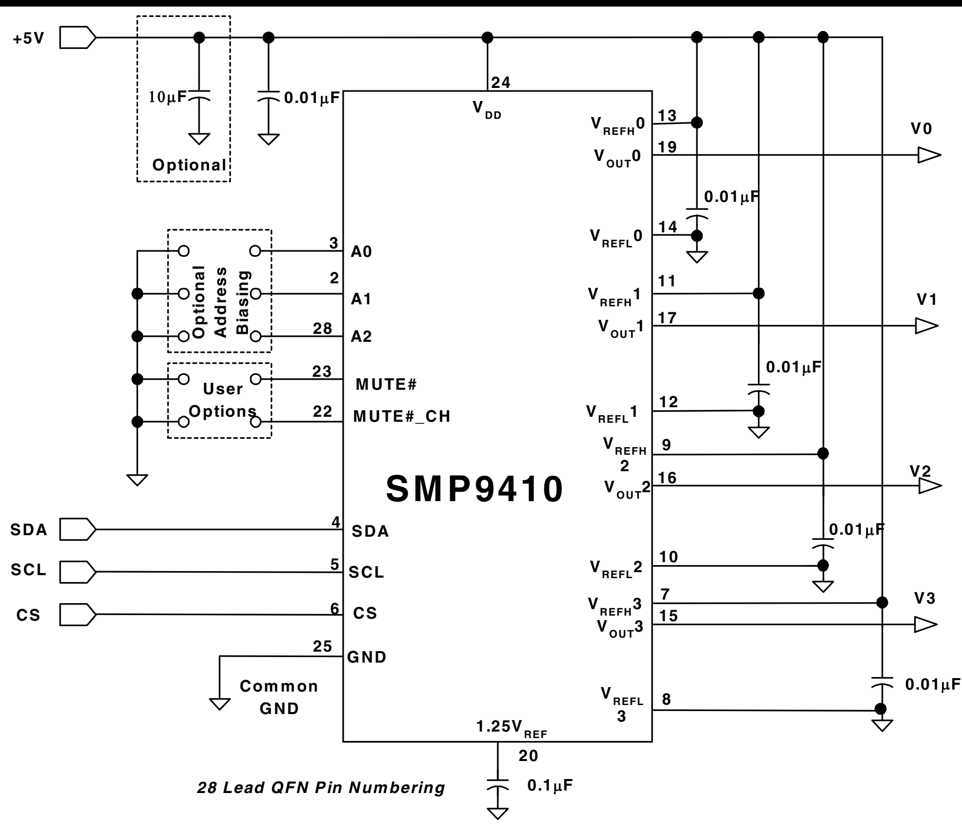


Figure 2. Applications Schematic. Additional bypass capacitors may be needed in noisy environments. The V_{REF}H and V_{REF}L pins can be tied to V_{DD} or GND or as specified in the pin descriptions. For optimum performance, all capacitors should be placed as close as possible to the SMP9410 Pins

APPLICATIONS INFORMATION (CONTINUED)

ACCESSING THE DACS

Data transfers are initiated when a Master issues a Start condition, which is a high to low transition on SDA while SCL is high (see Figure 3). The Start is immediately followed by an eight bit transmission: bits 7 through 1 comprise the device type identifier and device bus address; bit 0 is the Read/Write bit indicating the action to follow. If the intended device receives the byte and recognizes its address it will return an Acknowledge during the 9th clock cycle. Some data transfers will be concluded with a Stop condition, which is a low to high transition on SDA while SCL is high. Note: a Stop condition must be performed for all nonvolatile Write operations. Timing for all I^{2}C operations are summarized in Figure 4 and Table 1.

The default device type identifier for addressing DACs is 0101_{BIN}. In order to accommodate more than eight devices on a single bus the device type identifier can be modified by the end user by writing to the configuration registers. (See Table 2). A0, A1 and A2 are the address inputs. When addressing the nonvolatile or configuration registers, theaddress inputs distinguish which one of eight possible devices sharing the common bus is being addressed. Setting them high or low will determine the device's bus address that is contained within the serial bus data stream.

Command Structure

The command structure is illustrated in Table 2. Of special note is the ability to write individually to any of the four DACs, or to all of them. The first five commands are three bytes in length and can either be volatile or nonvolatile DAC writes.

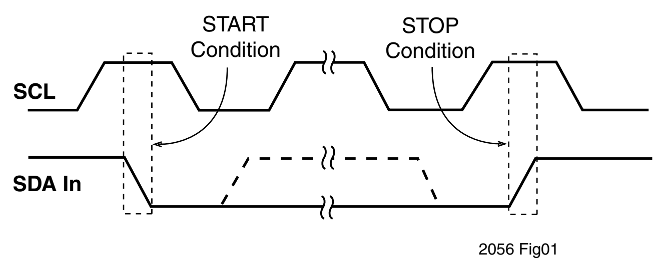


Figure 3. START and STOP Timing

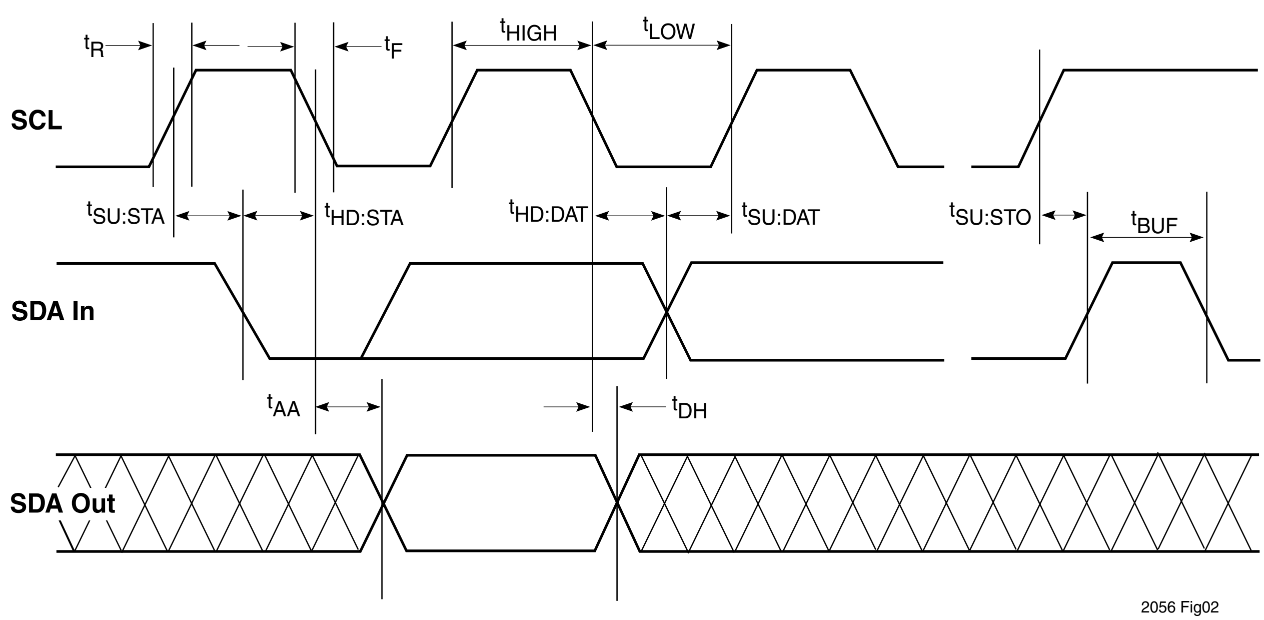


Figure 4. I^{2}C Data/Clock Timing

APPLICATIONS INFORMATION (CONTINUED)

ACK and NACK

A device that is receiving data will respond with an Acknowledge by pulling the SDA line low (ACK) after each byte is transmitted. The transmitting device will recognize this and continue to transmit. When the Master has received the data it expects it will hold the SDA line high (NACK) and the transmitting device will end transmission.

Sequence

The sequence is to issue a Start, followed by the device type and bus address with the Read/Write bit set to zero. The device will respond with an Acknowledge and the Master will then issue the command and follow-on data. In Figure 5 the Write is to DAC1 where the command = 1001_{BIN}; D9 and D8 are the MSBs of the DAC value being written. The device will then respond with an Acknowledge followed by the Master writing the last eight bits. If no Stop is generated after the device Acknowledge the Write is only to the register. If the device Acknowledge is followed by a Stop the data is written to both the DAC register and to the nonvolatile register.

Reading the Device

Reading the DACs requires setting the R/W bit to one. Then the host supplies clocks and the device will output data as shown in Figure 6.

Configuration Register

The SMP9410 can be configured by the end user or by Summit prior to shipment (see Programming Information). Reading the configuration register can also be performed if it has not already been locked. See Figure 7. There is one configuration register and it is accessed through the serial interface using 1001_{BIN} as the device type address, consequently the DAC address should never be set to 1001_{BIN}. The register is shown in Table 3.

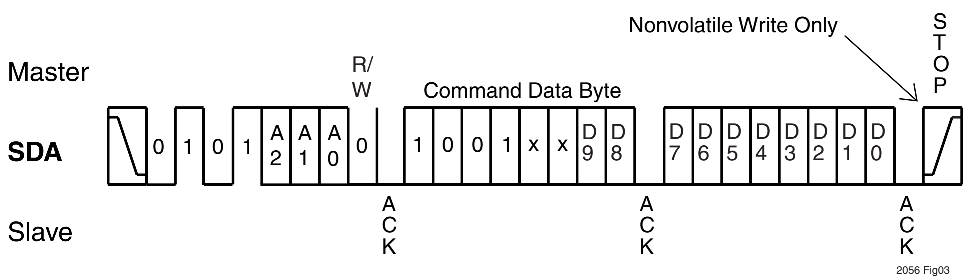


Figure 5. DAC1 Write Operation (see Table 2)

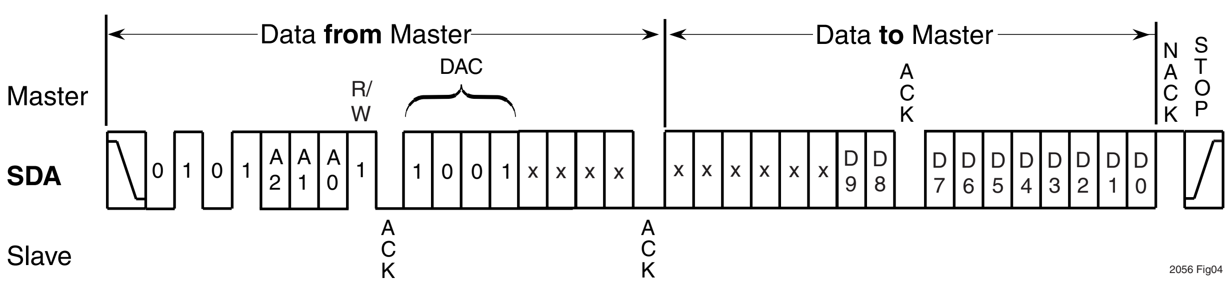


Figure 6. Read DACs

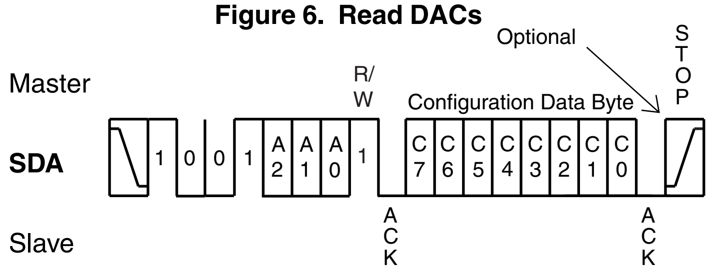


Figure 7. Configuration Register (see Table 3)

APPLICATIONS INFORMATION (CONTINUED)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	Command	Function
1	0	0	0	x	x	D9	D8	Write DAC0	Volatile with no stop, nonvolatile with stop
1	0	0	1	x	x	D9	D8	Write DAC1	
1	0	1	0	x	x	D9	D8	Write DAC2	
1	0	1	1	x	x	D9	D8	Write DAC3	
1	1	1	0	x	x	D9	D8	Write all DACs	
1	1	1	1	x	0	0	0	Recall E^2 to DAC0	Recall E^2 to DACs
1	1	1	1	x	0	0	1	Recall E^2 to DAC1	
1	1	1	1	x	0	1	0	Recall E^2 to DAC2	
1	1	1	1	x	0	1	1	Recall E^2 to DAC3	
1	1	1	1	x	1	x	x	Recall E^2 to all DACs	
1	1	0	1	x	0	0	0	PD DAC0	Power down DACs (see Table 3)
1	1	0	1	x	0	0	1	PD DAC1	
1	1	0	1	x	0	1	0	PD DAC2	
1	1	0	1	x	0	1	1	PD DAC3	
1	1	0	1	x	1	x	x	PD all DACs	
1	1	0	0	x	x	x	x	PU all DACs	Power up all DACs

2056Table02

Table 2. Command Structure

<table>
<tr><th>MSB C7</th><th>C6</th><th>C5</th><th>C4</th><th>C3</th><th>C2</th><th>C1</th><th>LSB C0</th><th>Function</th></tr>
<tr><td rowspan="8">x</td><td rowspan="8">x</td><td rowspan="8">x</td><td rowspan="8">x</td><td rowspan="6">x</td><td>x</td><td>x</td><td>0</td><td>Configuration register accessible</td></tr>
<tr><td>x</td><td>x</td><td>1</td><td>Configuration register locked</td></tr>
<tr><td>0</td><td>0</td><td rowspan="7">x</td><td>Power on recall: DACs set to all 0s</td></tr>
<tr><td>0</td><td>1</td><td>Power on recall: DACs set to all 1s</td></tr>
<tr><td>1</td><td>0</td><td>Power on recall: DACs set to mid scale</td></tr>
<tr><td>1</td><td>1</td><td>Power on recall: DACs set to NV register</td></tr>
<tr><td>0</td><td rowspan="3">x</td><td rowspan="3">x</td><td>At power down V_{OUT} = low impedance</td></tr>
<tr><td>1</td><td>At power down V_{OUT} = high impedance</td></tr>
<tr><td>PDA3*</td><td>PDA2*</td><td>PDA1*</td><td>PDA0*</td><td>x</td><td>Programmable Device Type Identifier for DAC addressing</td></tr>
</table>

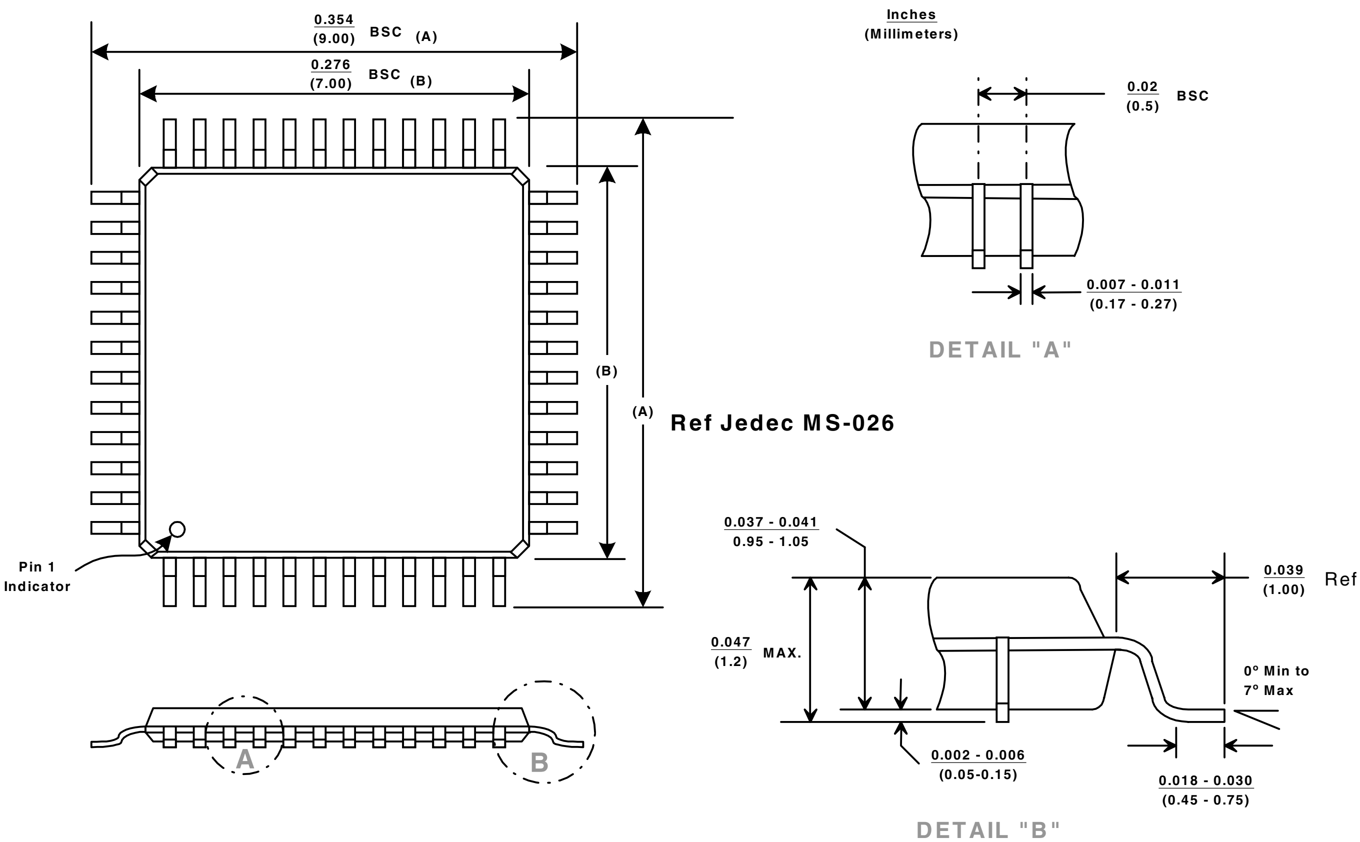
2056Table03

* Note: Never set the Programmable Device Type Identifier for DAC addressing to 1001_{BIN}. The Slave address for the configuration register is 1001_{BIN}, and a collision will occur on the I²C bus. Note: All parts are normally shipped with the Configuration Register locked with setting 5Fh (01011111). Unlocked user configurable parts are available on a special order basis. Contact Summit.

Table 3. Configuration Register

PACKAGES

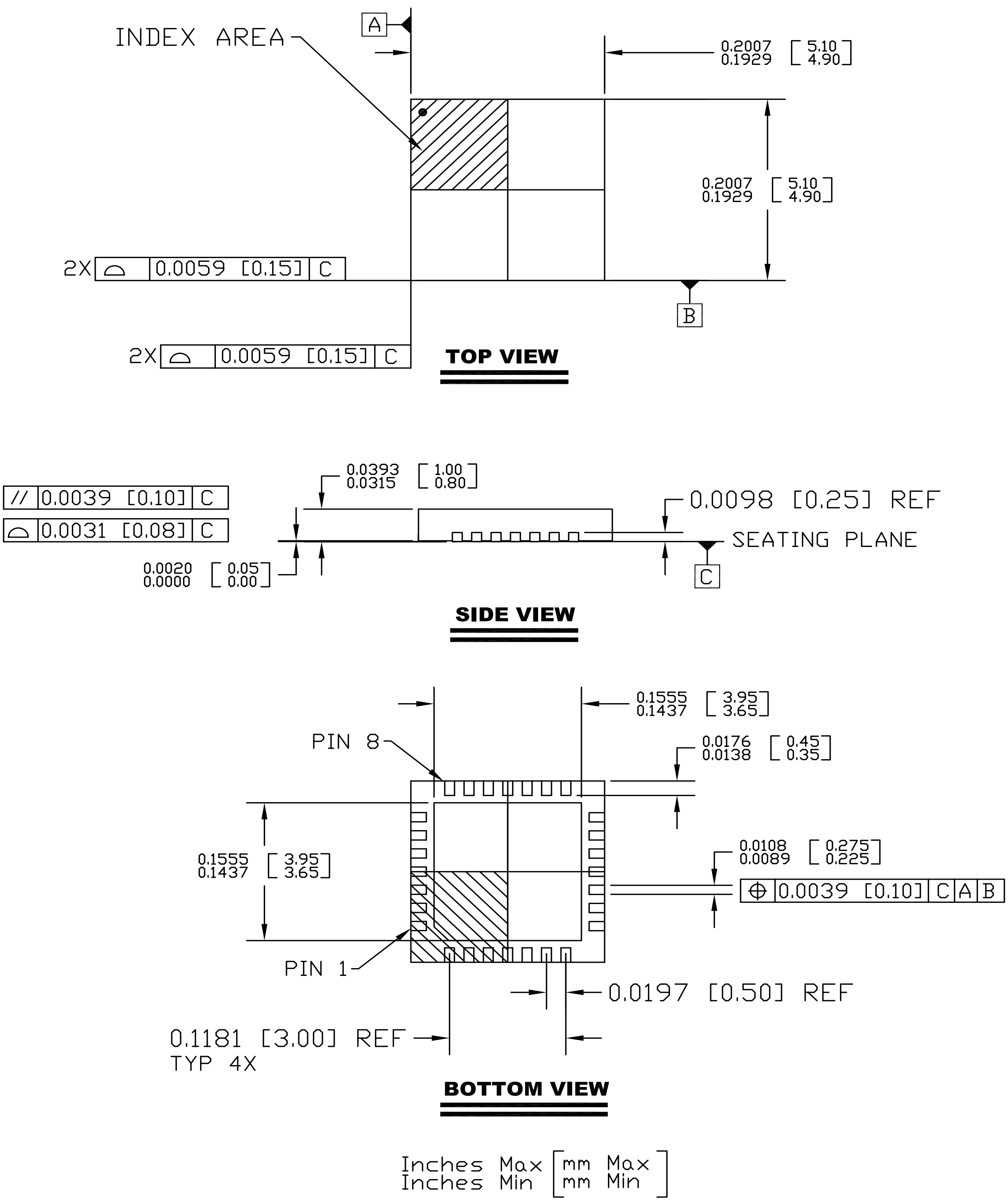
48 PIN TQFP PACKAGE



PACKAGES (CONTINUED)

28 PIN QFN PACKAGE

REFERENCE JEDEC MO-220



ORDERING INFORMATION

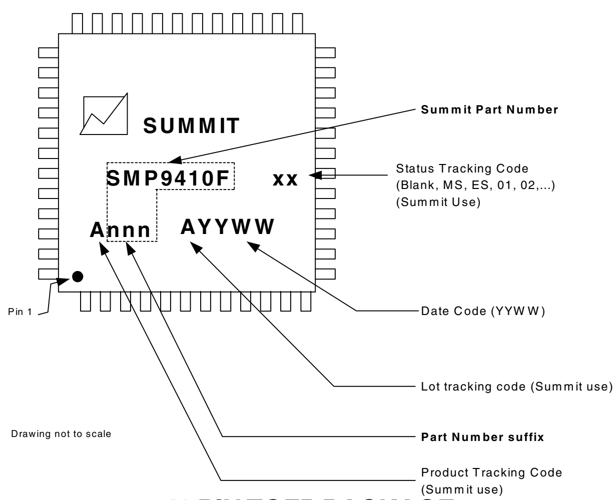
SMP9410 N

Base Part Number — SMP9410

Package — N
N = QFN
F = TQFP

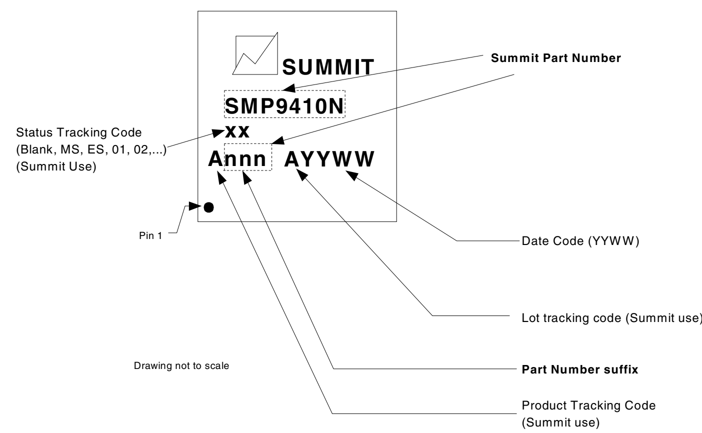
2056 Tree

PART MARKING



48 PIN TQFP PACKAGE

Top View



28 PIN QFN PACKAGE

Top View

NOTICE

Note 1 - This is a Preliminary Information data sheet that describes a Summit product currently in pre-production with limited characterization..

Revision 2.0 - This Document supersedes all previous versions.

I^2C is a trademark of Philips Corporation.