



N-Channel 30-V (D-S) MOSFETs

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
Channel-1 and Channel-2	30	0.012 at V _{GS} = 10 V	16 ^a	6.8 nC
		0.0145 at V _{GS} = 4.5 V	16 ^a	

FEATURES

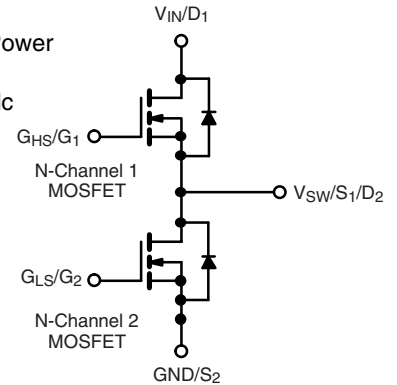
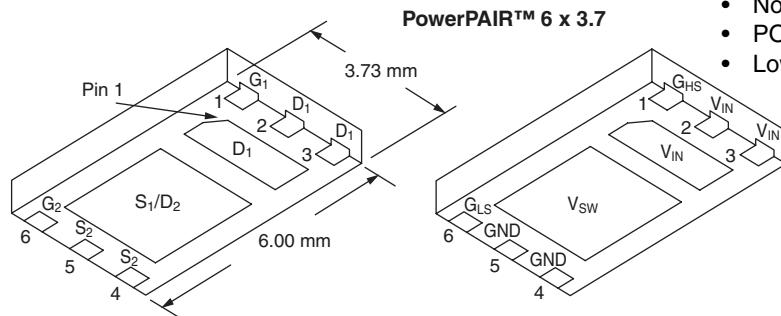
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFETs
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Notebook System Power
- POL
- Low Current dc-to-dc



Ordering Information: SiZ702DT-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Channel-1	Channel-2	Unit
Drain-Source Voltage	V _{DS}	30		V
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	16 ^a		A
		16 ^a		
		13.8 ^{b, c}	14 ^{b, c}	
		11 ^{b, c}	11.2 ^{b, c}	
Pulsed Drain Current	I _{DM}	50		A
Source Drain Current Diode Current	I _S	16 ^a	16 ^a	
		3.2 ^{b, c}	3.7 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	18		mJ
Single Pulse Avalanche Energy	E _{AS}	16		
Maximum Power Dissipation	P _D	27	30	W
		17.4	19	
		3.9 ^{b, c}	4.5 ^{b, c}	
		2.5 ^{b, c}	2.9 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	24	32	21	28	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	3.5	4.6	3.2	4.2		

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 67 °C/W for Channel-1 and for Channel-2.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1 Ch-2	30		V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1 Ch-2		33	mV/ $^\circ\text{C}$	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1 Ch-2		- 5		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1 Ch-2	1		2.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch-1 Ch-2			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1 Ch-2			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1 Ch-2			5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1 Ch-2	20			A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 13.8\text{ A}$	Ch-1 Ch-2		0.010	0.012	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 12.6\text{ A}$	Ch-1 Ch-2		0.012	0.0145	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 13.8\text{ A}$	Ch-1 Ch-2		47		S
Dynamic^a							
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1 Ch-2		790		pF
Output Capacitance	C_{oss}		Ch-1 Ch-2		190		
Reverse Transfer Capacitance	C_{rss}		Ch-1 Ch-2		76		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 13.8\text{ A}$	Ch-1 Ch-2		14	21	nC
			Ch-1 Ch-2		6.8	11	
Gate-Source Charge	Q_{gs}	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 13.8\text{ A}$	Ch-1 Ch-2		2.6		
Gate-Drain Charge	Q_{gd}		Ch-1 Ch-2		1.9		
Gate Resistance	R_g	$f = 1\text{ MHz}$	Ch-1 Ch-2	0.4	2	4	Ω

Notes:

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$	Ch-1		15	25	ns
Rise Time	t_r		Ch-2		12	20	
Turn-Off Delay Time	$t_{d(off)}$		Ch-1		20	30	
Fall Time	t_f		Ch-2		10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	Ch-1		10	15	
Rise Time	t_r		Ch-2		12	20	
Turn-Off Delay Time	$t_{d(off)}$		Ch-1		20	30	
Fall Time	t_f		Ch-2		10	15	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			16	A
Pulse Diode Forward Current ^a	I_{SM}		Ch-2			50	
Body Diode Voltage	V_{SD}	$I_S = 10\text{ A}, V_{GS} = 0\text{ V}$	Ch-1		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch-1		20	40	ns
Body Diode Reverse Recovery Charge	Q_{rr}		Ch-2		10	20	nC
Reverse Recovery Fall Time	t_a		Ch-1		11		ns
Reverse Recovery Rise Time	t_b		Ch-2		9		

Notes:

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

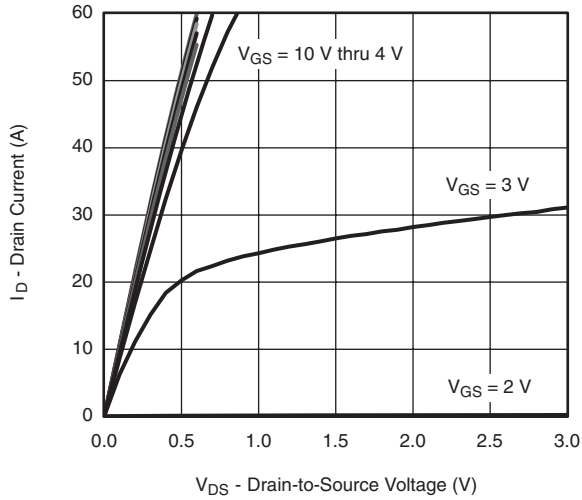
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SiZ702DT

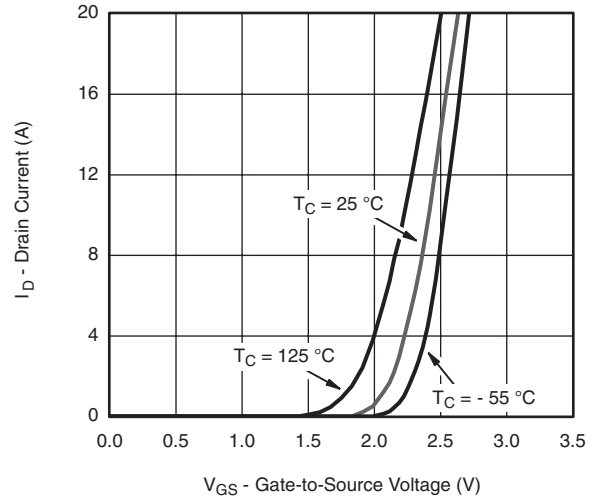
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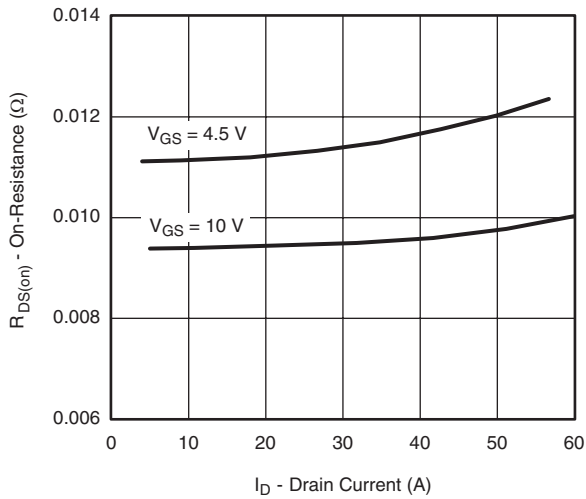
CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



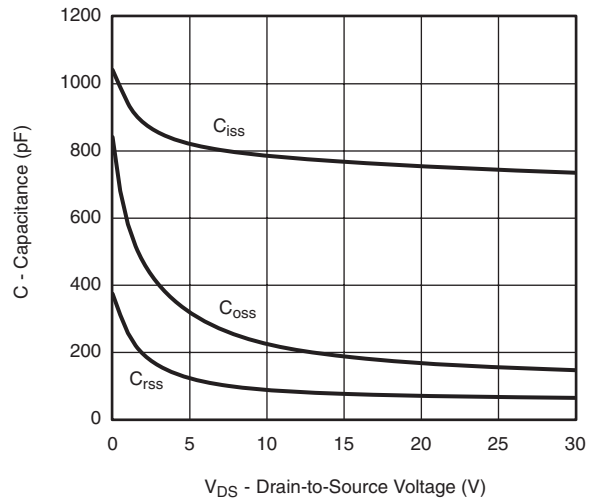
Output Characteristics



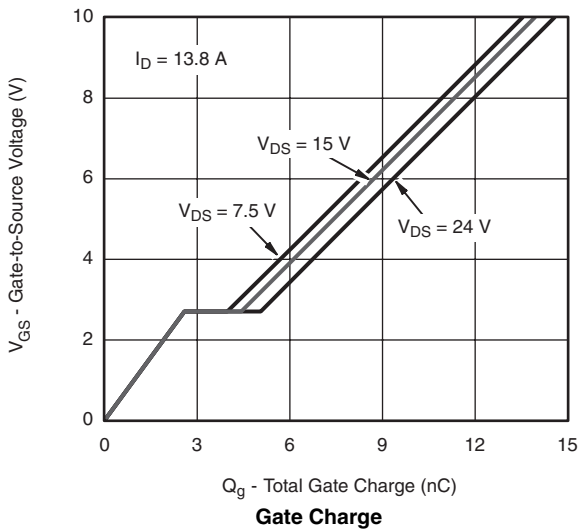
Transfer Characteristics



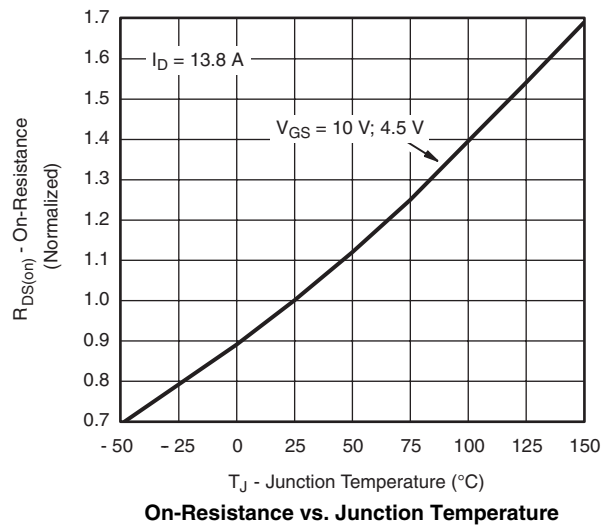
On-Resistance vs. Drain Current



Capacitance



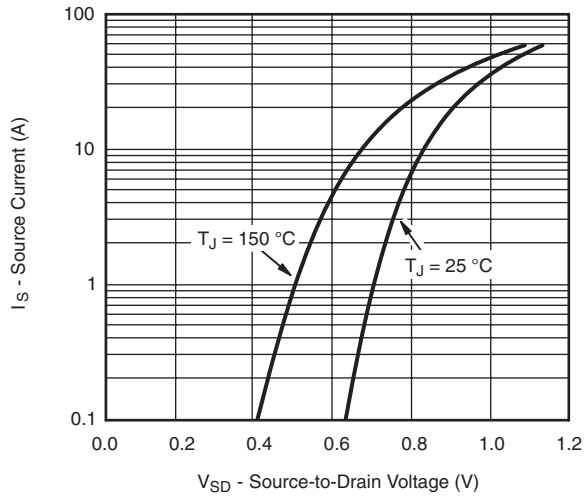
Gate Charge



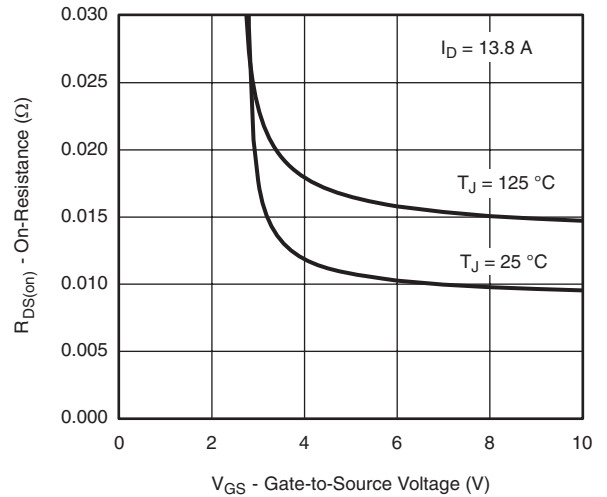
On-Resistance vs. Junction Temperature



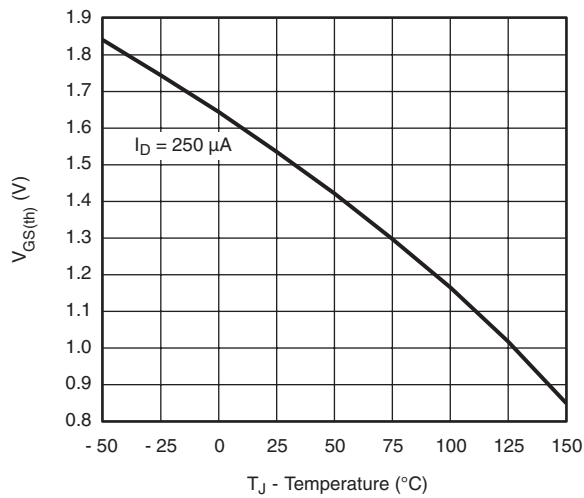
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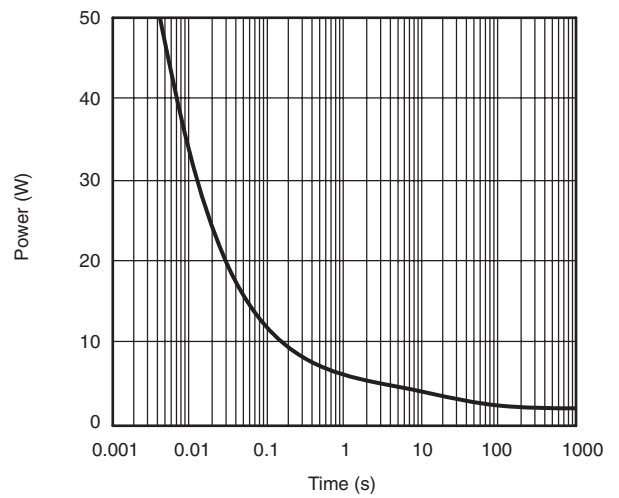
Source-Drain Diode Forward Voltage



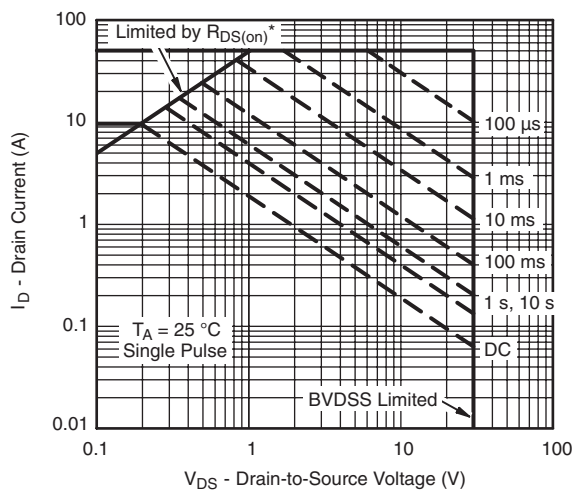
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

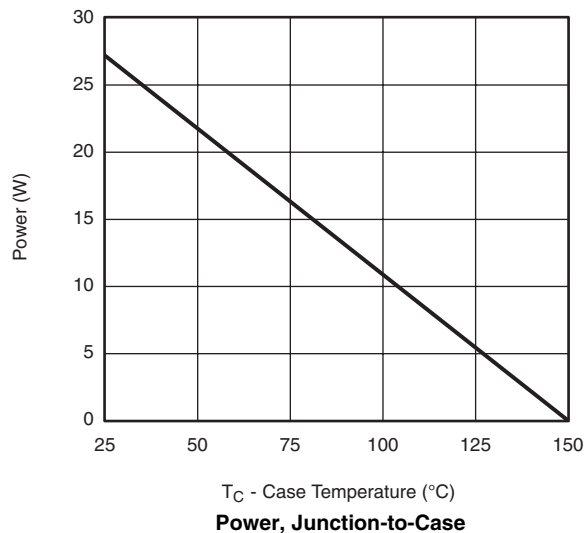
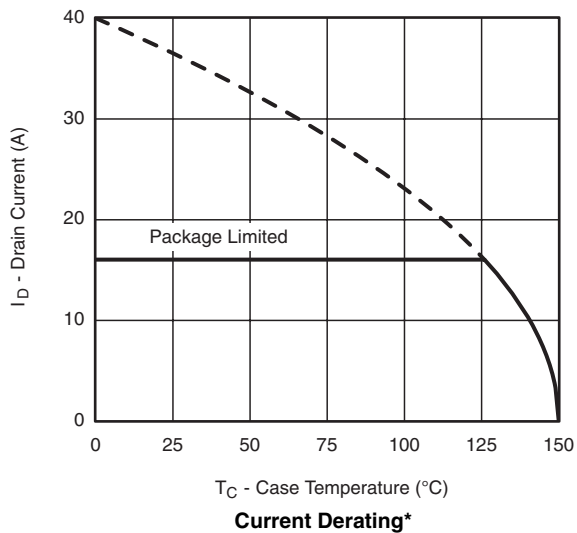
Safe Operating Area, Junction-to-Ambient

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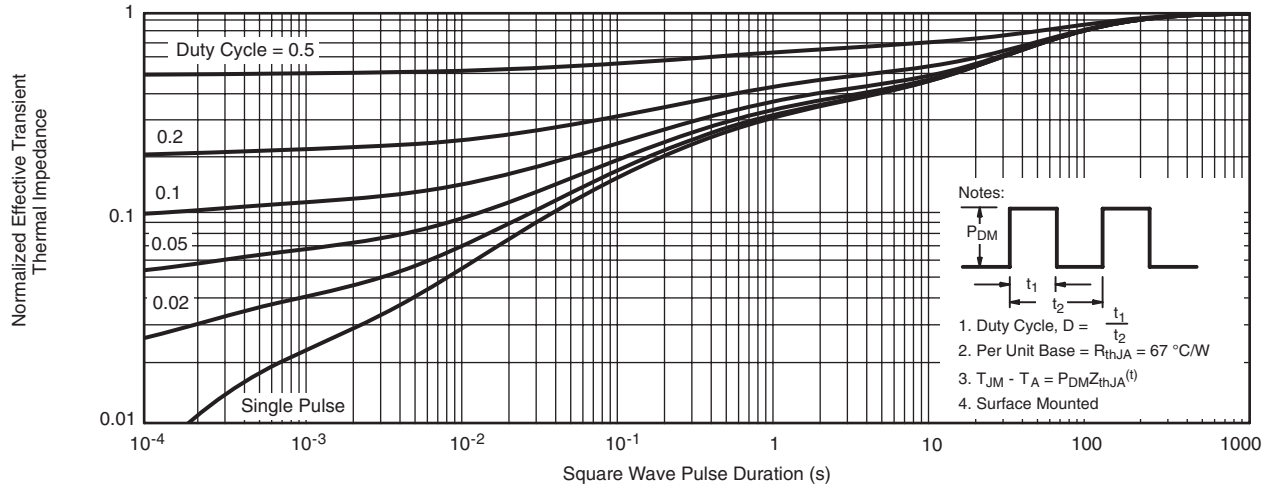
CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



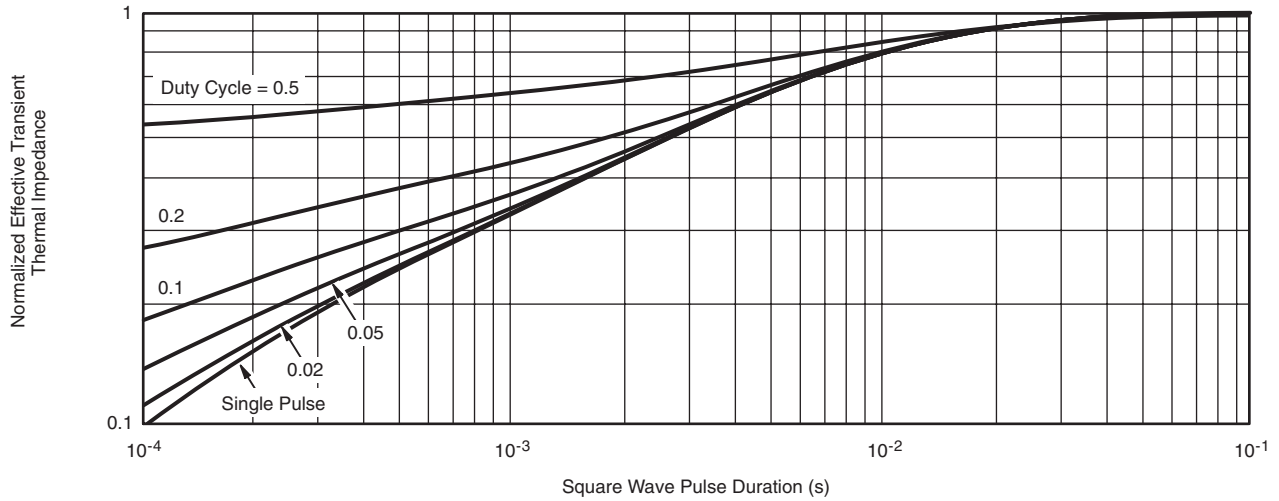
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



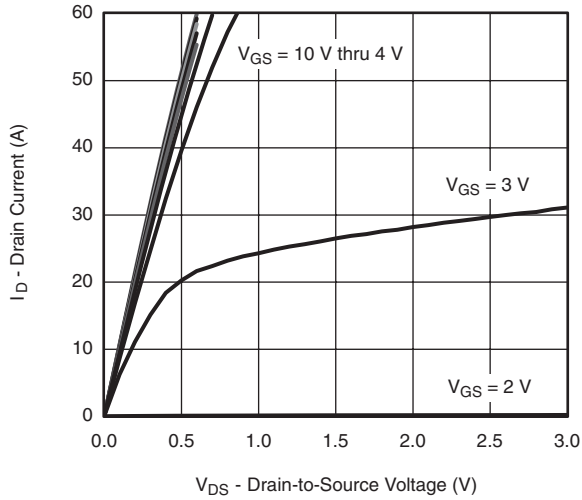
Normalized Thermal Transient Impedance, Junction-to-Case

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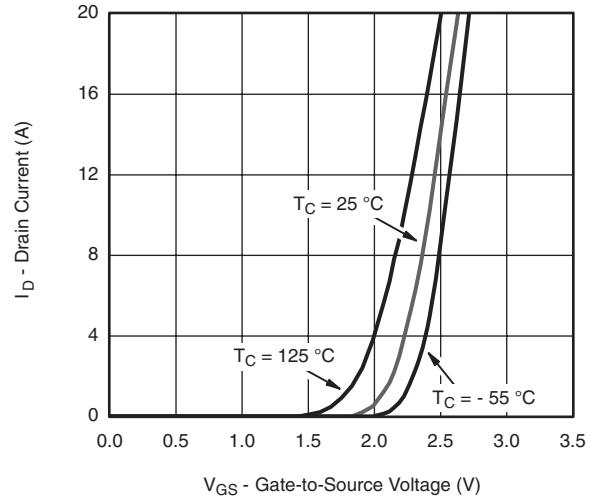
Vishay Siliconix



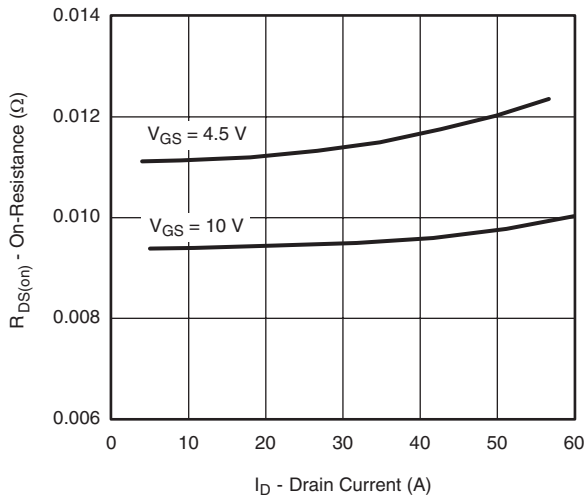
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



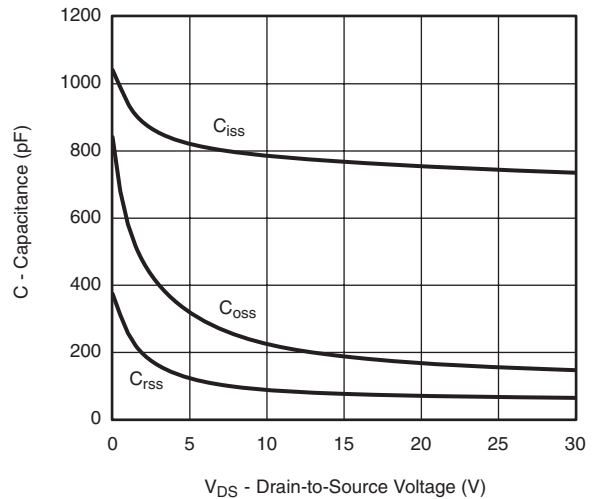
Output Characteristics



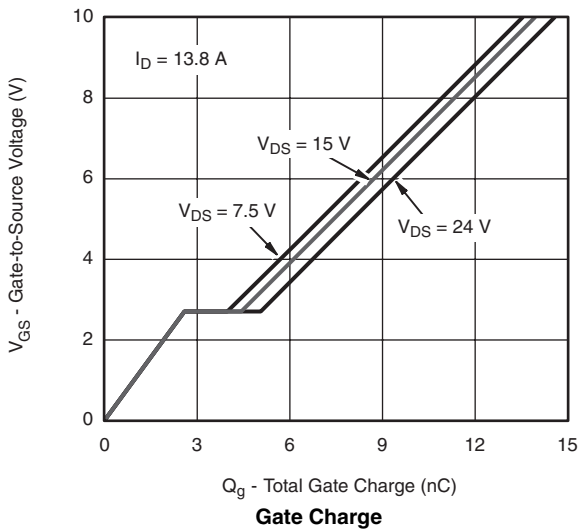
Transfer Characteristics



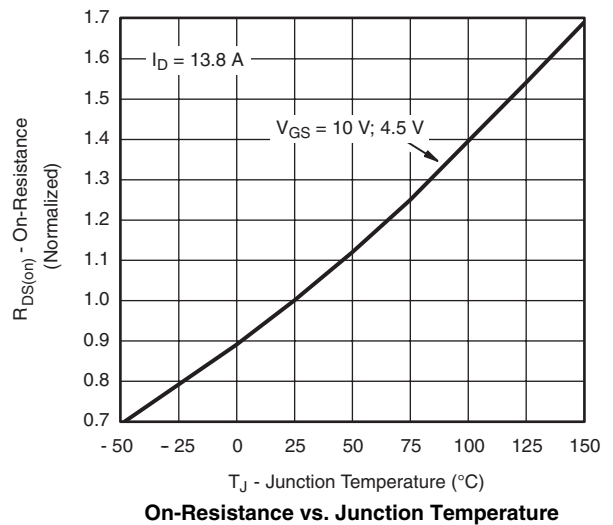
On-Resistance vs. Drain Current



Capacitance



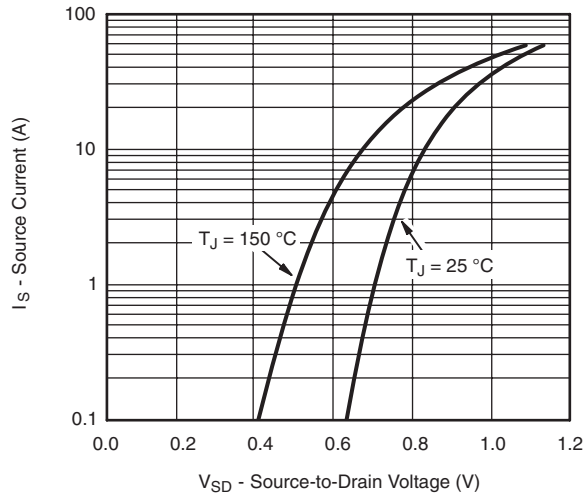
Gate Charge



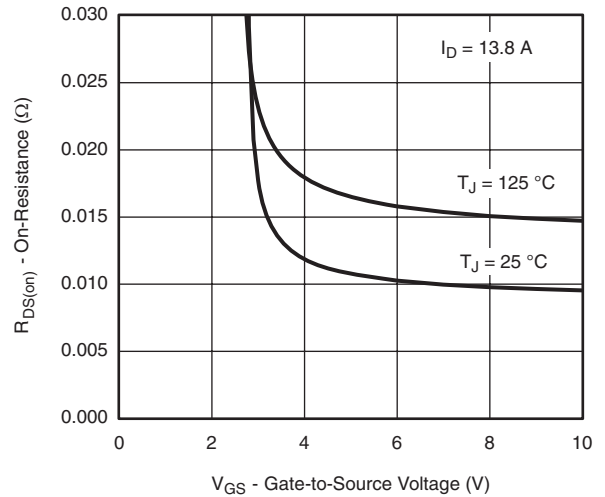
On-Resistance vs. Junction Temperature



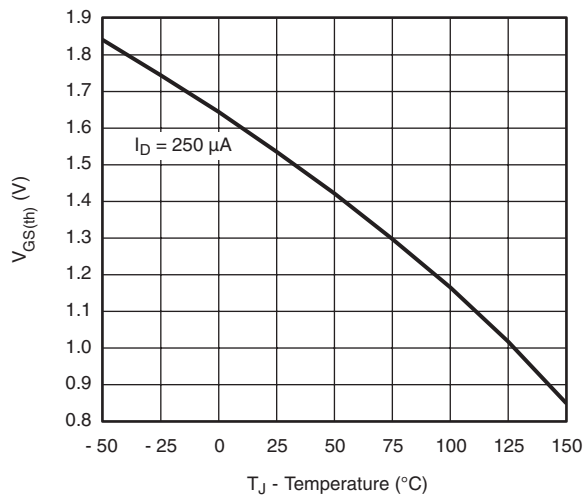
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



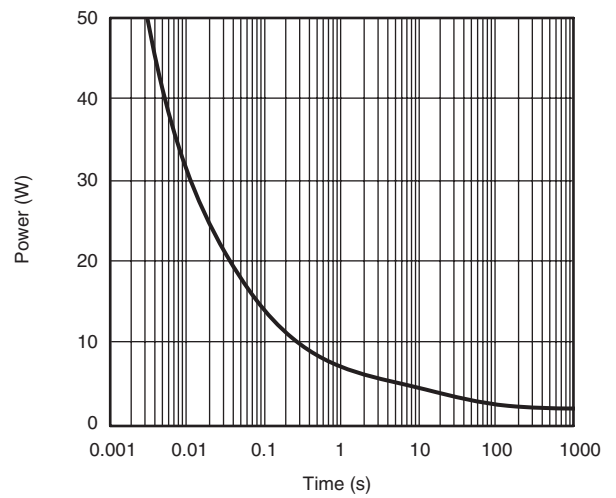
Source-Drain Diode Forward Voltage



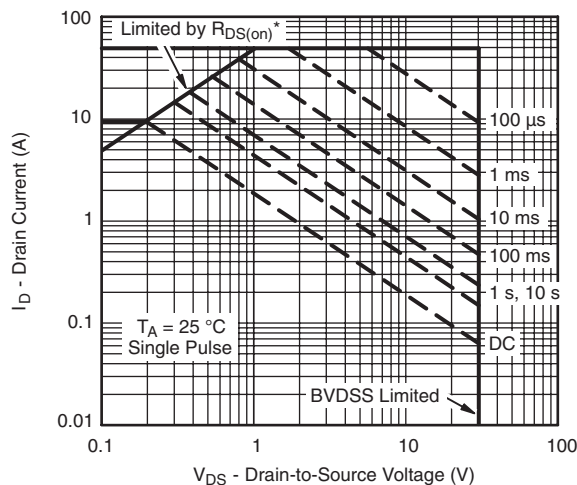
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

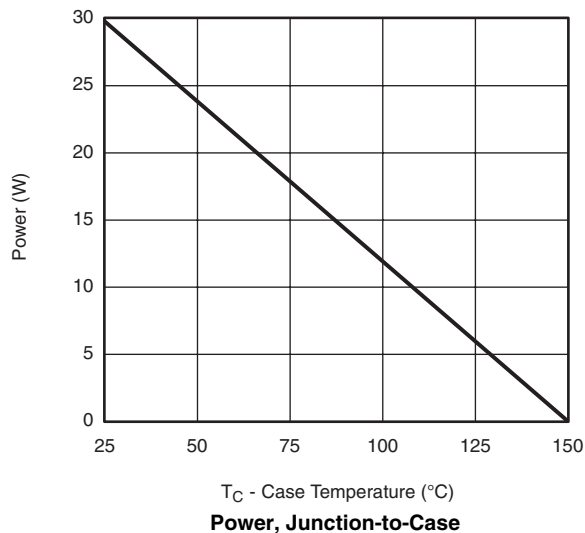
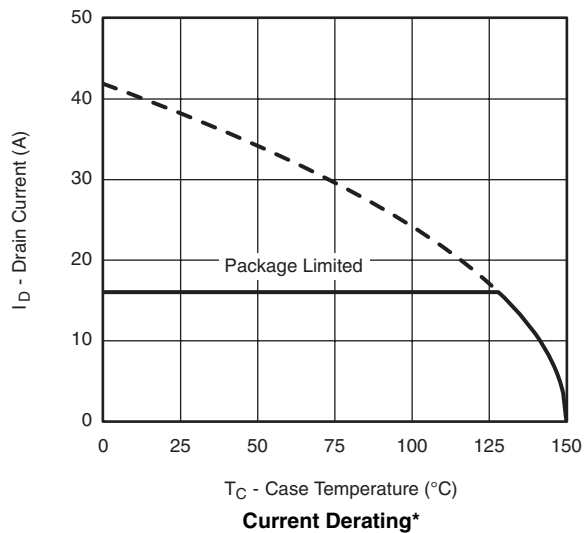
Safe Operating Area, Junction-to-Ambient

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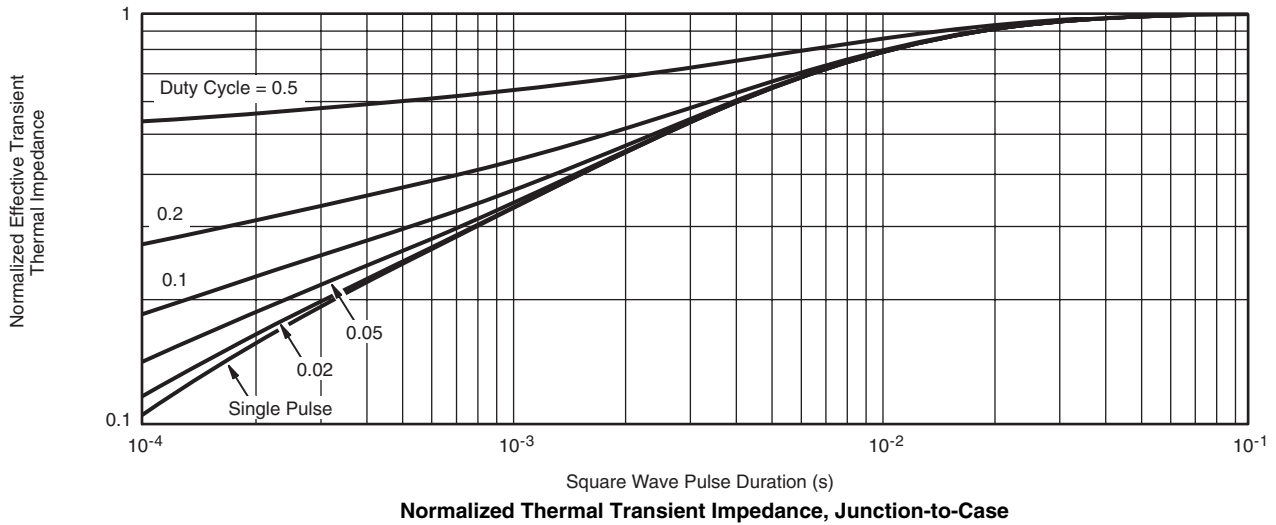
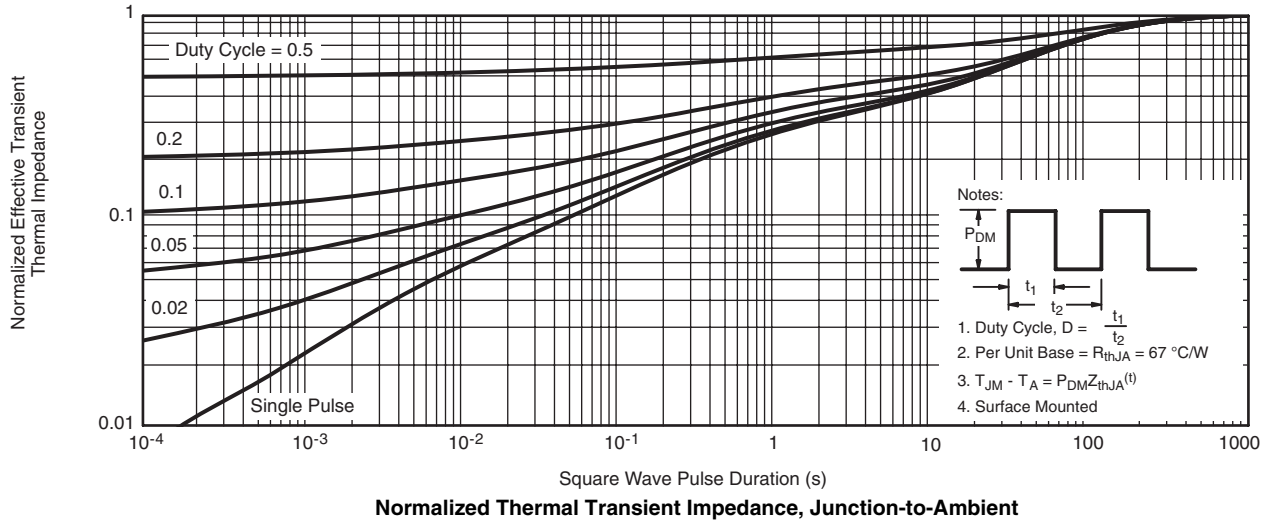
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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