

SAMSUNG ELECTRONICS Co., Ltd.

SPECIFICATION No.	
H9908010NS	
Issue Date.	9 Sep. 1999
Revised Date.	12 Nov. 1999
REV.	1
Cut No.	3.2

**MICRO MODULE
SPECIFICATIONS**

PF08109B-TB

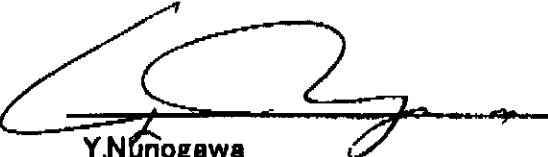
This document is revised.
Please return this document with your approval
signature by 22 Nov. 1999.

수신: 부품 표준팀 이명수 &

발신: 기획 부원 김태민
7/6/99

대사 : 1604

Micro Module Engineering Department
Multi Purpose Semiconductor Business Operation
Semiconductor & Integrated Circuits
HITACHI, LTD.


Y. Nunogawa

- ★ Correct
- ★★ Add
- ★★★ Delete

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Q. CM KD.

RE REGD.

11-22 13:36 MON FROM: SAMSUNG

1. Outline

Item \ Gr.	A	B	C
Customer name	SAMSUNG ELECTRONICS Co.,Ltd		
Customer type	—		
Hitachi type	PF08109B-TB		
Application	RF Power Amplifier		
Structure	Thick Film Hybrid IC		
Package	RF-O		
Note	—		

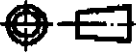
2. Absolute Maximum Ratings (Unless otherwise noted : Tc=25degC)

No.	Item	Gr. Syn.	A	B	C	Unit
1	Supply voltage	Vdd	8 *1			V
2	Supply current	Idd GSM Idd DCS	3 2			A
3	APC voltage	Vapc	4 *2			V
4	Vtxlo voltage	Vtxlo	4			V
5	Input power	Pin	10			dBm
6	Operating case temp.	Tc (op)	-30 to +100			degC
7	Storage temperature	Tstg.	-30 to +100			degC
8	Output Power	Pout GSM Pout DCS	5 3 *3			W

*1: This value is specified at no operation (Vapc=0V, Pin=none)

*2: This value is specified at no operation (Vdd=0V, Pin=none)

*3: This value is specified at 50 ohm load operation

Gr.	A	B	C	D
REMARKS	PROJECTION	SCALE	REGD.	SDTYPE D.D.
H9908010NS		NTS		
DWN.	TITLE			SH.
CHD.	PF08109B-TB CAS			2
REF.	Hitachi, Ltd.			
	Tokyo Japan			
	Semiconductor & Integrated Circuits Division			
	345			

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

Test conditions unless otherwise noted:

f=1710 to 1785MHz, Vdd_DCS=3.5V, Pin_DCS=0dBm, Vapc_GSM=0.1V, Vtxlo=0.1V, Rg=RI=50ohm, Tc=25degC
Pulse operation with pulse width 577us and duty cycle 1:8 shall be used.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Note
Frequency range	f	1710	—	1785	MHz		*1
Control voltage range	Vapc	0.2	—	2.2	V		
Total efficiency (H1)	hT (H1)	38	43	—	%	Pout_DCS=32.7dBm	*2
2nd harmonic distortion	2nd_H.D	—	-45	-38	dBc	Vapc_DCS=control	
3rd harmonic distortion	3rd_H.D	—	-45	-40	dBc		
Input VSWR	VSWR(In)	—	1.5	3	—		
Total efficiency (Lo)	hT (Lo)	17	25	—	%	Pout_DCS=26.7dBm Vapc_DCS=control	*2
Output power (1)	Pout(1)	32.7	33.2	—	dBm	Vapc_DCS=2.2V	*2
Output power (2)	Pout(2)	30.7	31.2	—	dBm	Vdd_DCS=3.0V, Vapc_DCS=2.2V Tc=+85degC	*2
Isolation	—	—	-42	-36	dBm	Vapc_DCS=0.2V	
Isolation at GSM RF-output when DCS is active	—	—	-10	0	dBm	Pout_DCS=32.7dBm Measured at f=1710 to 1785MHz	GBD
Switching time	tr, tf	—	1	2	us	Pout_DCS=0 to 32.7dBm	GBD
Stability	—	No parasitic oscillation			—	Vdd_DCS=3.0 to 5.1V Pout_DCS≤32.7dBm Rg=50ohm Output VSWR=8:1 All phases Vapc_DCS≤2.2V DCS pulse	*4 GBD
Load VSWR tolerance	—	No degradation or Permanent degradation			—	Vdd_DCS=3.0 to 5.1V, t=20sec. Pout_DCS≤32.7dBm Vapc_DCS≤2.2V DCS pulse Rg=50ohm Output VSWR=10:1 All phases	*4 *5 GBD

PROV.
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PY

Gr.	A	B	C	D
REMARKS	PROJECTION	SCALE	REGD.	SDTYPE D.D
H9908010NS		NTS		
CLASS.	MD	WORKSPEC No		
	M			
DWN.	TITLE			SH.
CHND.	PF08109B-TB CAS			6
ASST.	Hitachi, Ltd.			
	Tokyo Japan			
	Semiconductor & Integrated Circuits Division			
	345			

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

6. Electrical Characteristics.

Electrical Characteristic for GSM900 mode

Test conditions unless otherwise noted:

f=880 to 915MHz, Vdd_GSM=3.5V, Pin_GSM=0dBm, Vapc_DCS=0.1V, Rg=RI=50ohm, Tc=25degC
Pulse operation with pulse width 577us and duty cycle 1:8 shall be used.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Note
Frequency range	f	880	—	915	MHz		
Control voltage range	Vapc	0.2	—	2.2	V		
Total efficiency (HI)	hT (HI)	43	50	—	%	Pout_GSM=35.5dBm, Vtxlo=0.1V,	*2
2nd harmonic distortion	2nd. H.D.	—	-45	-38	dBc	Vapc_GSM=control	
3rd harmonic distortion	3rd. H.D.	—	-45	-40	dBc		
Input VSWR	VSWR(in)	—	1.5	3	—		
Total efficiency (Lo)	hT (Lo)	27	35	—	%	Pout_GSM=30.8dBm, Vtxlo=2.4V Vapc_GSM=control	*2
Output power (1) (HI)	Pout(1) (HI)	35.5	36.0	—	dBm	Vapc_GSM=2.2V, Vtxlo=0.1V	*2
Output power (1) (Lo)	Pout(1) (Lo)	30.8	31.3	—	dBm	Vapc_GSM=2.2V, Vtxlo=2.4V	*2
Output power (2) (HI)	Pout(2) (HI)	33.5	34.0	—	dBm	Vdd_GSM=3.0V, Vapc_GSM=2.2V Tc=+85degC, Vtxlo=0.1V	*2
Output power (2) (Lo)	Pout(2) (Lo)	28.8	29.3	—	dBm	Vdd_GSM=3.0V, Vapc_GSM=2.2V Tc=+85degC, Vtxlo=2.4V	*2
Isolation	—	—	-42	-36	dBm	Vapc_GSM=0.2V, Vtxlo=0.1V	
Isolation at DCS RF-output when GSM is active	—	—	-23	-17	dBm	Pout_GSM=35.5dBm, Vtxlo=0.1V Measured at f=1760 to 1830MHz	
Switching time	tr, tf	—	1	2	us	Pout_GSM=0to +35.5dBm, Vtxlo=0.1V	GBD
Stability	—	No parasitic oscillation			—	Vdd_GSM=3.0 to 5.1V Pout_GSM≤35.5dBm Vapc_GSM≤2.2V GSM pulse Vtxlo=0.1V, 2.4V, Rg=50ohm Output VSWR=6:1 All phases	*4 GBD
Load VSWR tolerance	—	No degradation or Permanent degradation			—	Vdd_GSM=3.0 to 5.1V, t=20sec. Pout_GSM≤35.5dBm Vapc_GSM≤2.2V GSM pulse Vtxlo=0.1V, 2.4V, Rg=50ohm Output VSWR=10:1 All phases	*4 *5 GBD

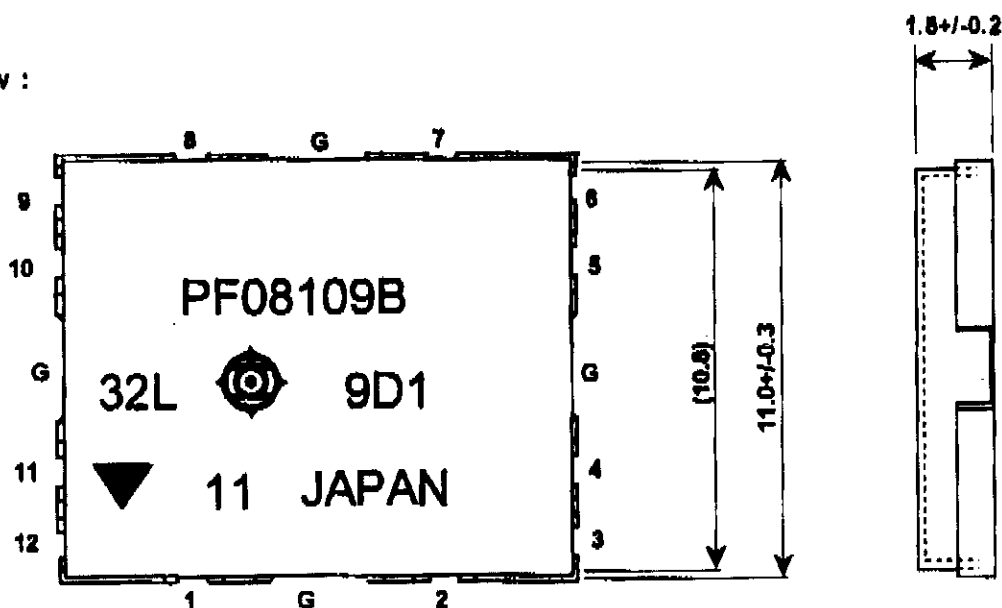
PROV. SECT.

Gr.	A	B	C	D
REMARKS	PROJECTION	SCALE	REGD.	SD TYPE D.D.
H9908010NS		NTS		
D. CHKD.				
CHND.				
RE REQD.				
TITLE		Hitachi, Ltd.		Semiconductor & Integrated Circuits Division
PF08109B-TB CAS		Tokyo Japan		SH. 5
		345		

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3. Package outline

Top view :

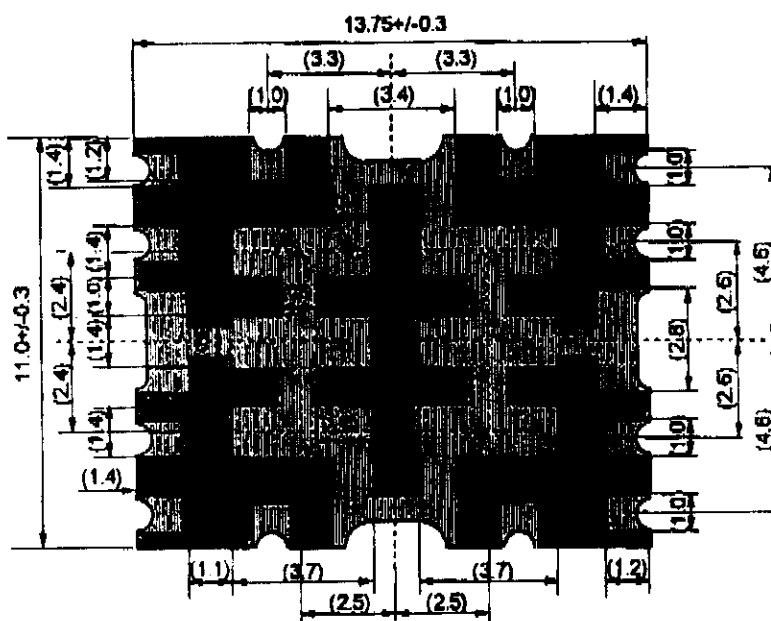


unit:mm



Pin assignment

Bottom view :



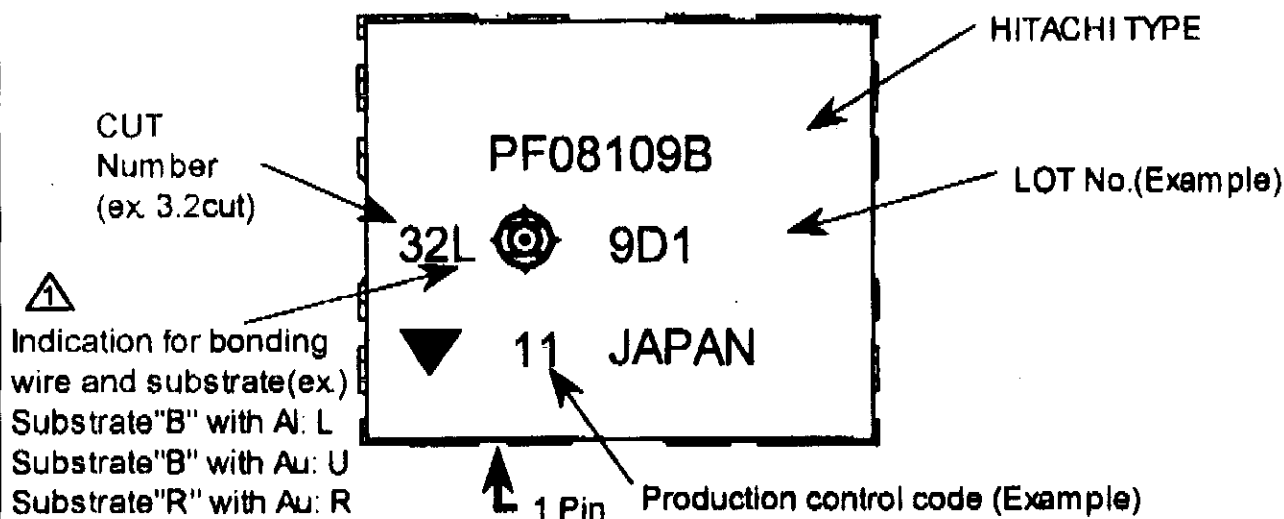
- 1 : NC
- 2 : NC
- 3 : Pout_DCS
- 4 : Vdd_DCS
- 5 : Vdd_GSM
- 6 : Pout_GSM
- 7 : NC
- 8 : Vtxio
- 9 : Pin_GSM
- 10 : Vapc_GSM
- 11 : Vapc_DCS
- 12 : Pin_DCS
- G : GND

Remark : Coplanarity of bottom side of terminals are less than 0±/0.1mm

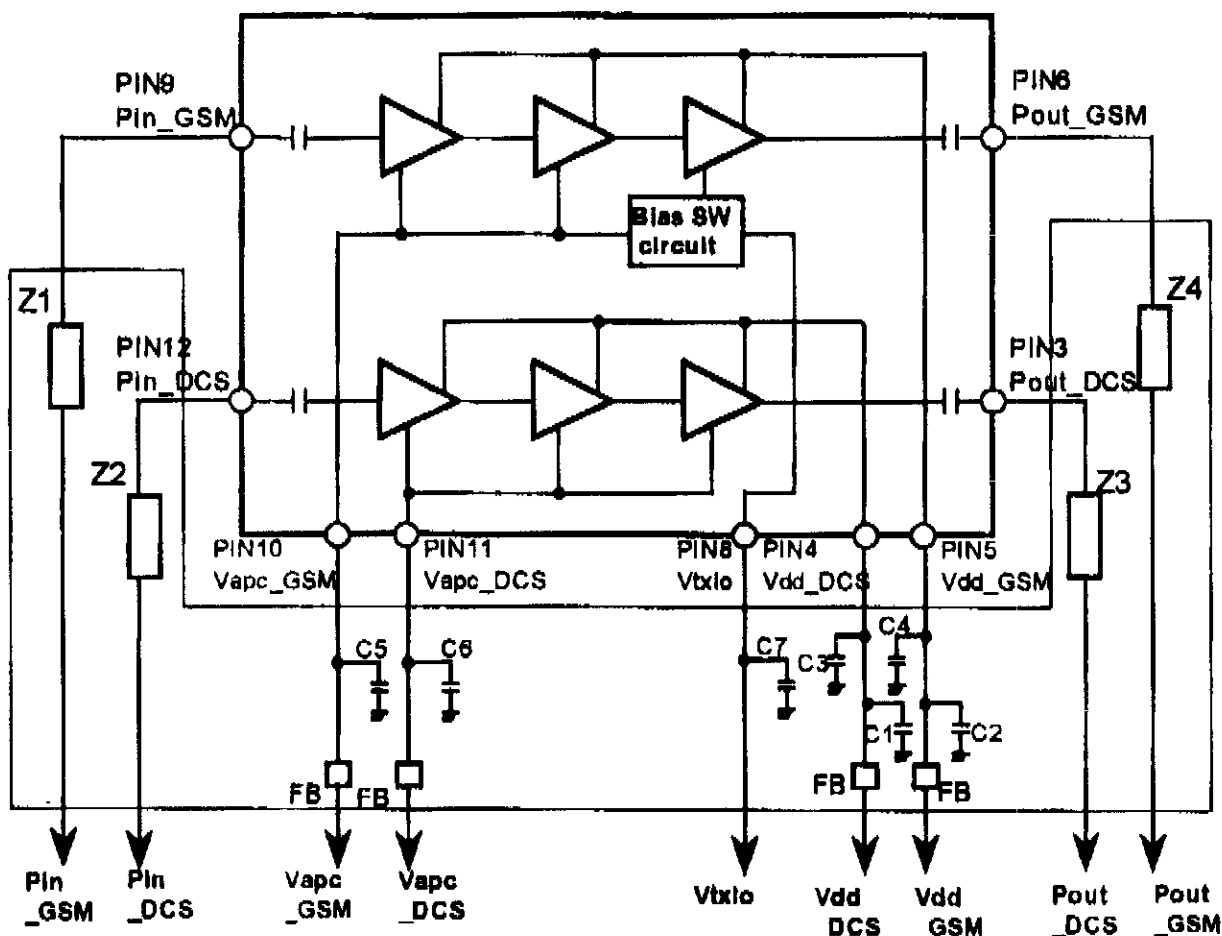
Gr.	A	B	C	D
REMARKS	H9908010NS			
PROJECTION				
SCALE	NTS			
REGD.				
SDTYPE D.D				
CLASS.				
MD	M			
WORK SPEC No				
DWN.				
CHD.				
APPR.				
TITLE	PF08109B-TB CAS			
Hitachi, Ltd.	Tokyo Japan			
Semiconductor & Integrated Circuits Division	345			
SH.	3			

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

4. Marking



5. Internal Diagram and External Circuit



C1=C2=4.7uF TANTALUM ELECTROLYTE
 C3=C4=0.01uF CERAMIC CHIP
 C5=C6=C7=1000pF CERAMIC CHIP
 FB=FERRITE BEAD BLO1RN1-A82-001(MURATA) or equiv alent
 Z1=Z2=Z3=Z4=50ohm MICRO STRIP LINE

Gr.	A	B	C	D
REMARKS	PROJECTION	SCALE	REGD.	SDTYPE D.D.
H9908010NS	NTS			
TITLE	Hitachi, Ltd.		Semiconductor & integrated Circuits Division	
PF08109B-TB CAS	Tokyo Japan		345	
SH.	4			

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Electrical Characteristic for DC

*1

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Note
Drain cutoff current	I _{ds}	—	—	100	uA	V _{dd} =8.0V, V _{apc} =0V, V _{txlo} =0.1V	
Vapc control current	I _{apc}	—	—	3	mA	V _{apc} =2.2V	
V _{txlo} control current	I _{txlo}	—	—	100	uA	V _{txlo} =2.4V	

*1: Items indicated GBD on Note are guaranteed by design and not tested.

*2: Output power P_{out} is defined at the root point of the module output pin P_{out}. The coefficient of output power loss in the P.C.B output line is showed as follows:

$$1/(S21)^2 = 1/(0.988)^2 = 1.02 \quad \text{at GSM band}$$

$$1/(S21)^2 = 1/(0.980)^2 = 1.04 \quad \text{at DCS band}$$

*3: characteristics not indicated as GBD are guaranteed under the following inspection level. AQL = 1.0, inspection level = II

AQL value refer to ANSI/ASQC-Z1.4

*4: P_{out} is defined as the transmission power using the directional coupler which is connected at load.

*5: GSM pulse is applied to Vapc

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Gr.	A	B	C	D
REMARKS	PROJECTION	SCALE	REGD.	SDTYPE D.D.
H9908010NS		NTS		
D. CHAD.	TITLE		CLASS.	MD WORK SPEC No.
	PF08109B-TB CAS			M
RE REGD.	Hitachi, Ltd. Tokyo Japan		Semiconductor & Integrated Circuits Division 345	SH. 7

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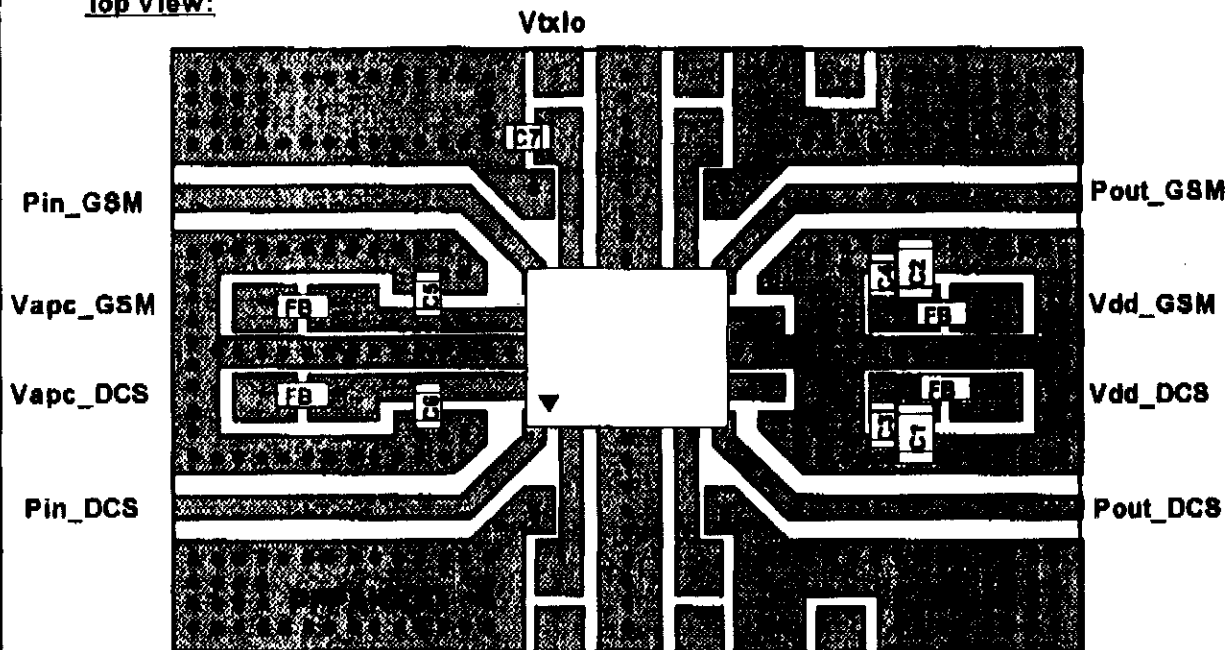
7. Test Fixture Pattern

7.1 Standard Test fixture for testing:

The test reference guarantes for all electorical characteristics is the Anritsu test fixture ME0104A. External circuit is specified in Item 5 (page 4).

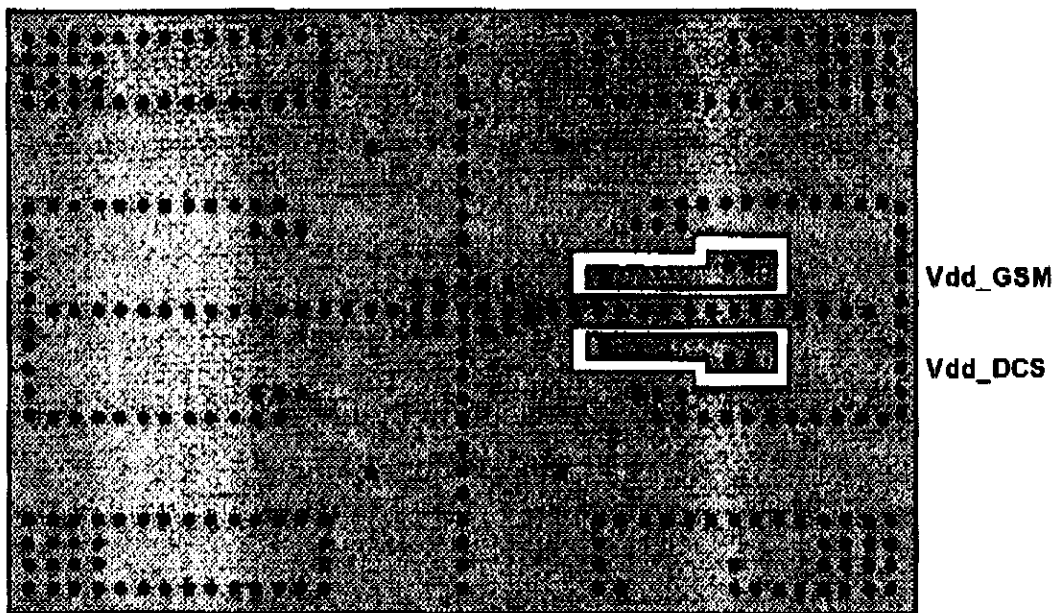
7.2 Standard PCB pattern and external parts for evaluation :

Top view:



C1=C2=4.7uF
C3=C4=0.01upF
C5=C6=C7=1000pF
FB= Ferrite Bead

Bottom view:



Grass Epoxy Double sided P.C.B (t = 0.85mm, $\epsilon_r = 4.8$)

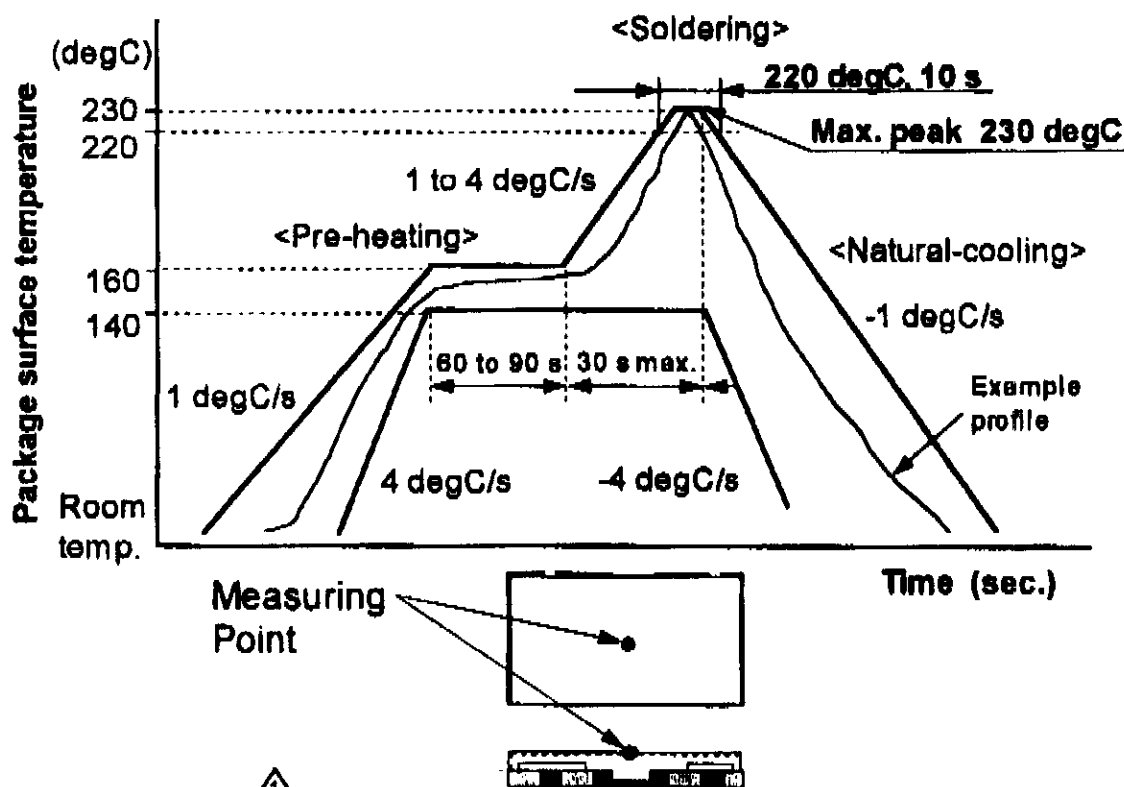
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H9908010NS		NTS		
DAN.	TITLE			CLASS.
CHNO.	PF08109B-TB CAS			NO WORK SPEC No
RE REQD.	Hitachi, Ltd.			M
	Tokyo Japan			
	Semiconductor & Integrated Circuits Division			SH
	345			8

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- 1) It should not be applied the mechanical stress on the module metal cap.
- 2) To protect devices from electro-static damage, soldering iron, measuring equipment and human body, etc. should be grounded.

8-4. Soldering:

- 1) Soldering temperature and time for I.R. Reflow and hot air Reflow must be within the following reflow profile shown in Fig3. 
- 2) Don't apply dipping solder method to soldering.
- 3) The solder paste including 2% Ag (Sn/Pb/Ag=62/36/2) is strongly recommended.
- 4) Reflow-soldering is permitted max two times, in order to keep the reliability of terminal connection.
- 5) The condition for manual hot gas soldering should be keep as follows,
Max. air temperature: 300 degC, Max. air velocity: 6 m/sec, Max. exposure time: 15sec.
- 6) Don't use the soldering iron for rework process, because the product has to be fully soldered its bottom side of terminals for stable operation.



(Fig3) Recommended Reflow profile

8-5. Washing:

- 1) After soldering, don't wash the module. Washing less solder paste is recommended.

8-6. Storage:

- 1) To get stable solderability, it should be avoid to put the sulfide material close to the module,
and avoid to storage the module at high temperature and humidity area.
- 2) Recommended shipping and strage condition: Relative humidity: 15 to 70%,
Temperature: -5 to +40 degC.

Gr.	A	B	C	D
REMARKS	PROJECTION	SCALE	REGD.	SDTYPE O.D.
H9908010NS		NTS		
D. CHKD.	TITLE	Hitachi, Ltd.		SH.
DWN.	PF08109B-TB CAS	Semiconductor & Integrated Circuits Division		10
CHKD.		345		
APRD.				

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

9. Warranty

Hitachi obligation shall be and is limited to replacing the products which may be prove to be defective by Hitachi according to this specification.

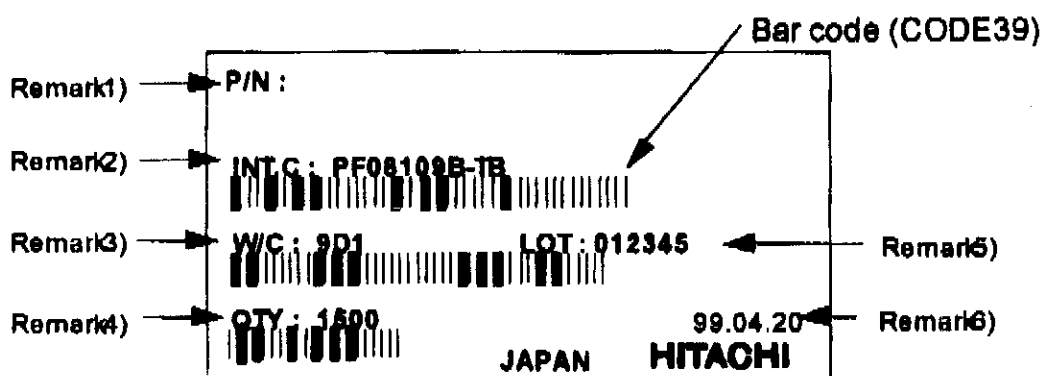
10. Warranty period

Limited one year after the arrival of the products at the port of destination.

11. Packing

1.Bar code:

Example for indication label with bar code



Remark1)P/N:Customer part number (If it required)

Remark2)INT.C:HITACHI product name

Remark3)W/C:Weekly code

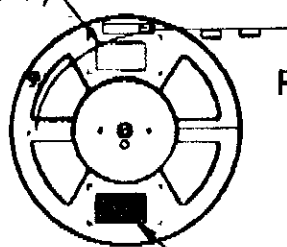
Remark4)QTY:Quantity of products under the indicated weekly code

Remark5)LOT:Delivery code

Remark6)DATE:date

Indicated position of the taping products

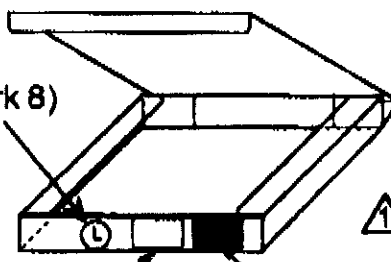
Remark 7)



Bar code label

Indication of reel

Remark 8)



Remark 7)

Bar code label

Indication of packing box

Remark 7) If plural weekly code products are contained in a packing box, label is indicated in this area too.

Sum of these label's quantity indicates the total quantity in a packing.

Remark 8)

Indication for bonding wire and substrate.

(Ex.)Substrate"B" with Al:L
Substrate"B" with Au:U
Substrate"R" with Au:R

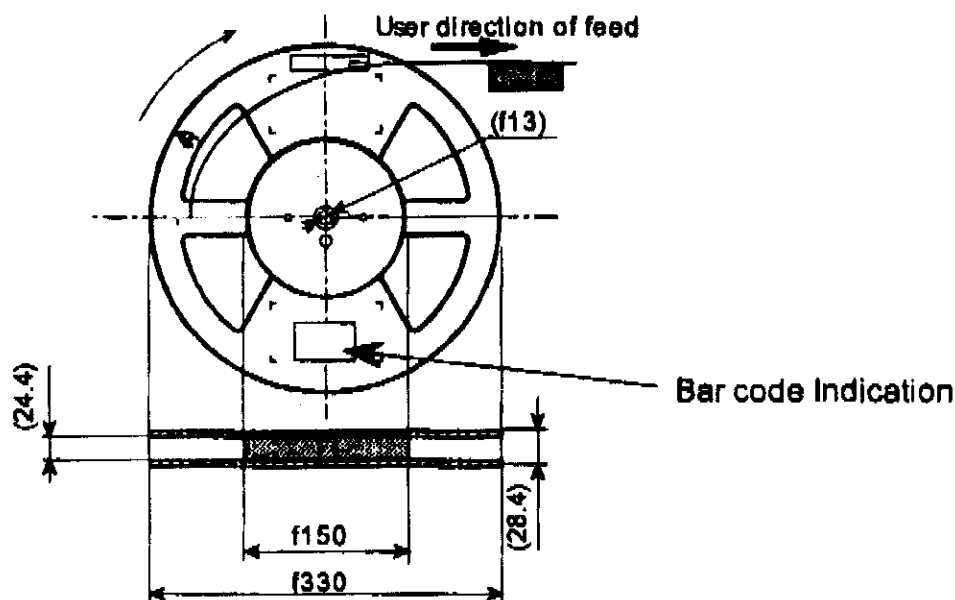
Gr.	A	B	C	D
REMARKS	PROJECTION	SCALE	REQD.	SDTYPE D.D
H9908010NS		NTS		
DWN.	TITLE	Hitachi, Ltd.		Semiconductor & Integrated Circuits Division
CHD.	PF08109B-TB CAS	Tokyo Japan		SH. 11
REFQD.		345		

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

- 1) Tape width : 24mm
- 2) Tape sprocket hole pitch : 4.0mm
- 3) Tape material : Embossed carrier tape ; Carbon coated APET (Amorphous PolyEthylene Terephthalate)
- 4) Cover tape material : PET/PE/PET/SEALNT
- 5) Leader and trailer length , and number empty cavities : 430 mm Min., and 24 cavities

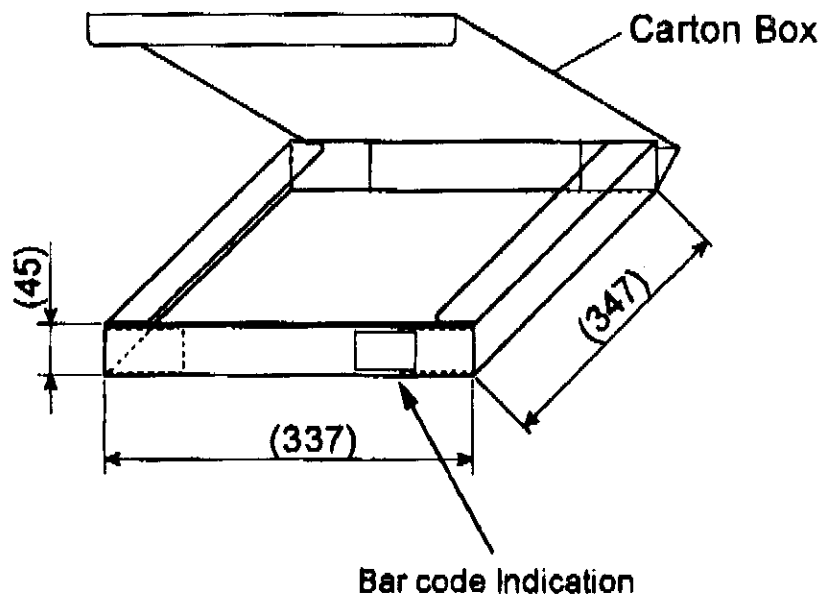


Reel material : RIALREEL ; Ploystyrene



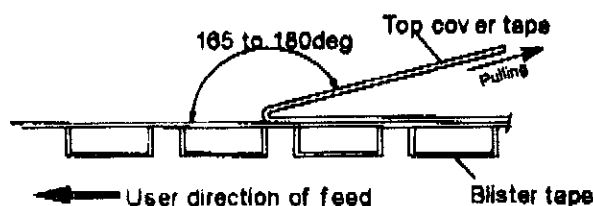
Gr.		A		B		C		D								
REMARKS			PROJECTION		SCALE		REGD.		SDTYPE D.D.		CLASS.		MO.		WORK SPEC. No.	
H9908010NS					NTS								M			
DWG.				TITLE		Hitachi, Ltd. Tokyo Japan		Semiconductor & Integrated Circuits Division		SH.		12		345		
CHD.		PF08109B-TB CAS														
APP.																

4. Outer box



5. Pulling force

- 1) The peel angle for cover tape shall be: 165 to 180 deg.
- 2) The force and pulling speed on the cover tape shall be: 0.10 to 1.3N for 300 mm/min.
- 3) The tape break force and Top cover tape strength: 10N min.



6. Quantity

- 1) 1500 pcs. of modules are put into a anti-static cover tape par reel.
- 2) One reel is packed into a carton box.

Gr.	A	B	C	D
REMARKS	PROJECTION	SCALE	REGD.	SDTYPE D.D.
H9908010NS		NTS		
D.W.N.				
C.H.O.				
RE REGD.				
TITLE		Hitachi, Ltd.		SH.
PF08109B-TB CAS		Tokyo Japan		13
		Semiconductor & Integrated Circuits Division		E
		345		

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

The product ID explanation of the material combination of the PF08109B

The PF08109B will be produced with Aluminum or Gold boning wire with the substrate from two sources to increase the security of the production of this product.

The bonding material and substrate type combinations are three. The aluminum or gold bonding wire with the substrate (type B) and the gold bonding wire with the substrate (type R).

The electrical performance of those three types will be the same and we will guarantee the same specification for all types of the products.

The product identification and packing identifications are as below.

(1) The product identification

The letter "L" after the cut number indicate the substrate "B" with aluminum wire bonding product.

The letter "U" after the cut number indicate the substrate "B" with gold wire bonding product.

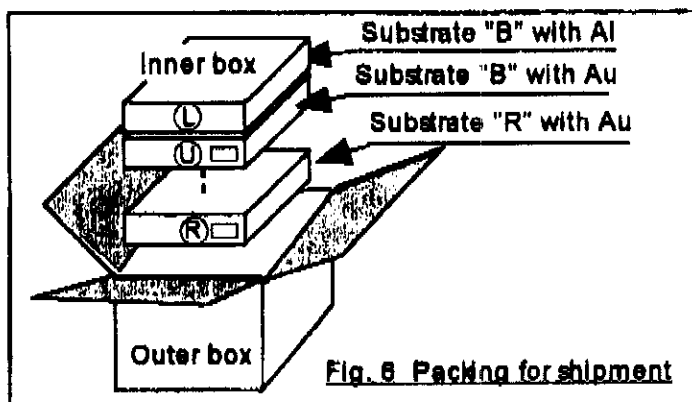
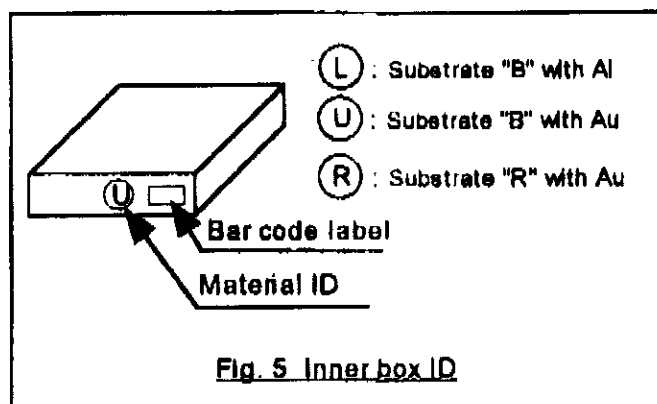
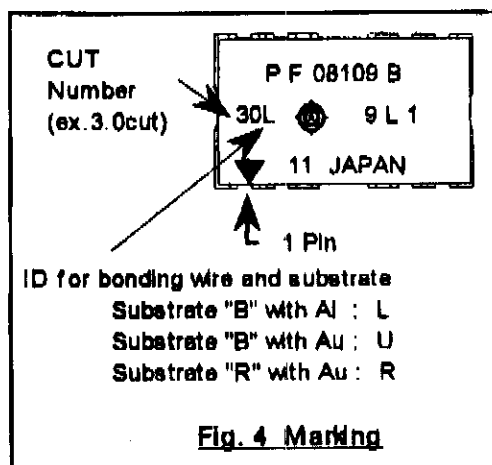
The letter "R" after the cut number indicate the substrate "R" with gold wire bonding product.

Please refer the marking example shown in Fig.4.

(2) The packing identification

The letter "L" or "U" or "R" is marked on inner box as shown in Fig.5.

As shown in Fig.6, it is possible that the either type of the product exists in the same outer box.



Cautions

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