



MMC 4030

QUAD EXCLUSIVE-OR GATE

GENERAL DESCRIPTION

The MMC 4030 is a monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package.

The MMC 4030 consists of four independent Exclusive-OR gates integrated on a single monolithic silicon chip. All inputs and outputs are protected against electrostatic effects.

FEATURES

- MEDIUM-SPEED OPERATION $t_{PLH} = t_{PHL} = 65$ ns (TYP.) AT $C_L = 50$ pF and $V_{DD} = V_{SS} = 10$ V
- LOW OUTPUT IMPEDANCE 500Ω (TYP.) AT $V_{OH} = V_{OL} = 10$ V

APPLICATIONS

- Even and odd-parity generators and checkers
- Logical comparators
- Adders/subtractors
- General logic functions

ABSOLUTE MAXIMUM RATINGS

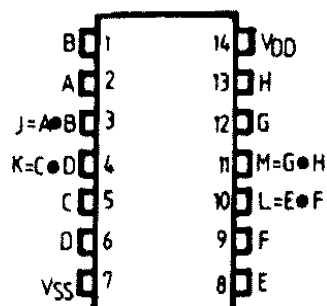
V_{DD}^*	Supply voltage: G and H types	-0.5 to 20	V
	E and F types	-0.5 to 18	V
V_i	Input voltage	-0.5 to $V_{OH} + 0.5$	V
I_i	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for $T_A =$ full package-temperature range	100	mW
T_A	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

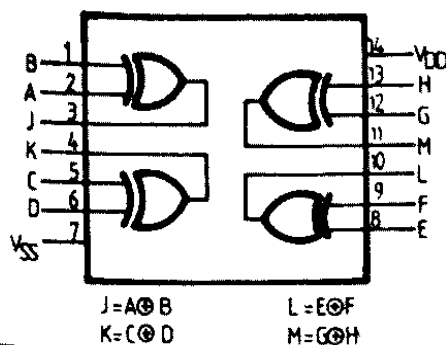
RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types	3 to 18	V
	E and F types	3 to 15	V
V_i	Input voltage	0 to V_{DD}	V
T_A	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



TRUTH TABLE

One of four identical gates

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where "1" = High level
"0" = Low level

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I _L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μ A
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
		0/15			15		16		0.02	16		120		
V _{OH}	Output high voltage		0/ 5 0/10 0/15		< 1 < 1 < 1	5 10 15	4.95 9.95 14.95		4.95 9.95 14.95			4.95 9.95 14.95		V
V _{OL}	Output low voltage		5 /0 10/0 15/0		< 1 < 1 < 1	5 10 15		0.05 0.05 0.05			0.05 0.05 0.05		0.05 0.05 0.05	V
V _{IH}	Input high voltage			0.5/4.5 1/9 1.5/13.5	< 1 < 1 < 1	5 10 15	3.5 7 11		3.5 7 11			3.5 7 11		V
V _{IL}	Input low voltage			4.5/0.5 9/1 13.5/1.5	< 1 < 1 < 1	5 10 15		1.5 3 4			1.5 3 4		1.5 3 4	V
I _{OH}	Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I _{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{II} , I _{IL}	Input leakage current	G, H types	0/18	Any input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A
		E, F types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
C _I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = -55°C for G, H devices, -40°C for E, F devices* T_{HIGH} = +125°C for G, H devices, +85°C for E, F devices

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V2 V min. with V_{DD} = 10 V2.5 V min. with V_{DD} = 15 V

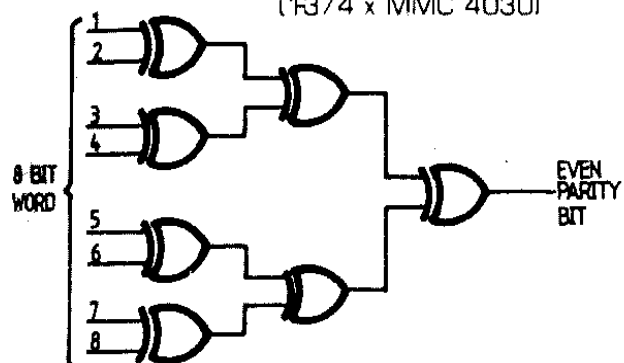
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ kohm}$, typical temperature coefficient for all $V_{DD} = 0.3\%/^\circ\text{C}$ values, all input rise and fall time = 20 ns).

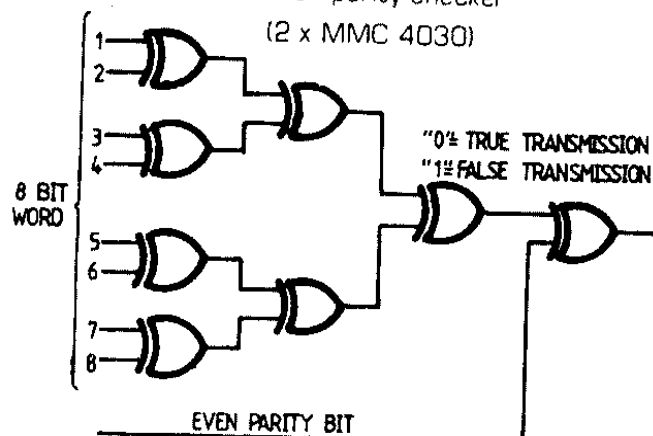
PARAMETER	TEST CONDITIONS	VALUES			UNIT
	V_{DD} (V)	min	typ	max	
t_{PLH} t_{PHL} Propagation delay time	5 10 15		140 65 50	280 130 100	ns
t_{TLH} t_{THL} Transition time	5 10 15		100 50 40	200 100 80	ns

TYPICAL APPLICATIONS

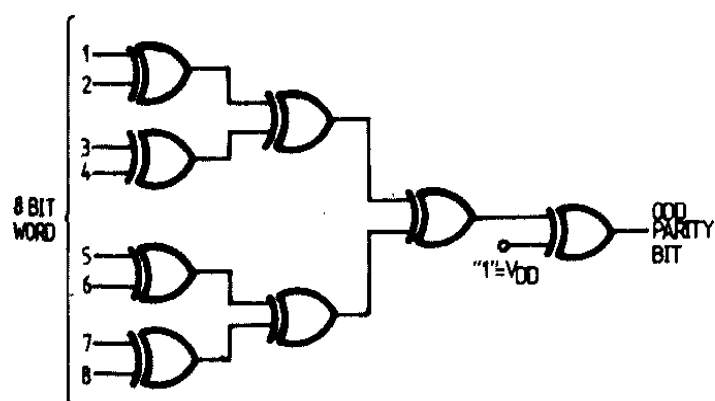
Even-parity-bit generator
(13/4 x MMC 4030)



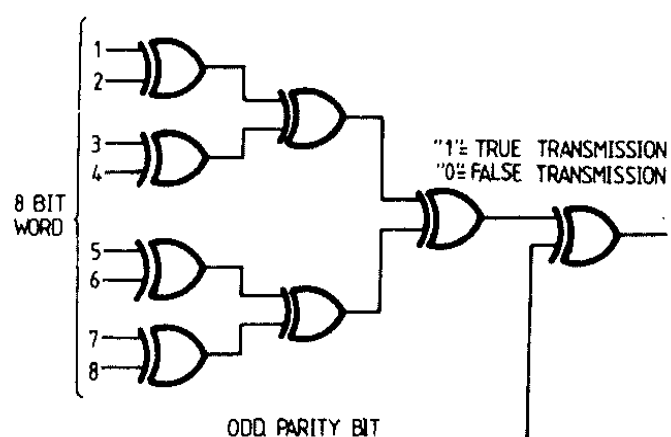
Even-parity checker
(2 x MMC 4030)



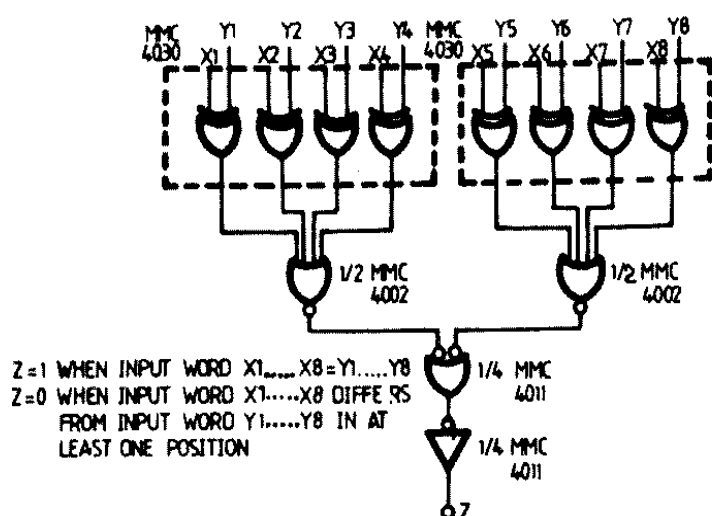
Odd-parity-bit generator
(2 x MMC 4030)



Odd-parity checker
(2 x MMC 4030)



8-bit comparator



8-bit two's complement adder-subtractor

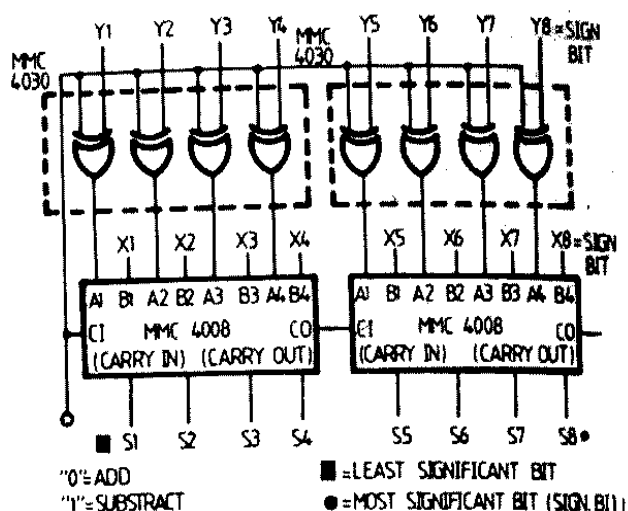


TABLE 1

Two's complement numbers and their equivalent decimal values

X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁		X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	
0	0	0	0	0	0	0	0	= 0	1	1	1	1	1	1	1	1	= - 1
0	0	0	0	0	0	0	1	= 1	1	1	1	1	1	1	0	1	= - 2
0	0	0	0	0	0	1	0	= 2	1	1	1	1	1	1	0	0	= - 3
0	0	0	0	0	0	1	1	= 3	1	1	1	1	1	1	0	0	= - 4
0	1	1	1	1	1	1	0	= 126	1	0	0	0	0	0	0	1	= - 127
0	1	1	1	1	1	1	1	= 127	1	0	0	0	0	0	0	0	= - 128

The two's complement adder-subtractor can add or subtract any two of the numbers in TABLE 1

For example

a)

2	SIGN																
+	= BIT																
- 5	X	0	0	0	0	0	1	0									
- Y		1	1	1	1	1	0	1									
CI								0									
S	0	1	1	1	1	1	0	1									
CO																	

= 3

b)

- 2	SIGN																
- = X	BIT																
- 5	Y	1	1	1	1	1	1	0									
- Y		1	1	1	1	1	0	1									
CI		0	0	0	0	0	1	0									
S	1	0	0	0	0	0	1	1									
CO																	

= 3