Integrated Device Technology, Inc.

T-52-07

RISC CPU WRITE BUFFER

IDT79R3020

FEATURES:

- Temporary storage buffers to enhance the performance of the IDT79R3000 RISC CPU processor
- Allows for write operations by the RISC CPU processor during Run cycles
- Each Write Buffer has four locations to handle an 8-bit address slice and a 9-bit data slice (including a parity bit)
- High-speed CEMOS™ technology
- Pin, functionally and software compatible with the MIPS Computer Systems R2020 Write Buffer
- Speeds from 16.7 to 40 MHz
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT79R3020 Write Buffer enhances the performance of IDT79R3000 systems by allowing the processor to perform write operations during Run cycles instead of resorting to time-consuming stall cycles. Each IDT79R3020 device handles an 8-bit slice of address, and a 9-bit slice of data (one parity bit per byte); thus, four IDT79R3020s provide 4-deep buffering of 32 bits of address and 36 bits of data and parity. Figure 1 illustrates the functional position of the Write Buffer in an IDT79R3000 system.

Whenever the processor performs a write operation, the Write Buffer captures the output data and its address (including the access type bits). The Write Buffer can hold up to four data–address sets while it waits to pass the data on to main memory. Transfers from the processor to the write buffers occur synchronously at the cycle rate of the processor and the write buffer signals the processor if it is unable to accept data. The write buffer also provides a set of handshake signals to communicate with a main memory controller and coordinate the transfer of write data to main memory.

The sections that follow describe these IDT79R3020 Write Buffer interfaces:

- the processor-Write Buffer interface
- the Write Buffer-main memory interface
- a miscellaneous, Write Buffer-board control interface.

WRITE BUFFER

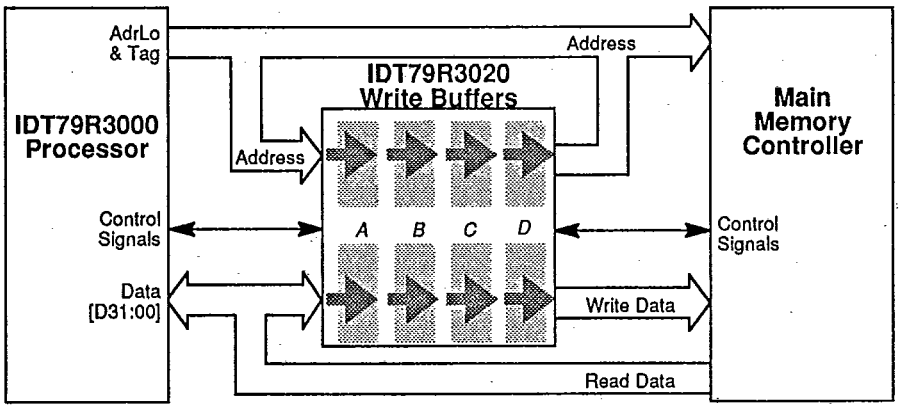

Figure 1. The IDT79R3020 Write Buffer in an IDT79R3000 System

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WRITE BUFFER - IDT79R3000 PROCESSOR INTERFACE

Figure 2 shows the signals comprising the Write Buffer interface to the IDT79R3000 (all descriptions assume that four IDT79R3020 Write Buffers are used to implement a 32-bit, buffered interface). The AdrLo bus and Tag bus bits from the processor are both connected to the Write Buffer to form a 32-bit physical address that is captured by the buffers. Thirty-two bits of data, four bits of parity, and two access type bits are also captured by the Write Buffer. The paragraphs that follow describe the Write Buffer-processor interface signals and the timing of processor-to-Write Buffer data transfers.

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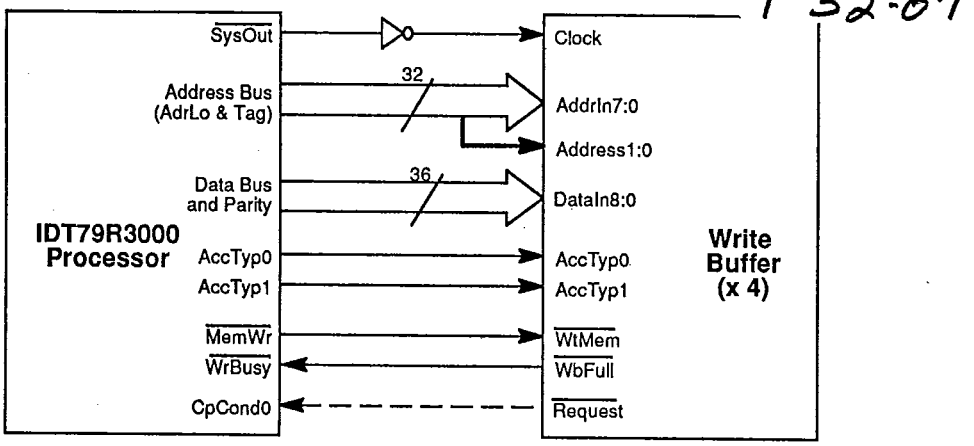

Figure 2. Write Buffer — IDT79R3000 Processor Interface

Write Buffer-Processor Interface Signals

Clock

An inverted version of the IDT79R3000's SysOut signal from the IDT79R3000 processor that synchronizes data transfers. The Write Buffer uses the trailing edge of *Clock* to latch the contents of the AdrLo bus and uses the leading *Clock* edge to latch the contents of the Data and Tag buses.

DataIn8:0

Nine input data lines from the IDT79R3000 processor's Data bus (eight bits of data and one bit of parity).

AddrIn7:0

Eight input address lines from the IDT79R3000 processor. The address lines are taken from the AdrLo and Tag buses.

Address1:0

The two least significant address bits from the IDT79R3000 processor. These two address bits must be connected to all four Write Buffers and are used in conjunction with the access type (*AccTyp1:0*) signals, the *Position1:0* signals, and the *BigEndian* signal to determine which byte(s) in a word are being written into a particular Write Buffer.

AccTypIn1:0

The access type signals from the IDT79R3000 processor specifying the size of a data access: word, tri-byte, half-word, or byte.

WtMem

This input is connected to the MemWr signal from the IDT79R3000 processor that is asserted whenever the processor is performing a store (write) operation.

Request

The primary purpose of this signal is to request access to memory and is described later when the Write Buffer-Main Memory Interface is discussed. The Request signal can also be connected to the CpCond0 input of the IDT79R3000 and can then be tested by software to determine if there is any data in the Write Buffer. Since Request is deasserted if there is no data in the Write Buffer, software can determine if a previous write operation (for example, to an I/O device) has been completed before initiating a read or read status operation from that device.

WbFull

The Write Buffer asserts this signal to the IDT79R3000's WrBusy input whenever it cannot accept any more data; that is, when the current write will fill the buffer or the buffer has all address-data pairs occupied. The IDT79R3000 processor performs a write-busy stall if it needs to store data while the WbFull/WrBusy signal is asserted.

Data & Address Connections

Figure 3 illustrates how four Write Buffers are connected to the address and data outputs of the IDT79R3000 processor.

Address Inputs

Each Write Buffer device has eight address inputs (AdrIn7:0). The four low-order bits (AdrIn3:0) are clocked into the device on the trailing edge of the Clock signal and are taken from the IDT79R3000's AdrLo bus. The four high-order bits (AdrIn7:4) are clocked into the device on the rising edge of the Clock signal and are taken from the IDT79R3000's Tag bus.

Each device also has separate inputs (Address1, Address0) for the two low-order bits from the AdrLo bus. These bits must be input to each device since they comprise the byte pointer. Note in Figure 3 that the two low-order AdrIn inputs (AdrIn1:0) to Write Buffer device 0 are connected to ground since the Address1, Address0 inputs already supply these bits to the device.

Data Inputs

Each Write Buffer device has nine data inputs that are clocked into the device on the leading edge of the Clock signal and are taken from the IDT79R3000's Data bus. In Figure 3, each device captures eight bits of data and one bit of parity. Also note that the data bits assigned to each device correspond to the address bits connected to the device. This arrangement is required since data

selection is dependent on a combination of the AccType signals and the two low order address bits. The arrangement also simplifies system utilization of the "Read Error Address" feature described later.

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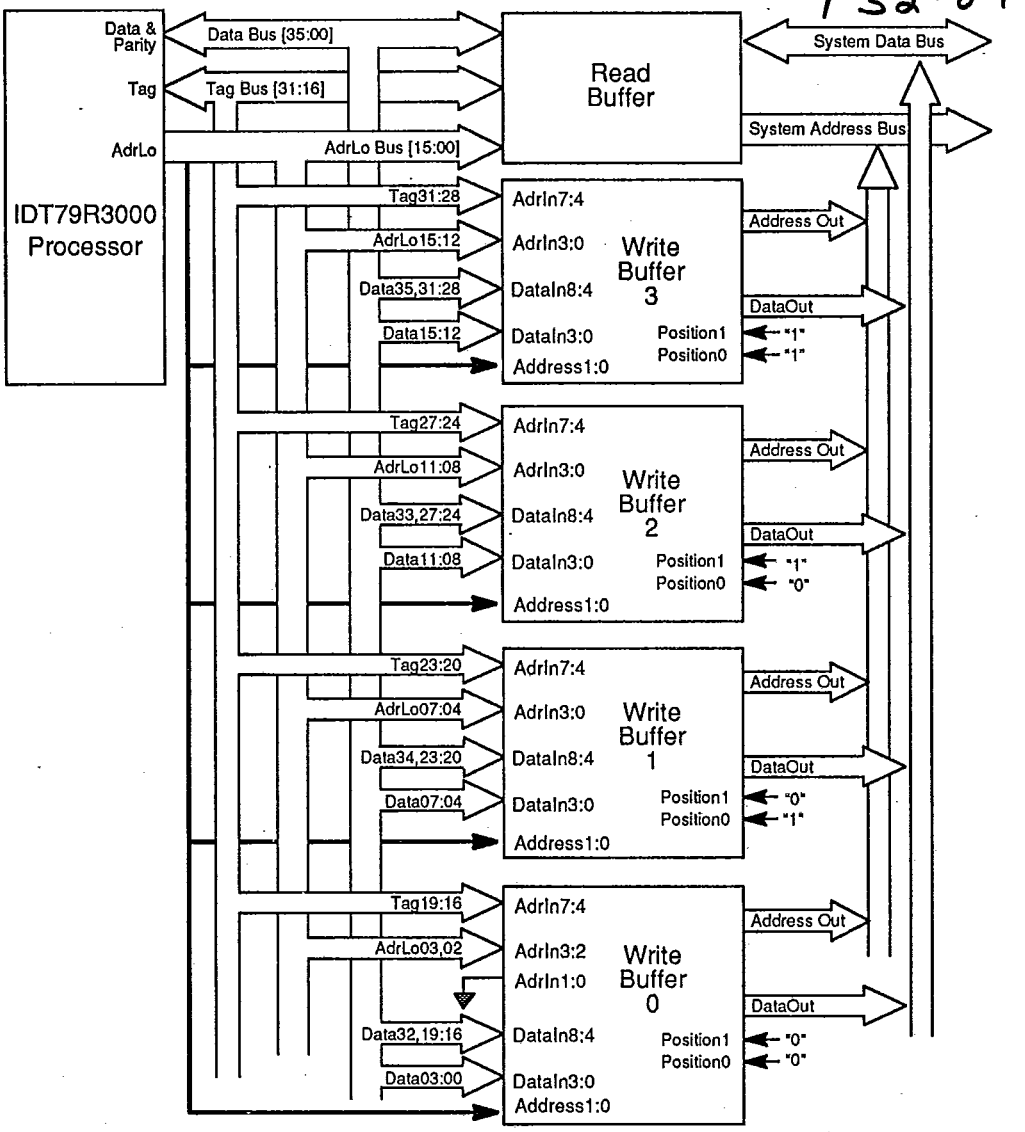

Figure 3. Write Buffer Data and Address Line Connections

The *Position1* and *Position0* signals shown in Figure 3 specify the nibble position within a halfword that each write buffer device comprises.

Write Buffer - Processor Timing

Transfers between the processor and the Write Buffers occur synchronously: the Clock signal from the processor is input to the Write Buffers and used to clock the address and data information into the Write Buffers' latches. Figure 4 illustrates the timing for the processor-Write Buffer interface.

When the WrtMem signal is asserted, the low-order address bits, and the Address 1:0 inputs, are latched on the trailing edge of the Clock signal (1). The rising edge of Clock (2) is used to latch the high-order address bits, the access type inputs and the contents of the data bus.

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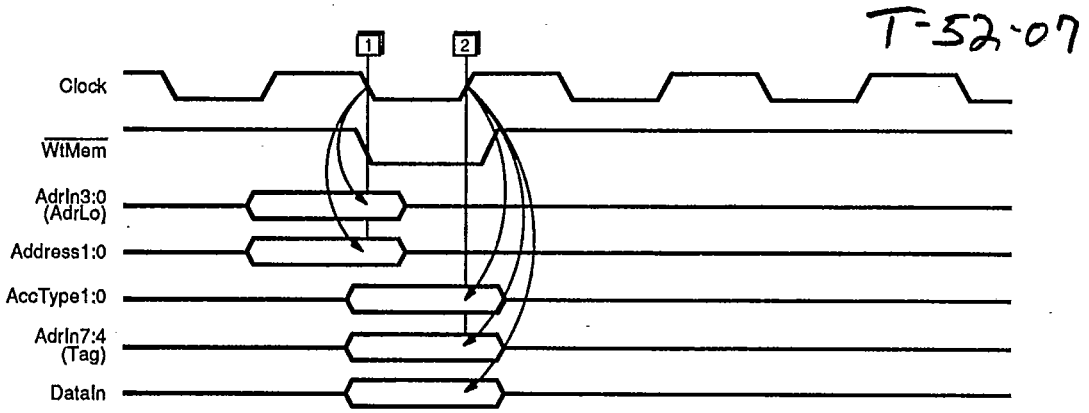

Figure 4. Processor — Write Buffer Interface Timing

WRITE BUFFER - MAIN MEMORY INTERFACE

Figure 5 shows the signals comprising the Write Buffer interface to main memory. This interface is essentially decoupled from the Write Buffer-processor interface: although some synchronization of the memory interface signals and the Clock signal is required, the handshaking signals in this interface have no direct connection to the operation of the Write Buffer-processor interface.

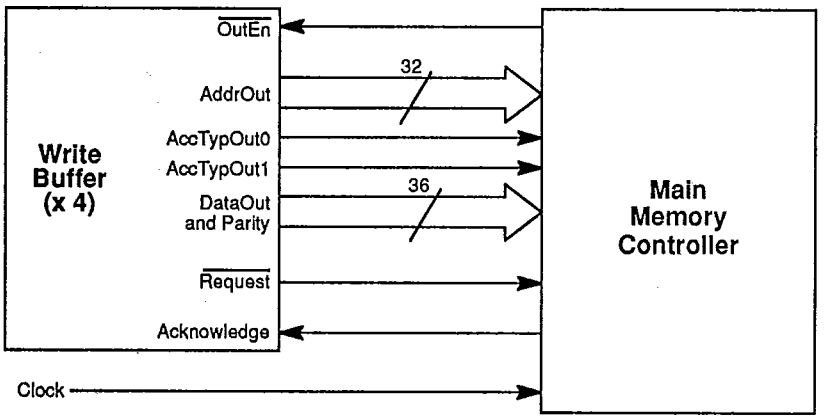

Figure 5. Write Buffer — Main Memory Interface

Write Buffer - Main Memory Interface Signals

Each Write Buffer provides the following signals that comprise the interface to a main memory controller:

AddrOut 7:0
Eight address line output from each Write Buffer.

DataOut 8:0
Nine data lines from each Write Buffer (eight bits of data and one bit of parity).

AccTypOut 1:0
The access type signals from the Write Buffer specifying the size of a data access: word, tri-byte, half-word, or byte.

$\overline{\text{OutEn}}$
The memory controller asserts this write input to enable the tri-state outputs of the IDT79R3020 address and data signals.

$\overline{\text{Request}}$
The Write Buffer asserts this signal to inform the main memory system that it has data to be written to memory.

Acknowledge
The main memory system asserts this signal when it has captured the data presented by the Write Buffer on the DataOut lines.

Write Buffer - Main Memory Interface Timing

Figure 6 illustrates the timing for the transfer of data from the Write Buffer to the main memory system. The sequence illustrated in this figure is as follows:

1) When the Write Buffer has a data-address pair for transfer to the memory system, it asserts the Request signal.
2) When memory system is ready to handle the Write Buffer data, it asserts the OutEn signal to enable the Write Buffers' address and data outputs onto the system buses.
3) When memory system no longer requires the Write Buffer address and data outputs, it asserts the Acknowledge signal. The Write Buffer responds to this signal by discarding the address-data pair that was just output.
4) The memory system can deassert the OutEn signal to return the Write Buffers' address and data outputs to their tri-state condition.
5) Since the Request signal remains asserted, the memory system asserts the OutEn signal again to enable the next address-data pair onto the system buses.
6) When memory system has accepted the second address-data pair, it again asserts the Acknowledge signal. If the Write Buffer is now empty, it responds to this signal by deasserting the Request signal.

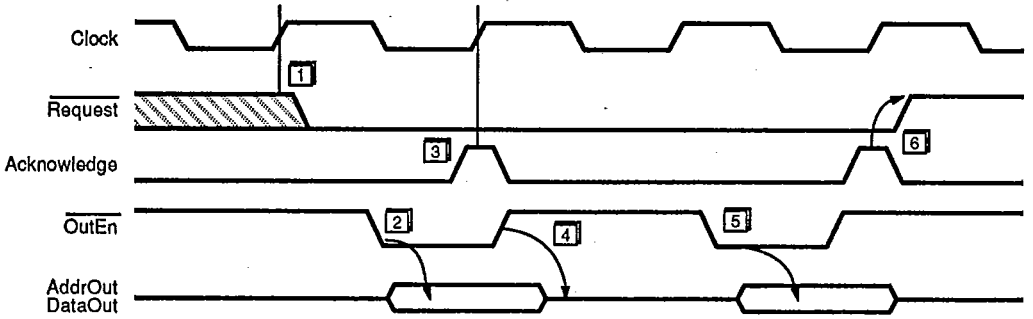

Figure 6. Write Buffer — Main Memory Interface Timing

Note that the buffer's interface to main memory is not completely asynchronous: assertion of the Request signal by the Write Buffer is synchronized with the rising edge of Clock, and the Acknowledge signal input by main memory has a minimum set up and hold time in relation to the Clock signal.

MISCELLANEOUS WRITE BUFFER - BOARD LOGIC INTERFACE

The Write Buffers support several functions that utilize signals that do not fit neatly into the descriptions of either the processor or main memory interfaces. These functions and signals typically involve miscellaneous logic on a CPU board and include the following:

- byte gathering
- configuration connections (Big Endian, Position 1:0)
- address matching logic
- error address latch logic

The sections that follow describe each of these categories.

Byte Gathering

The Write Buffers perform byte (half-word, tri-byte and word) gathering to decrease the number of write transfers to same location; that is, sequential writes to the same WORD address have their data combined into the same address-data pair buffer.

Byte gathering is prohibited in the address-data pair that is currently available to the memory controller. Thus, the first write into an empty Write Buffer will not have subsequent writes gathered into it because it is currently available for output to memory. Writes to the same location (byte) may be overwritten in the Write Buffer if the gathering is not prohibited by the preceding rule.

The Write Buffers present address-data pairs to the main memory controller in the sequence in which they were received from the processor except in the case of gathered data, where bytes or half words can be collected and written to main memory in a single write operation. If the address-data pair buffer is scheduled to be output, then gathering is inhibited and the buffer contents are presented to the main memory controller. Subsequent writes are then placed in another buffer. No reliance should be placed in any aspect of gathering (except that it only involves sequential writes to the same word address) as it is not readily deterministic. Non-sequential writes to the same word address are not gathered.

Note that gathering can require that two main memory controller references be used to empty a single Write Buffer entry. For example, this can occur if Bytes 0 and 3 of a word are sequentially written. Where order in writing is important, such as in I/O controllers, software should avoid sequential accesses to the same word. In cases where write-read access ordering is important but reading of the write location is not desired, such as during I/O, then a write followed by a write to a dummy location followed by a read of the dummy location will insure the first write has occurred before continuing. Alternatively, the Request signal can be tested to determine that the Write Buffer is empty.

Configuration Logic Connections

Because of their byte gathering capability, each buffer device internally maintains a record of each valid byte in an address/data pair. To do this, each device must have a way of determining which data bits within a word it is handling. The following signals determine how the write buffers handle data that is written to the devices:

- **Position 1, Position 0** - these signals (in conjunction with BigEndian) determine how each Write Buffer decodes the Address 1/0 and AccType 1/0 to determine if it should store the data inputs. Refer to Figure 3 for an illustration of how data bits are assigned to Write Buffer devices based on their *position.*
- BigEndian - When asserted, byte 0 is the leftmost, most significant byte (big-endian): when deasserted, byte 0 is the rightmost, least-significant byte (little-endian).
- **Address 1, Address 0** - these signals (taken from the AdrLo bus) must be connected to all buffer devices since they determine which byte within a word is being accessed.

- **AccType 1, AccType 0** - these inputs signals specify the data size of a write operation as shown in Table 1.

Table 1 shows how these signals operate to specify how bytes are saved within the Write Buffers.

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Access Type 1 0	Address 1 0	Bytes Accessed Big–Endian 31 … 0	Bytes Accessed Little–Endian 31 … 0
1 1 (word)	0 0	0 1 2 3	3 2 1 0
1 0 (triple–byte)	0 0	0 1 2	2 1 0
	0 1	1 2 3	3 2 1
0 1 (halfword)	0 0	0 1	1 0
	1 0	2 3	3 2
0 0 (byte)	0 0	0	0
	0 1	1	1
	1 0	2	2
	1 1	3	3

Table 1. Byte Specifications for Write Operations

The lower two address bits of the device in position zero (as determined by the two POSITION inputs) are inhibited; that is, they are not stored directly as they are output on the AdrLo bus. Instead, on output, the lower two address bits are generated from the indication of the positions of the valid data bytes as determined by above table.

MatchOut/MatchIn Logic and Read Conflicts

Whenever the processor references main memory (either a write or a read reference), the Write Buffers compare the word address from the CPU with the word addresses stored in the buffers. If any word address matches, the buffers assert signals that can be used by the main memory controller to ensure that the Write Buffer is emptied before the read access with the conflicting address has been performed.

Figure 7 illustrates the Write Buffer signals involved in address comparison logic. Each write buffer provides four output signals (MatchOut A, B, C, and D) which correspond to the four buffer ranks (A, B, C, D) in each device as shown in Figure 1. These MatchOut signals can be externally NANDed as shown in Figure 7 to determine if the address being input matches those in any rank of the Write Buffer.

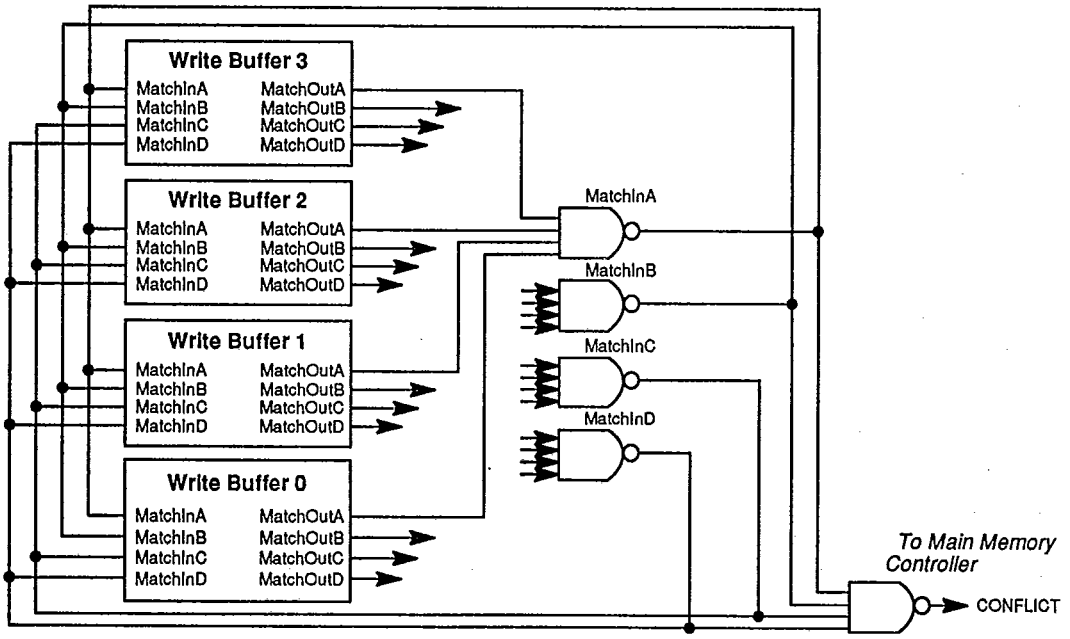

Figure 7. Write Buffer MatchOut/MatchIn Logic

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The outputs of the NAND gates are fed into Write Buffers via the MatchIn A, B, C, and D signals and are used within each device as part of the byte gathering logic. The NAND gate outputs can be NANDed together as shown in Figure 7 with the resultant signal used (in conjunction with the processor's $\overline{\text{MEMRD}}$ signal) to alert the main memory controller logic that there is a pending buffered write that conflicts with a just-issued read. The main memory controller can then delay the read access until the Request signal is deasserted indicating that the Write Buffer has been emptied.

Error Address Latch

The write buffer incorporates an internal latch that can be loaded with one of the buffered addresses and subsequently enabled out onto the data lines. This feature can be used by error handling routines to read an address back from the Write Buffer and analyze or recover from certain bus errors. Figure 8 shows the signals involved in operation of this latch.

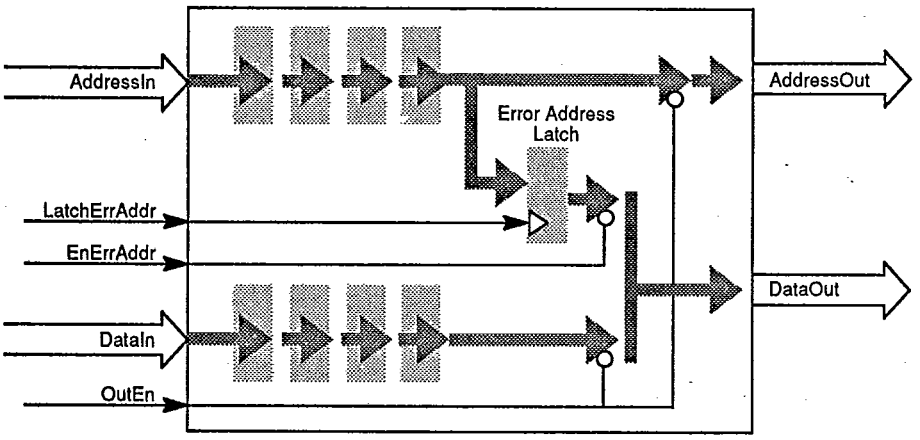

Figure 8. The Write Buffer Error Address Latch

When the LatchErrAddr signal is asserted, the address currently available to the address outputs of the Write Buffer is latched into the internal latch. This address can then be output on the DataOut lines by asserting the EnErrAdr signal so that the processor can read the address in as data. Refer to the AC specifications for timing parameters of the signals associated with the error address latch.

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ABSOLUTE MAXIMUM RATINGS(1, 3)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature(2)	–55 to +125	–65 to +150	°C
V_{IN}	Input Voltage	–0.5 to +7.0	–0.5 to +7.0	V

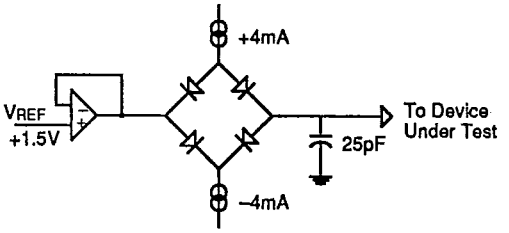
NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	Vcc
Military	–55°C to +125°C	0V	5.0 ± 10%
Commercial	0°C to +70°C	0V	5.0 ± 5%

OUTPUT LOADING FOR AC TESTING



DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0 V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	33.33MHz MIN.	33.33MHz MAX.	40 MHz MIN.	40 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	—	2.4	V
V_{IH}	Input HIGH Voltage(1)		2.4	—	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{IL}	Input LOW Voltage(2)		—	0.8	—	0.8	—	0.8	—	0.8	—	0.8	V
C_{IN}	Input Capacitance		10	—	10	—	10	—	10	—	10	—	pF
C_{OUT}	Output Capacitance		10	—	10	—	10	—	10	—	10	—	pF
I_{CC}	Operating Current	V_{CC} = Max	—	50	—	60	—	70	—	80	—	90	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	—	10	—	10	—	10	—	10	—	10	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–10	—	–10	—	–10	—	–10	—	–10	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	–40	40	–40	40	–40	40	µA

DC ELECTRICAL CHARACTERISTICS — MILITARY TEMPERATURE RANGE (T_A = –55°C to +125°C, V_{CC} = +5.0 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	33.0 MHz MIN.	33.0 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(1)		2.4	—	2.4	—	2.4	—	2.4	—	V
V_{IL}	Input LOW Voltage(2)		—	0.8	—	0.8	—	0.8	—	0.8	V
C_{IN}	Input Capacitance		10	—	10	—	10	—	10	—	pF
C_{OUT}	Output Capacitance		10	—	10	—	10	—	10	—	pF
I_{CC}	Operating Current	V_{CC} = Max	—	50	—	60	—	70	—	80	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	—	10	—	10	—	10	—	10	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–10	—	–10	—	–10	—	–10	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	–40	40	–40	40	µA

NOTES:

1. V_{IH} should be held above V_{CC} + 0.5 Volts.
2. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for longer periods.

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE (T_A + 0°C to 70°C, V_{CC} = +5.0V ± 5%)

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SYMBOL	PARAMETER	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	33.33 MHz MIN.	33.33 MHz MAX.	40.0 MHz MIN.	40.0 MHz MAX.	UNIT
t1	Addrin (3:0) to Clock falling setup	8	—	7	—	6	—	3	—	3	—	ns
t2	Addrin (3:0) from Clock falling hold	4	—	4	—	4	—	3	—	3	—	ns
t3	Address 1:0 to Clock falling setup	8	—	7	—	6	—	3	—	3	—	ns
t4	Address 1:0 from Clock falling hold	4	—	4	—	4	—	3	—	3	—	ns
t5	Access Type 1:0 to Clock rising setup	7	—	6	—	5	—	4	—	4	—	ns
t6	Access Type 1:0 from Clock rising hold	3	—	3	—	2	—	2	—	2	—	ns
t7	Addrin (7:4) to Clock rising setup	7	—	5	—	4	—	4	—	4	—	ns
t8	Addrin (7:4) from Clock rising hold	3	—	3	—	2	—	1	—	1	—	ns
t9	DataIn (8:0) to Clock rising setup	7	—	5	—	4	—	4	—	4	—	ns
t10	DataIn (8:0) from Clock rising hold	3	—	3	—	2	—	1	—	1	—	ns
t11	$\overline{\text{WrtMem}}$ to Clock rising setup	10	—	8	—	7	—	6	—	6	—	ns
t12	$\overline{\text{WrtMem}}$ from Clock rising hold	6	—	5	—	4	—	3	—	3	—	ns
t13	Request from Clock rising	—	32	—	30	—	22	—	16	—	16	ns
t14	Acknowledge to Clock rising setup	12	—	11	—	6	—	4	—	4	—	ns
t15	Acknowledge from Clock rising hold	7	—	6	—	5	—	3	—	3	—	ns
t16	LatchErrAdr to Acknowledge rising	5	—	5	—	5	—	3	—	3	—	ns
t17	$\overline{\text{WbFull}}$ active from Clock rising	—	21	—	19	—	17	—	9	—	9	ns
t18	$\overline{\text{WbFull}}$ inactive from Clock rising	—	21	—	19	—	11	—	9	—	9	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	2	15	2	15	2	15	2	12	2	12	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	2	15	2	15	2	15	2	12	2	12	ns
t21	MatchOut (ABCD) from Clock rising	—	24	—	22	—	20	—	15	—	15	ns
t22	MatchIn (ABCD) to Clock rising setup	10	—	9	—	8	—	5	—	5	—	ns
t23	MatchIn (ABCD) from Clock rising hold	3	—	3	—	3	—	3	—	3	—	ns
t24	$\overline{\text{EnErrAdr}}$ to Data (error latch) valid	2	15	2	15	2	15	2	15	2	15	ns
t25	$\overline{\text{EnErrAdr}}$ to Data (error latch) tri-state	2	15	2	15	2	15	2	15	2	15	ns
t26	Address/Data out from Clock rising	—	30	—	27	—	24	—	16	—	16	ns
t27	$\overline{\text{Reset}}$ to Clock rising, set-up	10	—	10	—	10	—	8	—	8	—	ns
t28	$\overline{\text{Reset}}$ from Clock rising, hold	3	—	2	—	1	—	1	—	1	—	ns
t29	Reset low pulse width	8	—	8	—	8	—	8	—	8	—	cycles
t30	$\overline{\text{WbFull}}$ High from Clock rising (after $\overline{\text{Reset}}$)	—	22	—	21	—	20	—	11	—	11	ns
t31	$\overline{\text{Request}}$ High from $\overline{\text{Reset}}$ low	—	20	—	19	—	18	—	16	—	16	ns
t32	Access TypOut 1:0 low from $\overline{\text{Reset}}$ low	—	28	—	26	—	25	—	23	—	23	ns
t33	Match Out (ABCD) Low from $\overline{\text{Reset}}$ low	—	21	—	20	—	20	—	15	—	15	ns
t34	Address/Data out tri-state from $\overline{\text{Reset}}$ low (OutEn negated)	—	32	—	30	—	27	—	23	—	23	ns
t35	Access TypeOut from Clock rising	—	32	—	30	—	27	—	23	—	23	ns
tcyc	Clock Pulse Width	60	2000	50	2000	40	2000	30	2000	25	2000	ns
tckhigh	Clock High Pulse Width	24	—	20	—	16	—	12	—	10	—	ns
tcklow	Clock Low Pulse Width	24	—	20	—	16	—	12	—	10	—	ns

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AC ELECTRICAL CHARACTERISTICS — MILITARY TEMPERATURE RANGE (T_A + –55°C to 125°C, V_{CC} = +5.0V ± 10%)

SYMBOL	PARAMETER	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	33.0 MHz MIN.	33.0 MHz MAX.	UNIT
t1	Addrin (3:0) to Clock falling setup	8	—	7	—	6	—	3	—	ns
t2	Addrin (3:0) from Clock falling hold	4	—	4	—	4	—	3	—	ns
t3	Address 1:0 to Clock falling setup	8	—	7	—	6	—	3	—	ns
t4	Address 1:0 from Clock falling hold	4	—	4	—	4	—	3	—	ns
t5	Access Type 1:0 to Clock rising setup	7	—	6	—	5	—	4	—	ns
t6	Access Type 1:0 from Clock rising hold	3	—	3	—	2	—	2	—	ns
t7	Addrin (7:4) to Clock rising setup	7	—	5	—	4	—	4	—	ns
t8	Addrin (7:4) from Clock rising hold	3	—	3	—	2	—	1	—	ns
t9	DataIn (8:0) to Clock rising setup	7	—	5	—	4	—	4	—	ns
t10	DataIn (8:0) from Clock rising hold	3	—	3	—	2	—	1	—	ns
t11	$\overline{\text{WrtMem}}$ to Clock rising setup	10	—	8	—	7	—	6	—	ns
t12	$\overline{\text{WrtMem}}$ from Clock rising hold	6	—	5	—	4	—	3	—	ns
t13	Request from Clock rising	—	32	—	30	—	22	—	16	ns
t14	Acknowledge to Clock rising setup	12	—	11	—	6	—	4	—	ns
t15	Acknowledge from Clock rising hold	7	—	6	—	5	—	3	—	ns
t16	LatchErrAdr to Acknowledge rising	5	—	5	—	5	—	3	—	ns
t17	$\overline{\text{WbFull}}$ active from Clock rising	—	21	—	19	—	17	—	9	ns
t18	$\overline{\text{WbFull}}$ inactive from Clock rising	—	21	—	19	—	11	—	9	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	2	15	2	15	2	15	2	12	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	2	15	2	15	2	15	2	12	ns
t21	MatchOut (ABCD) from Clock rising	—	24	—	22	—	20	—	15	ns
t22	MatchIn (ABCD) to Clock rising setup	10	—	9	—	8	—	5	—	ns
t23	MatchIn (ABCD) from Clock rising hold	3	—	3	—	3	—	3	—	ns
t24	$\overline{\text{EnErrAdr}}$ to Data (error latch) valid	2	15	2	15	2	15	2	15	ns
t25	$\overline{\text{EnErrAdr}}$ to Data (error latch) tri-state	2	15	2	15	2	15	2	15	ns
t26	Address/Data out from Clock rising	—	30	—	27	—	24	—	16	ns
t27	$\overline{\text{Reset}}$ to Clock rising, set-up	10	—	10	—	10	—	8	—	ns
t28	$\overline{\text{Reset}}$ from Clock rising, hold	3	—	2	—	1	—	1	—	ns
t29	$\overline{\text{Reset}}$ low pulse width	8	—	8	—	8	—	8	—	cycles
t30	$\overline{\text{WbFull}}$ High from Clock rising (after $\overline{\text{Reset}}$)	—	22	—	21	—	20	—	11	ns
t31	$\overline{\text{Request}}$ High from $\overline{\text{Reset}}$ low	—	20	—	19	—	18	—	16	ns
t32	Access TypOut 1:0 low from $\overline{\text{Reset}}$ low	—	28	—	26	—	25	—	23	ns
t33	Match Out (ABCD) Low from $\overline{\text{Reset}}$ low	—	21	—	20	—	20	—	15	ns
t34	Address/Data out tri–state from $\overline{\text{Reset}}$ low (OutEn negated)	—	32	—	30	—	27	—	23	ns
t35	Access TypeOut from Clock rising	—	32	—	30	—	27	—	23	ns
tcyc	Clock Pulse Width	60	2000	50	2000	40	2000	30	2000	ns
tckhigh	Clock High Pulse Width	24	—	20	—	16	—	12	—	ns
tcklow	Clock Low Pulse Width	24	—	20	—	16	—	12	—	ns

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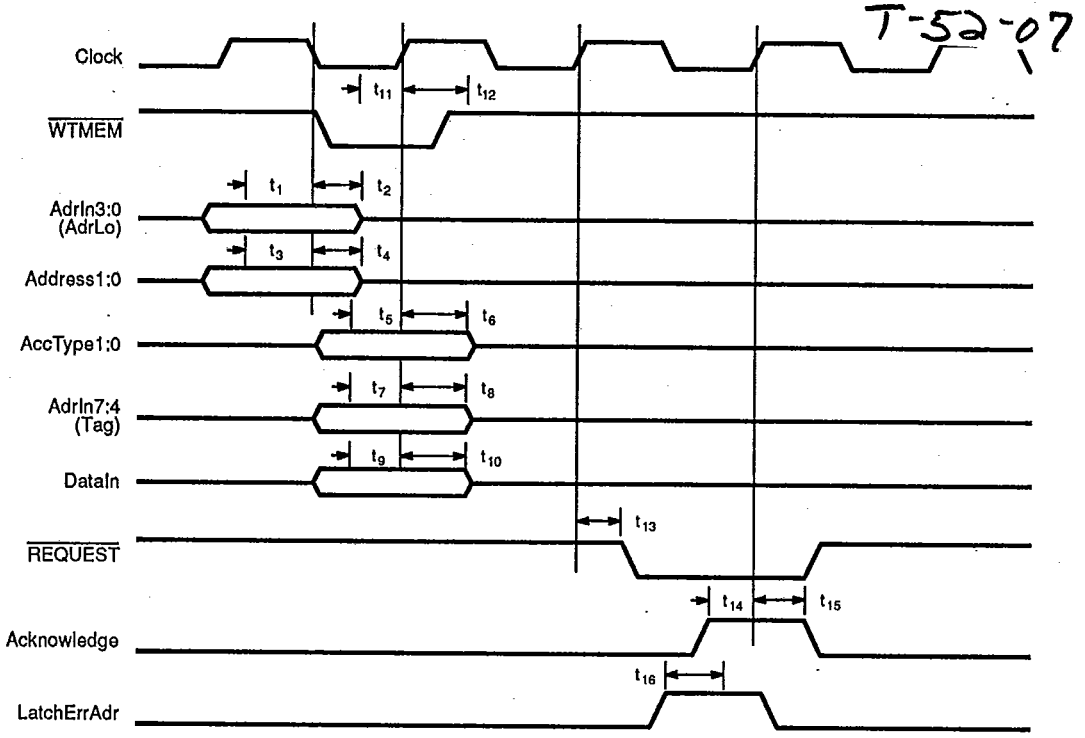

Figure 9. Write Buffer Timing Specifications

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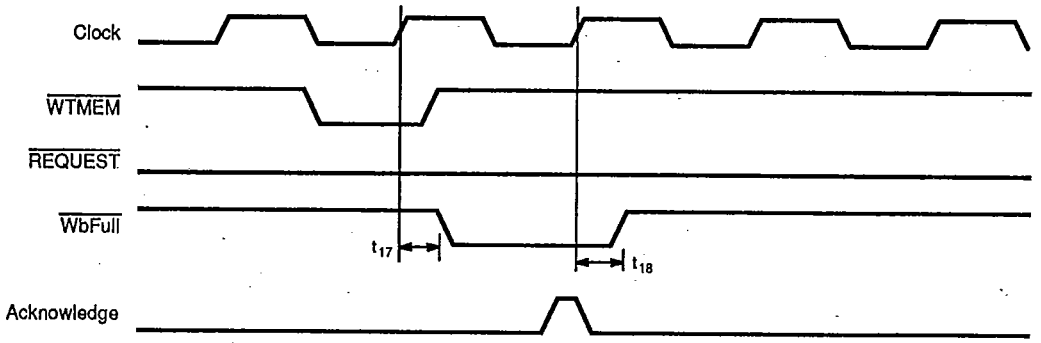

Figure 10. WBFULL Signal Timing Specifications

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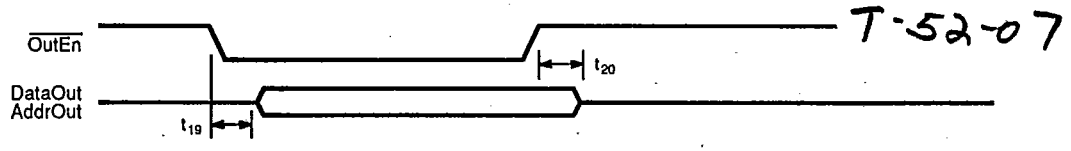

Figure 11. $\overline{\text{OUTEN}}$ Timing Specifications

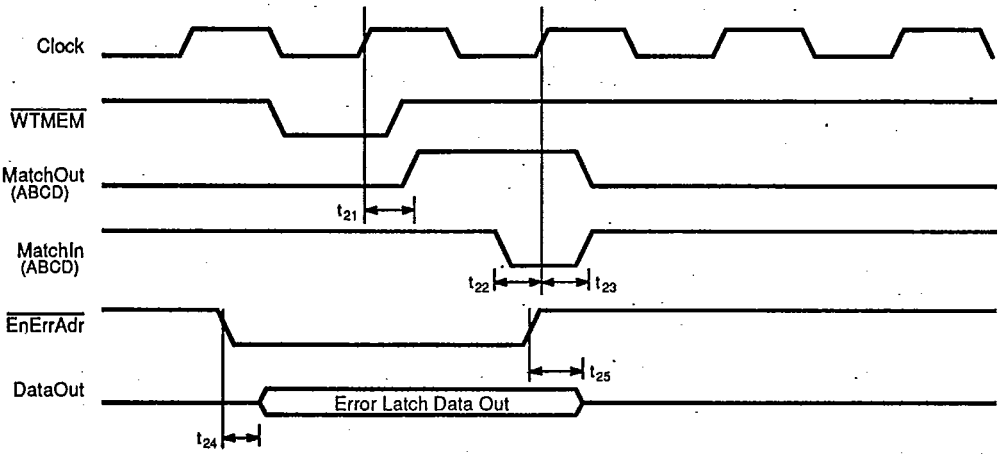

Figure 12. Match and Error Latch Timing Specifications

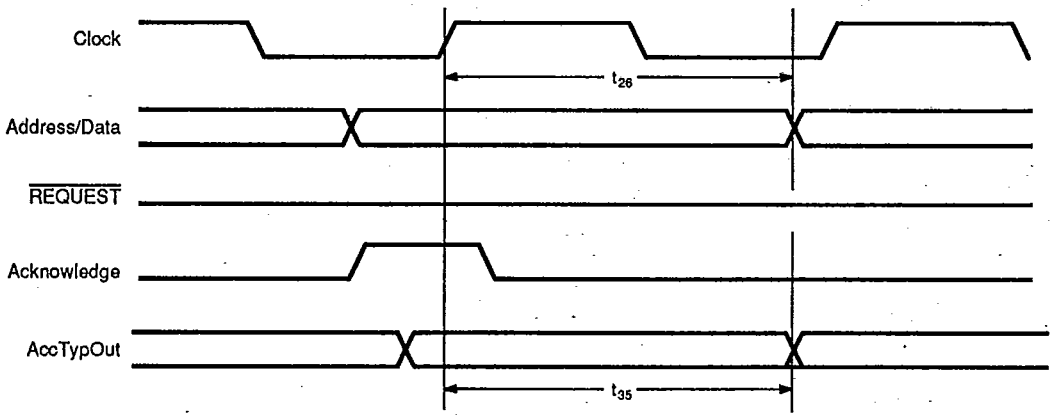

Figure 13. Address/Data Out, Access Type Out

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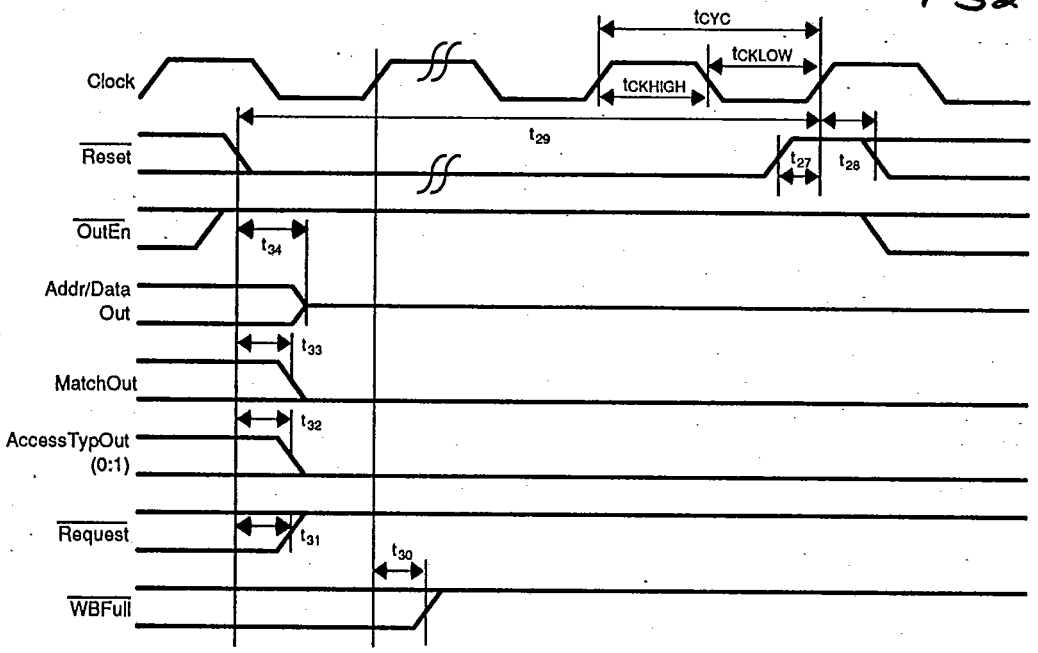

Figure 14. Reset Timing

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68-PIN CPGA FOR R3020
PIN GRID ARRAY (CERAMIC) – BOTTOM VIEW

T-52-07

	1	2	3	4	5	6	7	8	9	10	11
L		ACC-TYPE0	AC-KNOWL-EDGE	AD-DRESS1	CLOCK	DATA-IN0	DATA-IN2	DATA-IN4	DATA-IN6	VCC2	
K	GND1	VCC1	ACC-TYPE1	AD-DRESS0	$\overline{\text{BIG-ENDIAN}}$	$\overline{\text{EN-ERROR-ADR}}$	DATA-IN1	DATA-IN3	DATA-IN5	GND2	DATA-IN7
J	ADDR-OUT5	ADDR-OUT4								DATA-IN8	ADDR-IN0
H	ADDR-OUT3	ADDR-OUT2								ADDR-IN1	ADDR-IN2
G	ADDR-OUT1	ADDR-OUT0								ADDR-IN3	ADDR-IN4
F	DATA-OUT8	DATA-OUT0								ADDR-IN5	ADDR-IN6
E	DATA-OUT1	DATA-OUT2								ADDR-IN7	LATCH-ERR-ADR
D	DATA-OUT3	ADDR-OUT6								MATCH-INA	MATCH-INB
C	ADDR-OUT7	ACC-TYPE OUT1								MATCH-INC	MATCH-IND
B	ACC-TYPE OUT0	GND0	DATA-OUT7	DATA-OUT4	$\overline{\text{RE-QUEST}}$	MATCH-OUTC	MATCH-OUTA	$\overline{\text{RESET}}$	POSITION0	VCC3	GND3
A		VCC0	DATA-OUT5	DATA-OUT6	$\overline{\text{WBFULL}}$	MATCH-OUTD	MATCH-OUTB	$\overline{\text{WTMEM}}$	POSITION1	$\overline{\text{OUTEN}}$	

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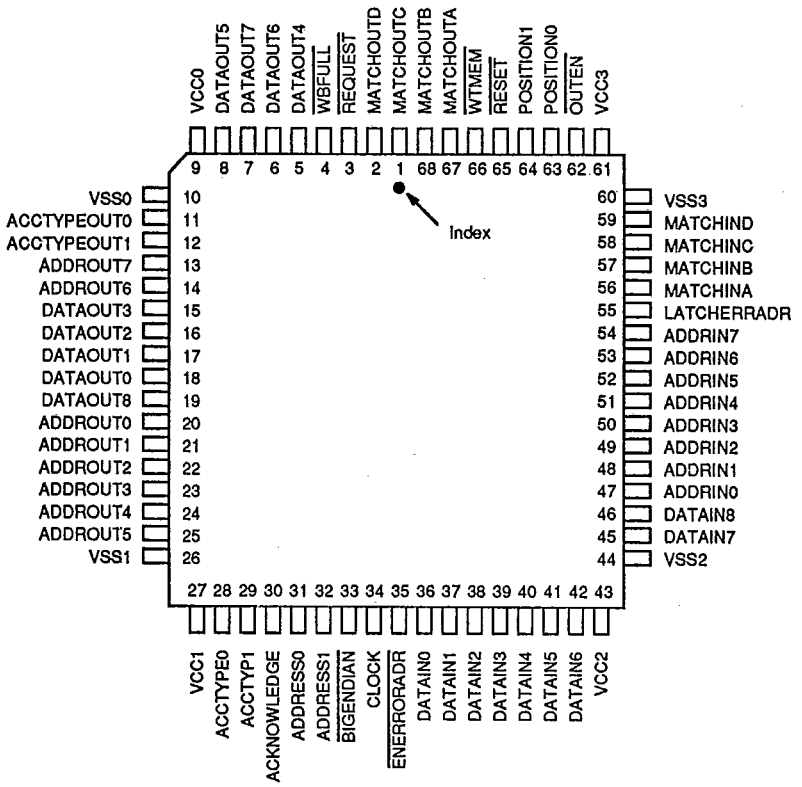
PIN CONFIGURATION
PLASTIC LEADED CHIP CARRIER
(TOP VIEW)



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ORDERING INFORMATION