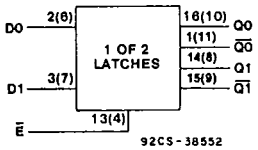
T-46-07-09

CD54/74HC75
CD54/74HCT75

File Number **1666**



Dual 2-Bit Bistable Transparent Latch

Type Features:

- *True and Complementary Outputs*
- *Buffered Inputs and Outputs*

FUNCTIONAL DIAGRAM

The RCA-CD54/74HC75 and CD54/74HCT75 are dual 2-bit bistable transparent latches. Each one of the 2-bit latches is controlled by separate Enable inputs ($\overline{1E}$ and $\overline{2E}$) which are active LOW. When the Enable input is HIGH data enters the latch and appears at the Q output. When the Enable input ($\overline{1E}$ and $\overline{2E}$) is LOW the output is not affected.

The CD54HC/HCT75 are supplied in 16-lead hermetic dual-in-line packages (F suffix). The CD74HC/HCT75 are supplied in 16-lead dual-in-line plastic package (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: —40 to + 85°C
- *Balanced Propagation delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noice Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

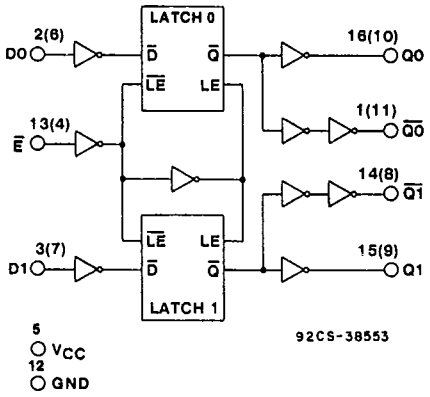


Fig. 1 - Logic Diagram

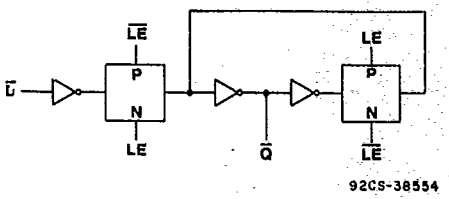


Fig. 2 - Latch Detail

CD54/74HC75
CD54/74HCT75

MAXIMUM RATINGS, *Absolute-Maximum Values:*

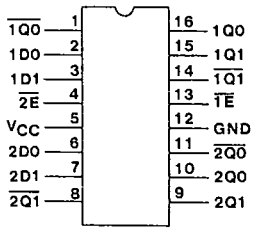
DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V) ..... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ OR $V_O > V_{CC} + 0.5$ V) ..... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V) ..... ± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): ..... ± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING -TEMPERATURE RANGE (T_A)
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 +150°C
LEAD TEMPERATUARE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



TERMINAL ASSIGNMENT

TRUTH TABLE

Inputs		Outputs	
D	$\overline{E}$	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q0	$\overline{Q0}$

H = High Level
L = Low Level
X = Don't Care
Q0 = The level of Q before the transition of $\overline{E}$.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC75/CD54HC75										CD74HCT75/CD54HCT75									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	Io mA	Vcc V	+ 25°C			-40/ + 85°C		-55/ + 125°C		V_I V	Vcc V	+ 25°C			-40/ + 85°C		-55/ + 125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—		4.5								
			4.5	3.15	—	—	3.15	—	3.15	—		to	2	—	—	2	—	2	—	
			6	4.2	—	—	4.2	—	4.2	—	—	5.5								V
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5								
			4.5	—	—	1.35	—	1.35	—	1.35		to	—	—	0.8	—	0.8	—	0.8	
			6	—	—	1.8	—	1.8	—	1.8		5.5								V
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or VIH	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	VIL or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	Vcc or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between Vcc & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	Vcc or Gnd	0	6	—	—	4	—	40	—	80	Vcc or Gnd	5.5	—	—	4	—	40	—	80	µA
Additional quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											Vcc-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
DO, D1	0.8
$\overline{1E}$, $\overline{2E}$	1.2

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6ns)

CHARACTERISTIC		C_L (pF)	SYMBOL	TYPICAL		UNITS
				HC75	HCT75	
Propagation Delay	D to Q	15	t_{PLH}	9	11	ns
	D to $\overline{Q}$	15		10	11	ns
	Enable to Q	15	t_{PHL}	10	11	ns
	Enable to $\overline{Q}$	15		11	12	ns
Power Dissipation Capacitance*		—	C_{PD}	46	46	pF

*C_{PD} is used to determine the dynamic power consumption per latch.
$PD = V_{CC}^2 fi (C_{PD} + C_L)$
fi = Input Frequency
C_L = Load Capacitance
V_{CC} = Supply Voltage

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25°C				-40°C to + 85°C				-55°C to + 125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pulse Width	t_w	2	80		—		100		—		120		—		
Enable Input		4.5	16		16		20		20		24		24		ns
		6	14		—		17		—		20		—		
Setup Time	t_{su}	2	60		—		75		—		90		—		
D to Enable		4.5	12		12		15		15		18		18		ns
		6	10		—		13		—		15		—		
Hold Time	t_h	2	3		—		3		-		3		—		
Enable to D		4.5	3		3		3		3		3		3		ns
		6	3		—		3		—		3		—		

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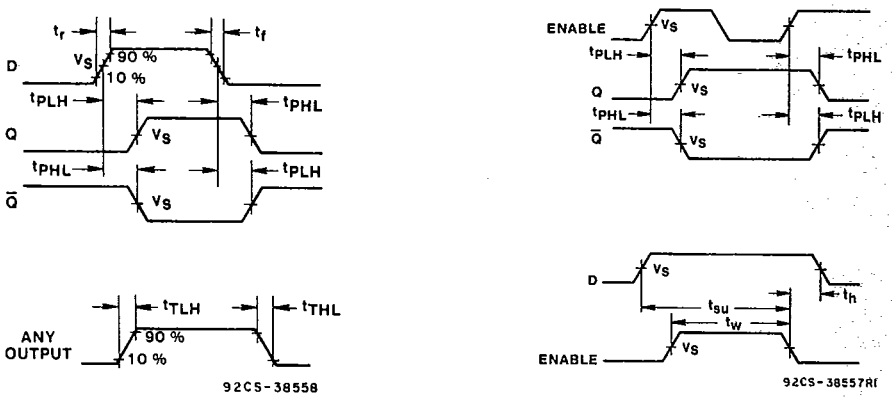
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to + 85°C				-55°C to + 125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Data to Q	t_{PLH}	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
	t_{PHL}	4.5	—	22	—	28	—	28	—	35	—	33	—	42	
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Propagation Delay Data to $\overline{Q}$	t_{PLH}	2	—	130	—	—	—	165	—	—	—	195	—	—	ns
	t_{PHL}	4.5	—	26	—	28	—	33	—	35	—	39	—	42	
		6	—	22	—	—	—	28	—	—	—	33	—	—	
Propagation Delay Enable to Q	t_{PLH}	2	—	130	—	—	—	165	—	—	—	195	—	—	ns
	t_{PHL}	4.5	—	26	—	28	—	33	—	35	—	39	—	42	
		6	—	22	—	—	—	28	—	—	—	33	—	—	
Propagation Delay Enable to $\overline{Q}$	t_{PLH}	2	—	130	—	—	—	165	—	—	—	195	—	—	ns
	t_{PHL}	4.5	—	26	—	30	—	33	—	38	—	39	—	45	
		6	—	22	—	—	—	28	—	—	—	33	—	—	
Output Transition Time	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V