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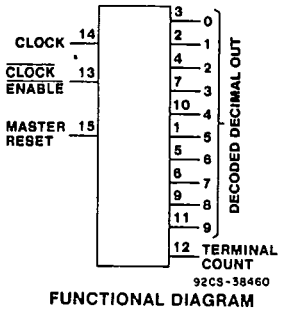
CD54/74HC4017
CD54/74HCT4017

File Number 1639

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM
CD54/74HC4017, CD54/74HCT4017

Decade Counter/Divider with 10 Decoded Outputs

Type Features:
- *Fully static operation*
- *Buffered inputs*
- *Common reset*
- *Positive edge clocking*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC4017 and CD54/74HCT4017 are high speed silicon gate CMOS 5-stage Johnson counters with 10 decoded outputs. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition of the CLOCK (CP) input. Each output stays high for one clock period of the 10 clock period cycle. The CARRY (TC) output transitions low to high after OUTPUT 10 goes low, and can be used in conjunction with the CLOCK ENABLE ($\overline{CE}$) to cascade several stages. The CLOCK ENABLE input disables counting when in the high state. A RESET (MR) input is also provided which when taken high sets all the decoded outputs, except "0", low.

The device can drive up to 10 low power Schottky equivalent loads. The CD54/74HCT4017 is an enhanced version of equivalent CMOS types.

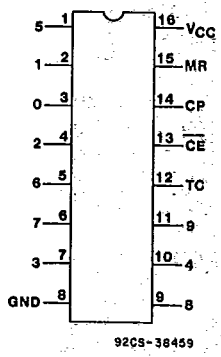
The CD54HC4017 and CD54HCT4017 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4017 and CD74HCT4017 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE

CP	$\overline{CE}$	MR	Output State*
L	X	L	No Change
X	H	L	No Change
X	X	H	"O"=H, "1"-"9"=L
↘	L	L	Increments Counter
↘	X	L	No Change
X	↗	L	No Change
H	↗	L	Increments Counter

H = High Level
L = Low Level
↘ = High-to-Low Transition
↗ = Low-to-High Transition
X=Don't Care
*If n<5 TC=H, Otherwise=L

Family Features:
- *Fanout (Over Temperature Range):*
  Standard Outputs — 10 LSTTL Loads
  Bus Driver Outputs — 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC4017
CD54/74HCT4017

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) ..... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) ..... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 V < V_O < V_{CC} +0.5$ V) ..... ± 25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}) ..... ± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

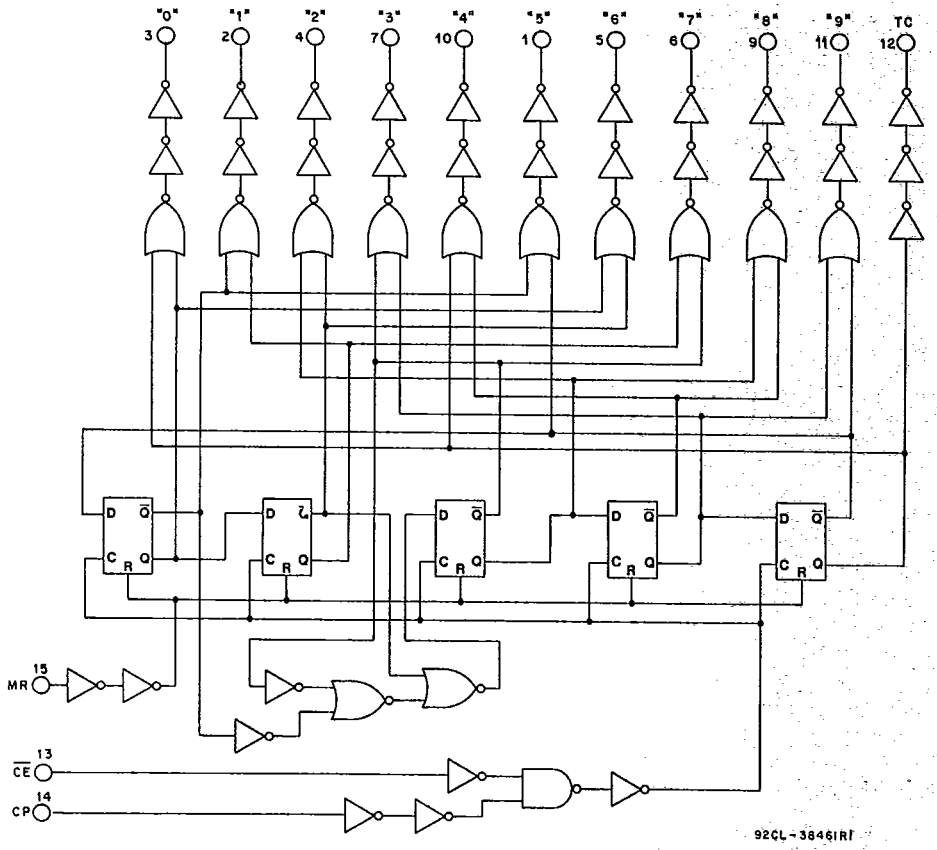


Fig. 1 — Logic diagram for the CD54/74HC/HCT 4017

CD54/74HC4017
CD54/74HCT4017

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4017/CD54HC4017										CD74HCT4017/CD54HCT4017									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
CP	0.15
$\overline{CE}$	0.25
MR	0.3

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2V	0	1000	ns
at 4.5 V	0	500	ns
at 6V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	Typical Values		UNITS
			HC	HCT	
Propagation Delay CP to Out	t_{PLH} t_{PHL}	15	19	19	ns
CP to TC	t_{PLH} t_{PHL}	15	19	19	ns
$\overline{CE}$ to Out	t_{PLH} t_{PHL}	15	21	21	ns
$\overline{CE}$ to TC	t_{PLH} t_{PHL}	15	21	21	ns
MR to Out	t_{PLH} t_{PHL}	15	19	19	ns
MR to TC	t_{PLH} t_{PHL}	15	19	19	ns
Max. CP Frequency	f_{MAX}	15	60	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	39	39	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency.
f_o = output frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

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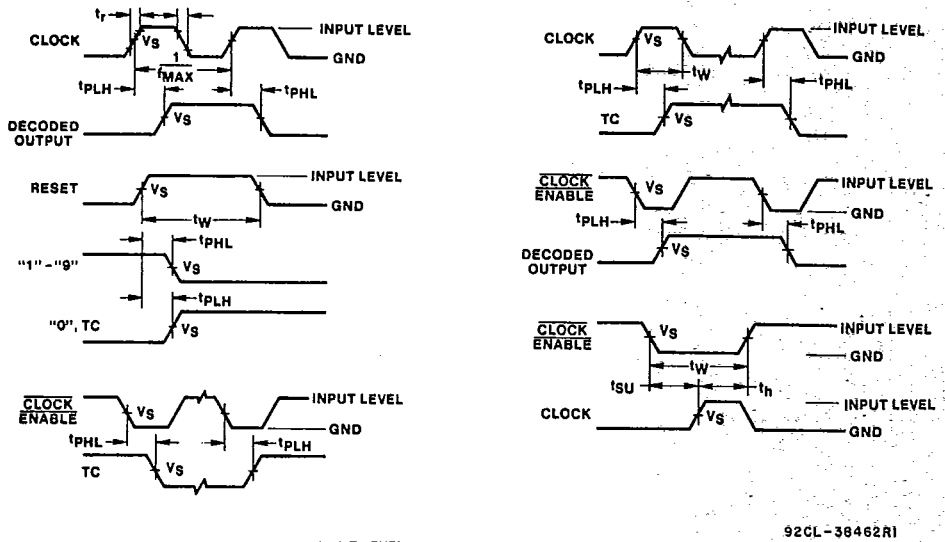
PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
CP Pulse Width	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
MR Pulse Width	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Max. Clock Freq.	f_{CL} (max.)	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	24	—	20	—	20	—	17	—	
		6	35	—	—	—	30	—	—	—	23	—	—	—	
$\overline{CE}$ to CP Setup Time	t_{su}	2	75	—	—	—	95	—	—	—	110	—	—	—	ns
		4.5	15	—	15	—	19	—	19	—	22	—	22	—	
		6	13	—	—	—	16	—	—	—	19	—	—	—	
$\overline{CE}$ to CP Hold Time	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
MR Removal Time	t_{REM}	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

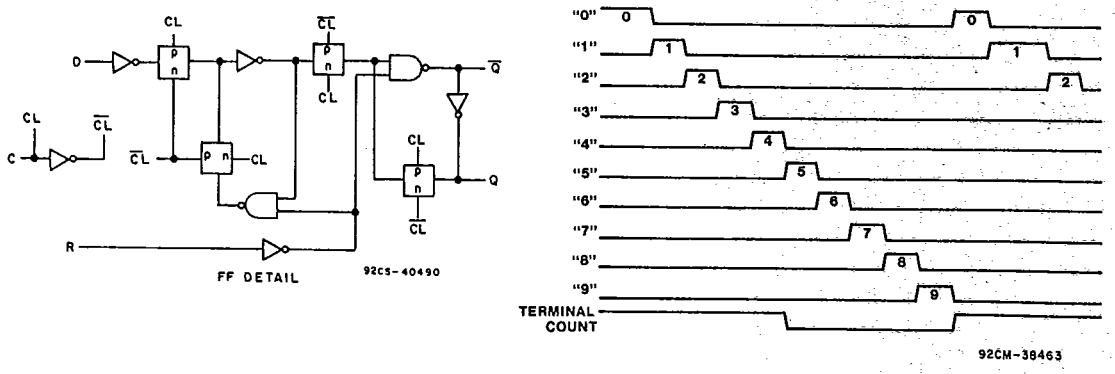
CHARACTERISTIC	SYMBOL	V_{CC}	25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay CP to any Dec. Out	t_{PLH}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
	t_{PHL}	4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
CP to TC	t_{PLH}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
	t_{PHL}	4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
$\overline{CE}$ to any Dec. Out	t_{PLH}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
	t_{PHL}	4.5	—	50	—	50	—	63	—	63	—	75	—	75	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
$\overline{CE}$ to TC	t_{PLH}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
	t_{PHL}	4.5	—	50	—	50	—	63	—	63	—	75	—	75	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
MR to any Dec. Out	t_{PLH}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
	t_{PHL}	4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
MR to TC	t_{PLH}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
	t_{PHL}	4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
Transition Time TC, Dec. Out	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_{IN}		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4017
CD54/74HCT4017



	CD54/74HC	CD54/74HCT
Input Level	V_{CC}	3 V
Vs	0.5 V_{CC}	1.3 V

Transition times and propagation delay times.



Timing diagram for the CD54/74HC/HCT4017