FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13715-3E

16-bit Proprietary Microcontrollers

CMOS

F^{2}MC-16LX MB90560/565 Series

MB90561/561A/562/562A/F562/F562B/V560
MB90567/568/F568

■ DESCRIPTION

The MB90560/565 series is a general-purpose 16-bit microcontroller designed for industrial, OA, and process control applications that require high-speed real-time processing. The device features a multi-function timer able to output a programmable waveform.

The microcontroller instruction set is based on the same AT architecture as the F^{2}MC-8L and F^{2}MC-16L families with additional instructions for high-level languages, extended addressing modes, enhanced signed multiplication and division instructions, and a complete range of bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word (32-bit) data.

■ FEATURES

- **Clock**
  - Internal oscillator circuit and PLL clock multiplication circuit
  - Oscillation clock
    Clock speed selectable from either the machine clock, main clock, or PLL clock. The main clock is the oscillation clock divided into 2 (0.5 MHz to 8 MHz for a 1 MHz to 16 MHz base oscillation) . The PLL clock is the oscillation clock multiplied by one to four (4 MHz to 16 MHz for a 4 MHz base oscillation) .
  - Minimum instruction execution time : 62.5 ns (for oscillation = 4 MHz, PLL clock setting = × 4, V_{CC} = 5.0 V)
- **Maximum CPU memory space : 16 MB**
  - 24-bit addressing
  - Bank addressing

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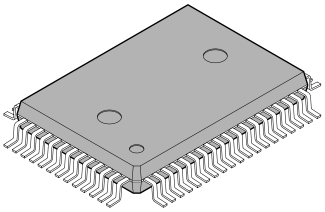
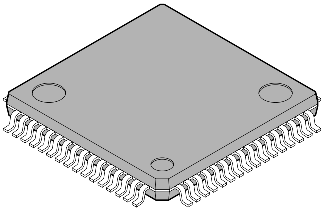
■ PACKAGES

64-pin plastic QFP



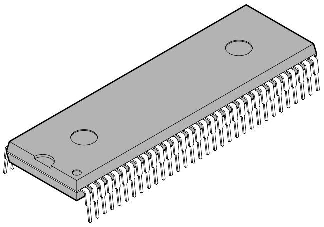
(FPT-64P-M06)

64-pin plastic LQFP



(FPT-64P-M09)

64-pin plastic SH-DIP



(DIP-64P-M01)

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- **Instruction set**
  - Bit, byte, word, and long word data types
  - 23 different addressing modes
  - Enhanced calculation precision using a 32-bit accumulator
  - Enhanced signed multiplication and division instructions and RETI instruction
- **Instruction set designed for high level language (C) and multi-tasking**
  - Uses a system stack pointer
  - Symmetric instruction set and barrel shift instructions
- **Program patch function (2 address pointers) .**
- **4-byte instruction queue**
- **Interrupt function**
  - Priority levels are programmable
  - 32 interrupts
- **Data transfer function**
  - Extended intelligent I/O service function : Up to 16 channels
- **Low-power consumption modes**
  - Sleep mode (CPU operating clock stops.)
  - Timebase timer mode (Only oscillation clock and timebase timer continue to operate.)
  - Stop mode (Oscillation clock stops.)
  - CPU intermittent operation mode (The CPU operates intermittently at the specified interval.)
- **Package**
  - LQFP-64P (FTP-64P-M09 : 0.65 mm pin pitch)
  - QFP-64P (FTP-64P-M06 : 1.00 mm pin pitch)
  - SH-DIP (DIP-64P-M01 : 1.778 mm pin pitch)
- **Process : CMOS technology**

■ PERIPHERAL FUNCTIONS (RESOURCES)

- **I/O ports : 51 ports (max.)**
- **Timebase timer : 1 channel**
- **Watchdog timer : 1 channel**
- **16-bit reload timer : 2 channel 5**
- **Multi-function timer**
  - 16-bit free-run timer : 1 channel
  - Output compare : 6 channels
    Can output an interrupt request when a match occurs between the count in the 16-bit freerun timer and the value set in the compare register.
  - Input capture : 4 channels
    On detecting an active edge on the input signal from an external input pin, copies the count value of the 16-bit freerun timer to the input capture data register and generates an interrupt request.
  - 8/16-bit PPG timer (8-bit × 6 channels or 16-bit × 3 channels) The period and duty of the output pulse can be set by the program.
  - Waveform generator (8-bit timer : 3 channels)
- **UART : 2 channels**
  - Full-duplex, double-buffered (8-bit)
  - Can be set to asynchronous or clock synchronous serial transfer (I/O expansion serial) operation
- **DTP/external interrupt circuit (8 channels)**
  - External interrupts can activate the extended intelligent I/O service.
  - Generates interrupts in response to external interrupt inputs.

- **Delayed interrupt generation module**
    - Generates an interrupt request for task switching.
- **8/10-bit A/D converter : 8 channels**
    - 8-bit or 10-bit resolution selectable

■ PRODUCT LINEUP

1. MB90560 Series

Part Number	MB90F562/B	MB90562/A	MB90561/A	MB90V560
Classification	Internal flash memory product	Internal mask ROM product		Evaluation product
ROM size	64 Kbytes		32 Kbytes	No ROM
RAM size	2 Kbytes		1 Kbytes	4 Kbytes
Dedicated emulator power supply*	—		—	No
CPU functions	Number of instructions : 351 Minimum instruction execution time : 62.5 ns for a 4 MHz oscillation (with ×4 multiplier) Addressing modes : 23 modes Program patch function : 2 address pointers Maximum memory space : 16 Mbytes			
Ports	I/O ports (CMOS) : 51			
UART	Full-duplex, double-buffered Clock synchronous or asynchronous operation selectable Can be used as I/O serial Internal dedicated baud rate generator 2 channels			
16-bit reload timer	16-bit reload timer operation 2 channels			
Multi-function timer	16-bit free-run timer × 1 channel Output compare × 6 channels Input capture × 4 channels 8/16-bit PPG timer (8-bit × 6 channels or 16-bit × 3 channels) Waveform generator (8-bit timer × 3 channels) 3-phase waveform output, deadtime output			
8/10-bit A/D converter	8 channels (multiplexed input) 8-bit or 10-bit resolution selectable Conversion time : 6.13 μs (min.) (for maximum machine clock speed 16 MHz)			
DTP/external interrupts	8 channels (8 channels available, shared with A/D input) Interrupt triggers : “L” → “H” edge, “H” → “L” edge, “L” level, “H” level (selectable)			
Low power consumption modes	Sleep mode, timebase timer mode, stop mode, and CPU intermittent operation mode			
Process	CMOS			
Operating voltage	5 V ± 10%			

* : DIP switch setting (S2) when using the emulation pod (MB2145-507) .
Refer to “2.7 Dedicated Emulator Power Supply” in the “MB2145-507 Hardware Manual” for details.

2. MB90565 Series

Part Number	MB90F568	MB90568	MB90567
Classification	Internal flash memory product	Internal mask ROM product	
ROM size	128 Kbytes		96 Kbytes
RAM size	4 Kbytes		4 Kbytes
Dedicated emulator power supply*	—		—
CPU functions	Number of instructions : 351 Minimum instruction execution time : 62.5 ns for a 4 MHz oscillation (with ×4 multiplier) Addressing modes : 23 modes Program patch function : 2 address pointers Maximum memory space : 16 Mbytes		
Ports	I/O ports (CMOS) : 51		
UART	Full-duplex, double-buffered Clock synchronous or asynchronous operation selectable Can be used as I/O serial Internal dedicated baud rate generator 2 channels		
16-bit reload timer	16-bit reload timer operation 2 channels		
Multi-function timer	16-bit free-run timer × 1 channel Output compare × 6 channels Input capture × 4 channels 8/16-bit PPG timer (8-bit × 6 channels or 16-bit × 3 channels) Waveform generator (8-bit timer × 3 channels) 3-phase waveform output, deadtime output		
8/10-bit A/D converter	8 channels (multiplexed input) 8-bit or 10-bit resolution selectable Conversion time : 6.13 µs (min.) (for maximum machine clock speed 16 MHz)		
DTP/external interrupts	8 channels (8 channels available, shared with A/D input) Interrupt triggers : “L” → “H” edge, “H” → “L” edge, “L” level, “H” level (selectable)		
Low power consumption modes	Sleep mode, timebase timer mode, stop mode, and CPU intermittent operation mode		
Process	CMOS		
Operating voltage	3.3 V ± 0.3 V		

* : DIP switch setting (S2) when using the emulation pod (MB2145-507) .
Refer to “2.7 Dedicated Emulator Power Supply” in the “MB2145-507 Hardware Manual” for details.

■ PACKAGE AND CORRESPONDING PRODUCTS

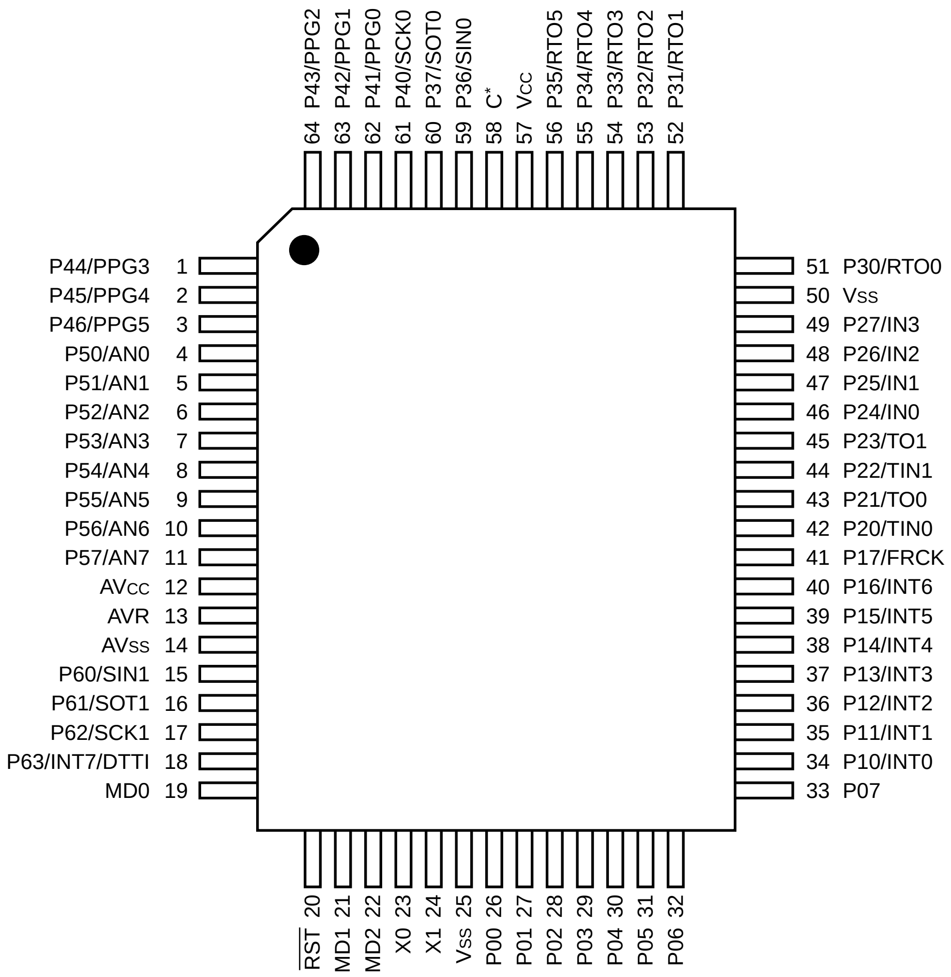
Package	MB90561/A	MB90562/A	MB90F562/B	MB90567	MB90568	MB90F568	MB90V560
FPT-64P-M09 (LQFP-0.65 mm)	○	○	○	○	○	○	×
FPT-64P-M06 (QFP-1.00 mm)	○	○	○	○	○	○	×
DIP-64P-M01 (SH-DIP)	○	○	○	×	×	×	×
PGA-256C-A01 (PGA)	×	×	×	×	×	×	○

○ : Available × : Not available

Note : See the “Package Dimensions” section for details of each package.

■ PIN ASSIGNMENTS

(TOP VIEW)


64 P43/PPG2
63 P42/PPG1
62 P41/PPG0
61 P40/SCK0
60 P37/SOT0
59 P36/SIN0
58 C*
57 Vcc
56 P35/RTO5
55 P34/RTO4
54 P33/RTO3
53 P32/RTO2
52 P31/RTO1
P44/PPG3 1
P45/PPG4 2
P46/PPG5 3
P50/AN0 4
P51/AN1 5
P52/AN2 6
P53/AN3 7
P54/AN4 8
P55/AN5 9
P56/AN6 10
P57/AN7 11
AVcc 12
AVR 13
AVss 14
P60/SIN1 15
P61/SOT1 16
P62/SCK1 17
P63/INT7/DTTI 18
MD0 19
51 P30/RTO0
50 Vss
49 P27/IN3
48 P26/IN2
47 P25/IN1
46 P24/IN0
45 P23/TO1
44 P22/TIN1
43 P21/TO0
42 P20/TIN0
41 P17/FRCK
40 P16/INT6
39 P15/INT5
38 P14/INT4
37 P13/INT3
36 P12/INT2
35 P11/INT1
34 P10/INT0
33 P07
20 RST
21 MD1
22 MD2
23 X0
24 X1
25 Vss
26 P00
27 P01
28 P02
29 P03
30 P04
31 P05
32 P06

(FPT-64P-M06)

* : N.C. on the MB90F568, MB90567, and MB90568.

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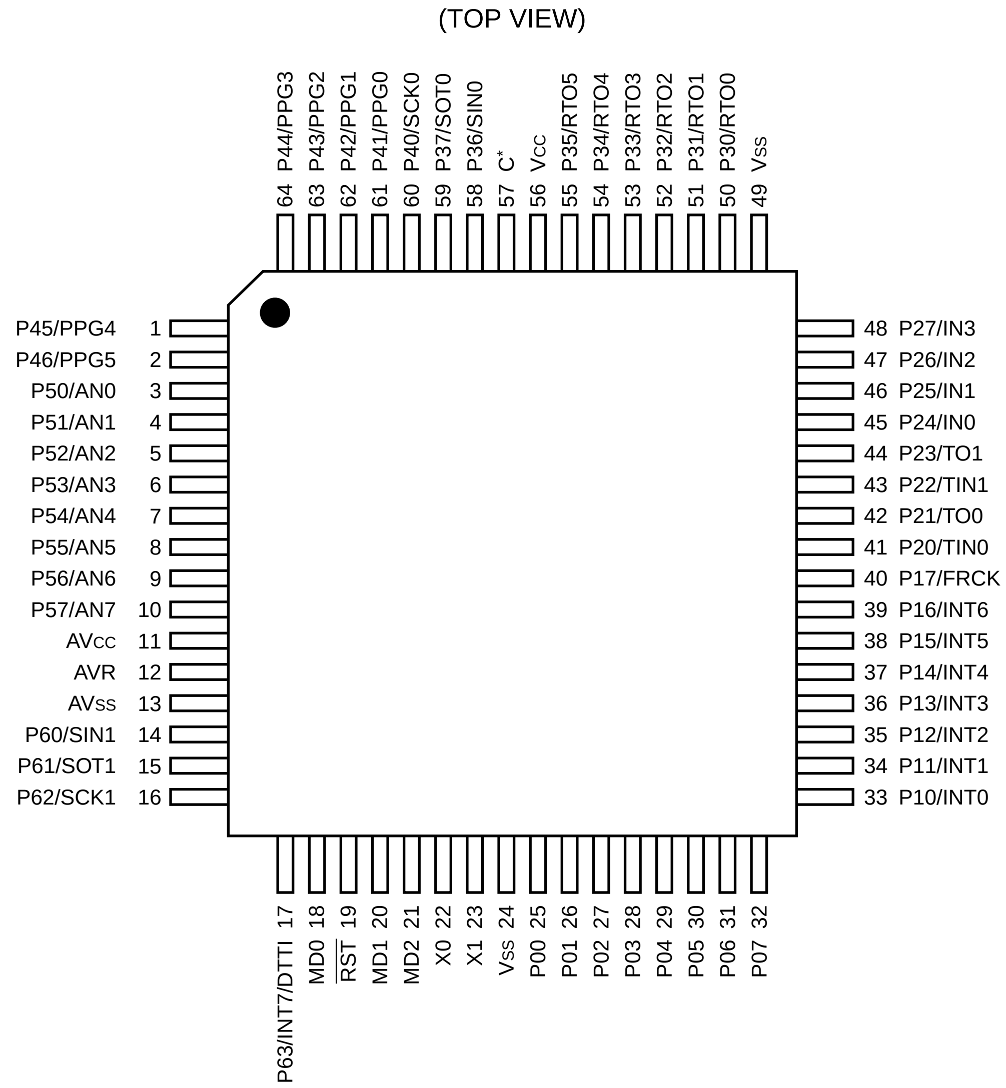
(TOP VIEW)
64 P44/PPG3
63 P43/PPG2
62 P42/PPG1
61 P41/PPG0
60 P40/SCK0
59 P37/SOT0
58 P36/SIN0
57 C*
56 Vcc
55 P35/RTO5
54 P34/RTO4
53 P33/RTO3
52 P32/RTO2
51 P31/RTO1
50 P30/RTO0
49 Vss
P45/PPG4 1
P46/PPG5 2
P50/AN0 3
P51/AN1 4
P52/AN2 5
P53/AN3 6
P54/AN4 7
P55/AN5 8
P56/AN6 9
P57/AN7 10
AVcc 11
AVR 12
AVss 13
P60/SIN1 14
P61/SOT1 15
P62/SCK1 16
48 P27/IN3
47 P26/IN2
46 P25/IN1
45 P24/IN0
44 P23/TO1
43 P22/TIN1
42 P21/TO0
41 P20/TIN0
40 P17/FRCK
39 P16/INT6
38 P15/INT5
37 P14/INT4
36 P13/INT3
35 P12/INT2
34 P11/INT1
33 P10/INT0
P63/INT7/DTTI 17
MD0 18
RST 19
MD1 20
MD2 21
X0 22
X1 23
Vss 24
P00 25
P01 26
P02 27
P03 28
P04 29
P05 30
P06 31
P07 32

(FPT-64P-M09)

* : N.C. on the MB90F568, MB90567, and MB90568.

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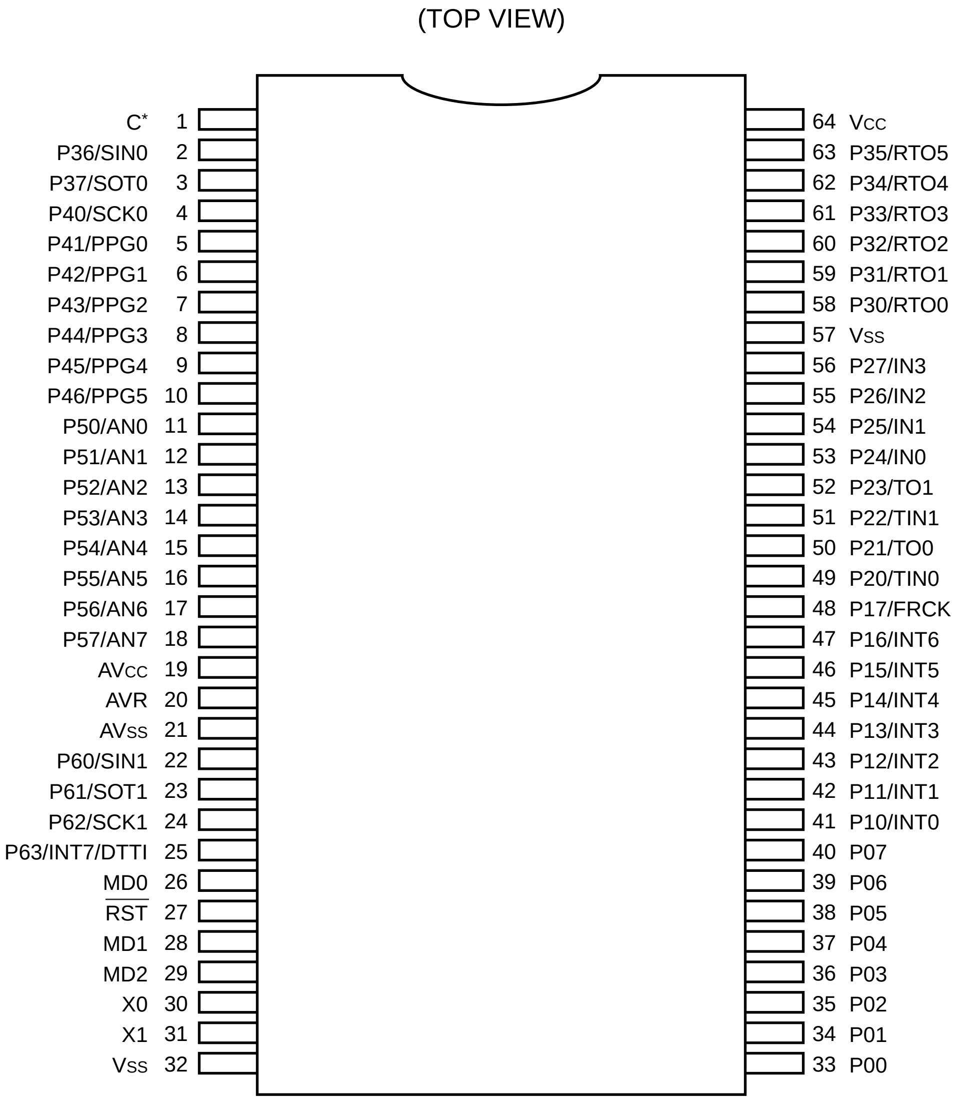
(TOP VIEW)
C* 1
P36/SIN0 2
P37/SOT0 3
P40/SCK0 4
P41/PPG0 5
P42/PPG1 6
P43/PPG2 7
P44/PPG3 8
P45/PPG4 9
P46/PPG5 10
P50/AN0 11
P51/AN1 12
P52/AN2 13
P53/AN3 14
P54/AN4 15
P55/AN5 16
P56/AN6 17
P57/AN7 18
AVCC 19
AVR 20
AVSS 21
P60/SIN1 22
P61/SOT1 23
P62/SCK1 24
P63/INT7/DTTI 25
MD0 26
RST 27
MD1 28
MD2 29
X0 30
X1 31
VSS 32
64 VCC
63 P35/RTO5
62 P34/RTO4
61 P33/RTO3
60 P32/RTO2
59 P31/RTO1
58 P30/RTO0
57 VSS
56 P27/IN3
55 P26/IN2
54 P25/IN1
53 P24/IN0
52 P23/TO1
51 P22/TIN1
50 P21/TO0
49 P20/TIN0
48 P17/FRCK
47 P16/INT6
46 P15/INT5
45 P14/INT4
44 P13/INT3
43 P12/INT2
42 P11/INT1
41 P10/INT0
40 P07
39 P06
38 P05
37 P04
36 P03
35 P02
34 P01
33 P00

(DIP-64P-M01)
(Only support MB90F562/B, MB90561/A, and MB90562/A.)

* : Not support on the MB90F568, MB90567, and MB90568.

■ PIN DESCRIOTIONS

Pin No.			Pin Name	Circuit Type*	State/ Function at Reset	Description
QFPM06	LQFPM09	SDIP				
23, 24	22, 23	30, 31	X0, X1	A	Oscillator	Connect oscillator to these pins. If using an external clock, leave X1 open.
20	19	27	$\overline{\text{RST}}$	B	Reset input	External reset input pin
26 to 33	25 to 32	33 to 40	P00 to P07	C	Port inputs (Hi-Z outputs)	I/O ports
34 to 40	33 to 39	41 to 47	P10 to P16	C		I/O ports
			INT0 to INT6			Can be used as interrupt request inputs ch0 to ch6. In standby mode, these pins can operate as inputs by setting the bits corresponding to EN0 to EN6 to “1” and setting as input ports. When used as a port, set the corresponding bits in the analog input enable register (ADER) to “port”.
41	40	48	P17	C		I/O port
			FRCK			External clock input pin for the freerun timer. This pin can be used as an input when set as the clock input for the freerun timer and set as an input port. When used as a port, set the corresponding bit in the analog input enable register (ADER) to “port”.
42	41	49	P20	D		I/O port
			TIN0			External clock input pin for reload timer ch0. This pin can be used as an input when set as the external clock input and set as an input port.
43	42	50	P21	D		I/O port
			TO0			Event output pin for reload timer ch0. Output operates when event output is enabled.
44	43	51	P22	D		I/O port
			TIN1			External clock input pin for reload timer ch1. This pin can be used as an input when set as the external clock input and set as an input port.
45	44	52	P23	D		I/O port
			TO1			Event output pin for reload timer ch1. Output operates when event output is enabled.
46 to 49	45 to 48	53 to 56	P24 to P27	D		I/O ports
			IN0 to IN3			Trigger input pins for input capture ch0 to ch3. These pins can be used as an input when set as an input capture trigger input and set as an input port.

* : See “■ I/O CIRCUITS” for details of the circuit types.

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Pin No.			Pin Name	Circuit Type*	State/ Function at Reset	Description
QFPM06	LQFPM09	SDIP				
51 to 56	50 to 55	58 to 63	P30 to P35	E	Port inputs (Hi-Z)	I/O ports
			RTO0 to RTO5			Event output pins for the output compare and waveform generator output pins. The pins output the specified waveform generated by the waveform generator. If not using waveform generation, these terminals enable output compare event output to use as output compare outputs. When used as a port, set the corresponding bits in the analog input enable register (ADER) to “port”.
59	58	2	P36	D		I/O port
			SIN0			Serial data input pin for UART ch0. This pin is used continuously when input operation is enabled for UART ch0. In this case, do not use as a general input pin.
60	59	3	P37	D		I/O port
			SOT0			Serial data output pin for UART ch0. Output operates when UART ch0 output is enabled.
61	60	4	P40	D		I/O port
			SCK0			Serial clock I/O pin for UART ch0. Output operates when UART ch0 clock output is enabled.
62 to 64, 1 to 3	61 to 64, 1, 2	5 to 10	P41 to P46	D		I/O ports
			PPG0 to PPG5			Output pins for PPG ch0 to ch5. The outputs operate when output is enabled for PPG ch0 to ch5.
4 to 11	3 to 10	11 to 18	P50 to P57	F	Analog inputs	I/O ports
			AN0 to AN7			Analog input pins for the A/D converter. Input is available when the corresponding analog input enable register bits are set. (ADER : bit0 to bit7)
12	11	19	AV$_{CC}$	—	Power supply input	V$_{CC}$ power supply input pin for A/D converter.
13	12	20	AVR	G	Reference voltage input	Reference voltage input pin for A/D converter. Ensure that the voltage does not exceed V$_{CC}$.
14	13	21	AV$_{SS}$	—	Power supply input	V$_{SS}$ power supply input pin for A/D converter.

* : See “■ I/O CIRCUITS” for details of the circuit types.

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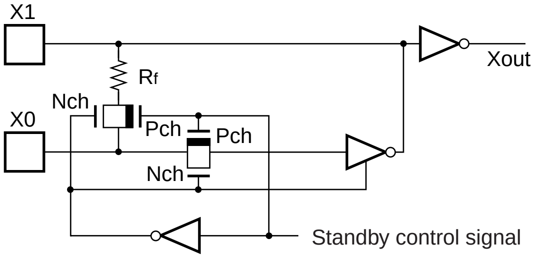
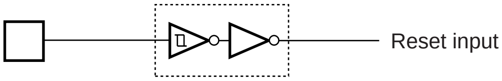
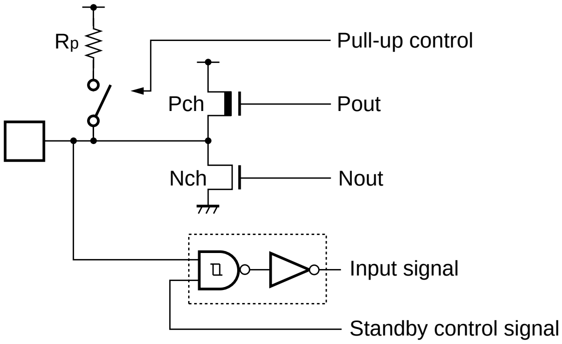
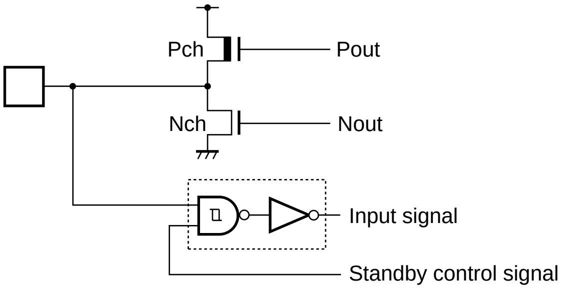
Pin No.			Pin Name	Circuit Type*1	State/ Function at Reset	Description
QFPM06	LQFPM09	SDIP				
15	14	22	P60	D	Port input (Hi-Z)	I/O port
			SIN1			Serial data input pin for UART ch1. This pin is used continuously when input operation is enabled for UART ch1. In this case, do not use as a general input pin.
16	15	23	P61	D		I/O port
			SOT1			Serial data output pin for UART ch1. Output operates when UART ch1 output is enabled.
17	16	24	P62	D		I/O port
			SCK1			Serial clock I/O pin for UART ch1. Output operates when UART ch1 clock output is enabled.
18	17	25	P63	D		I/O port
			INT7			This pin can be used as interrupt request input ch7. In standby mode, this pin can operate as an input by setting the bit corresponding to EN7 to "1" and setting as an input port.
			DTTI			Fixed pin level input pin when RTO0 to RTO5 pins are used. Input is enabled when "input enabled" set in the waveform generator.
58	57	1	C*2	—	Capacitor pin, power supply input	Capacitor pin for stabilizing the power supply. Connect an external ceramic capacitor of approximately 0.1 µF.
19	18	26	MD0	B	Mode input pins	Input pin for setting the operation mode. Connect directly to V_{CC} or V_{SS}.
21	20	28	MD1	B		Input pin for setting the operation mode. Connect directly to V_{CC} or V_{SS}.
22	21	29	MD2	B		Input pin for setting the operation mode. Connect directly to V_{SS}.
25, 50	24, 49	32, 57	V_{SS}	—	Power supply inputs	Power supply (GND) input pin
57	56	64	V_{CC}	—		MB90560 series is power supply (5 V) input pin MB90565 series is power supply (3.3 V) input pin

*1 : See "■ I/O CIRCUITS" for details of the circuit types.

*2 : N.C. on the MB90F568, MB90567, and MB90568

■ I/O CIRCUITS

Type	Circuit	Remarks
A	 X1 Xout Rf Nch X0 Pch Pch Nch Standby control signal	• Oscillation circuit Internal oscillation feedback resistor (R_f)
B	 Reset input	• CMOS hysteresis reset input pin
C	 Rp Pull-up control Pch Pout Nch Nout Input signal Standby control signal	• CMOS hysteresis I/O pin with pull-up control CMOS output CMOS hysteresis input (with input cut-off function in standby mode) Internal pull-up resistor (R_p) < Note > • The pull-up resistor is active when the port is set as an input.
D	 Pch Pout Nch Nout Input signal Standby control signal	• CMOS hysteresis I/O pin CMOS output CMOS hysteresis input (with input cut-off function in standby mode) < Notes > • The I/O port output and internal resource output share the same output buffer. • The I/O port input and internal resource input share the same input buffer.

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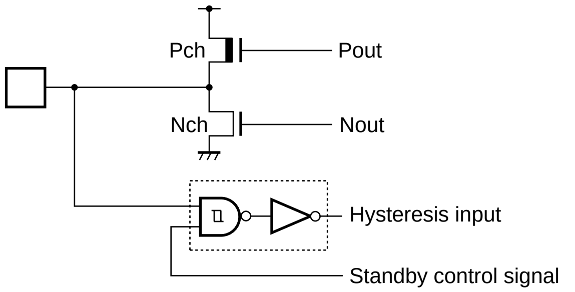
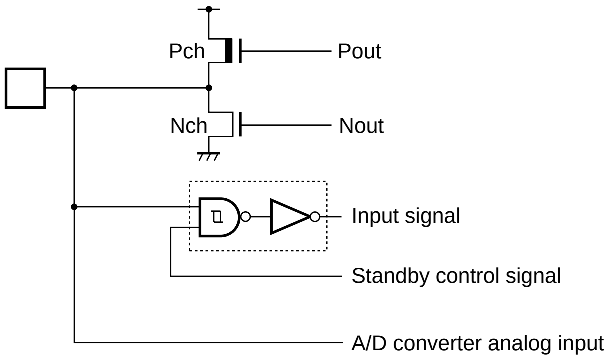
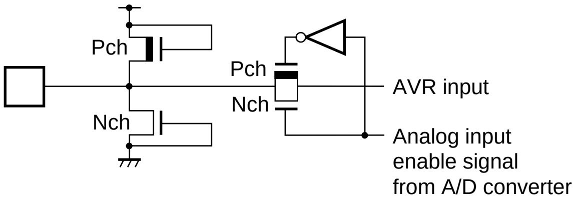
Type	Circuit	Remarks
E	 Pch Pout Nch Nout Hysteresis input Standby control signal	• CMOS I/O pin CMOS output CMOS hysteresis input (with input cut-off function in standby mode) < I_{OL} = 12 mA >
F	 Pch Pout Nch Nout Input signal Standby control signal A/D converter analog input	• Analog/CMOS hysteresis I/O pin CMOS output CMOS hysteresis input (with input cut-off function in standby mode) Analog input (Analog input to A/D converter is enabled when “1” is set in the corresponding bit in the analog input enable register (ADER) .) • The I/O port output and internal resource output share the same output buffer. • The I/O port input and internal resource input share the same input buffer.
G	 Pch Nch Pch Nch AVR input Analog input enable signal from A/D converter	• A/D converter (AVR) voltage input pin

■ HANDLING DEVICES

Take note of the following nine points when handling devices :

- Do not exceed maximum rated voltage (to prevent latch-up)
- Supply voltage stability
- Power-on precautions
- Treatment of unused pins
- Treatment of A/D converter power supply pins
- Notes on using an external clock
- Power supply pins
- Sequence for connecting and disconnecting the A/D converter power supply and analog input pins
- Notes on using the DIV A, Ri and DIVW A, RWi instructions

- **Device Handling Precautions**

(1) Do not exceed maximum rated voltage (to prevent latch-up)

Do not apply a voltage grater than V_{CC} or less than V_{SS} to the MB90560/565 series input or output pins. Also ensure that the voltage between V_{CC} and V_{SS} does not exceed the rating. Applying a voltage in excess of the ratings may result in latch-up causing thermal damage to circuit elements.

Similarly, when connecting or disconnecting the power to the analog power supply (AV_{CC}, AVR) and analog inputs (AN0 to AN7) , ensure that the analog power supply voltages do not exceed the digital voltage (V_{CC}) .

(2) Supply voltage stability

Rapid changes in the V_{CC} supply voltage may cause the device to misoperate. Accordingly, ensure that the V_{CC} power supply is stable. The standard for power supply voltage stability is a peak-to-peak V_{CC} ripple voltage at the supply frequency (50 to 60 Hz) of 10% or less of V_{CC} and a transient fluctuation in the voltage of 0.1 V/ms or less when turning the power supply on or off.

(3) Power-on precautions

To prevent misoperation of the internal regulator circuit, ensure that the voltage rise time at power-on is at least 50 µs (between 0.2 V to 2.7 V) .

(4) Treatment of unused pins

Leaving unused input pins unconnected can cause misoperation or permanent damage to the device due to latchup. Always pull-up or pull-down unused pins using a 2 kΩ or larger resistor.

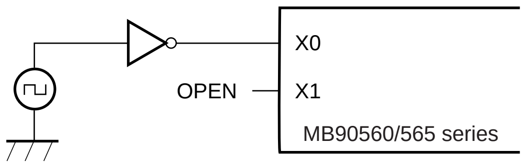
If some I/O pins are unused, either set as outputs and leave open circuit or set as inputs and treat in the same way as input pins.

(5) Treatment of A/D converter power supply pins

If not using the A/D converter, connect the analog power supply pins so that $AV_{CC} = AVR = V_{CC}$ and $AV_{SS} = V_{SS}$.

(6) Notes on using an external clock

Even if using an external clock, an oscillation stabilization delay time occurs after a power-on reset and when recovering from stop mode in the same way as when an oscillator is connected. When using an external clock, drive the X0 pin only and leave the X1 pin open.



Example of using an external clock

(7) Power supply pins

The multiple V_{CC} and V_{SS} pins are connected together in the internal device design so as to prevent misoperation such as latch-up. However, always connect all V_{CC} and V_{SS} pins to the same potential externally to minimize spurious radiation, prevent misoperation of strobe signals due to increases in the ground level, and maintain the overall output current rating.

Also, ensure that the impedance of the V_{CC} and V_{SS} connections to the power supply is as low as possible.
To minimize these problems, connect a bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS}. Connect the capacitor close to the V_{CC} and V_{SS} pins.

(8) Sequence for connecting and disconnecting power supply

Do not apply voltage to the A/D converter power supply pins (AV_{CC}, AVR, AV_{SS}) or analog inputs (AN0 to AN7) until the digital power supply (V_{CC}) is turned on. When turning the device off, turn off the digital power supply after disconnecting the A/D converter power supply and analog inputs. When turning the power on or off, ensure that AVR does not exceed AV_{CC}.

When using the I/O ports that share pins with the analog inputs, ensure that the input voltage does not exceed AV_{CC} (turning the analog and digital power supplies on and off simultaneously is OK) .

(9) Conditions when output from ports 0 and 1 is undefined

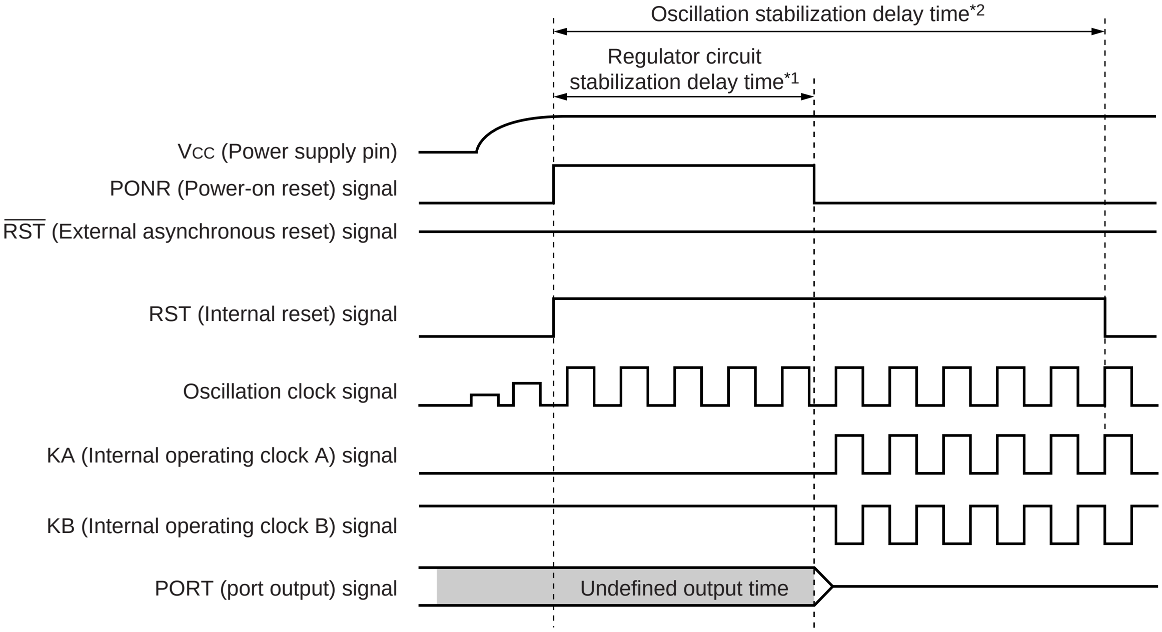
After turning on the power supply, the outputs from ports 0 and 1 are undefined during the oscillation stabilization delay time controlled by the regulator circuit (during the power-on reset) if the $\overline{RST}$ pin level is “H”. When the $\overline{RST}$ pin level is “L”, ports 0 and 1 go to high impedance.

Figures 1 and 2 show the timing (for the MB90F562/B and MB90V560) .

Note that this undefined output period does not occur on products without an internal regulator circuit as these products do not have an oscillation stabilization delay time.

(MB90561/A, MB90562/A, MB90F568, and MB90567/8)

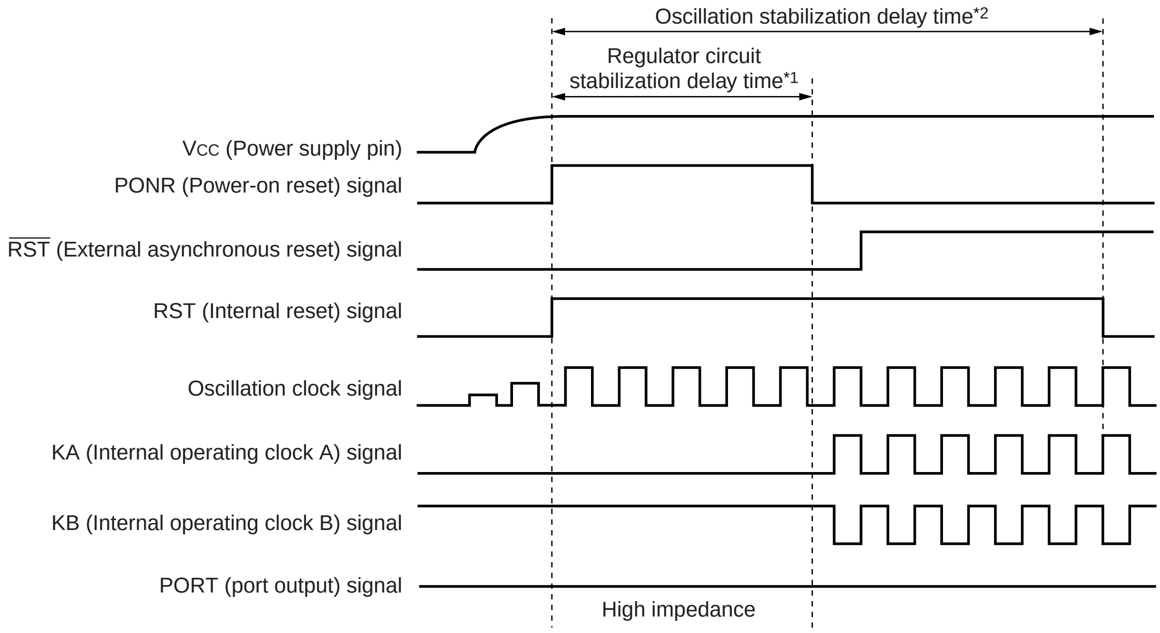
- **Figure 1 Timing chart for undefined output from ports 0 and 1 (When $\overline{\text{RST}}$ pin level is “H”)**


Oscillation stabilization delay time*2
Regulator circuit stabilization delay time*1
Vcc (Power supply pin)
PONR (Power-on reset) signal
$\overline{\text{RST}}$ (External asynchronous reset) signal
RST (Internal reset) signal
Oscillation clock signal
KA (Internal operating clock A) signal
KB (Internal operating clock B) signal
PORT (port output) signal
Undefined output time

*1 : Regulator circuit oscillation stabilization delay time :
2^{17}/Oscillation clock frequency (approx. 8.19 ms for a 16 MHz oscillation clock frequency)

*2 : Oscillation stabilization delay time :
2^{18}/Oscillation clock frequency (approx. 16.38 ms for a 16 MHz oscillation clock frequency)

- **Figure 2 Timing chart for ports 0 and 1 going to high impedance state (When $\overline{RST}$ pin level is “L”)**


Oscillation stabilization delay time*2
Regulator circuit stabilization delay time*1
VCC (Power supply pin)
PONR (Power-on reset) signal
RST (External asynchronous reset) signal
RST (Internal reset) signal
Oscillation clock signal
KA (Internal operating clock A) signal
KB (Internal operating clock B) signal
PORT (port output) signal
High impedance

*1 : Regulator circuit oscillation stabilization delay time :
2^{17}/Oscillation clock frequency (approx. 8.19 ms for a 16 MHz oscillation clock frequency)

*2 : Oscillation stabilization delay time :
2^{18}/Oscillation clock frequency (approx. 16.38 ms for a 16 MHz oscillation clock frequency)

(10) Notes on using the DIV A, Ri and DIVW A, RWi instructions

The location in which the remainder value produced by the signed division instructions “DIV A, Ri” and “DIVW A, RWi” is stored depends on the bank register. The remainder is stored in an address in the memory bank specified in the bank register.

Set the bank register to “00_H” when using the “DIV A, Ri” and “DIVW A, RWi” instructions.

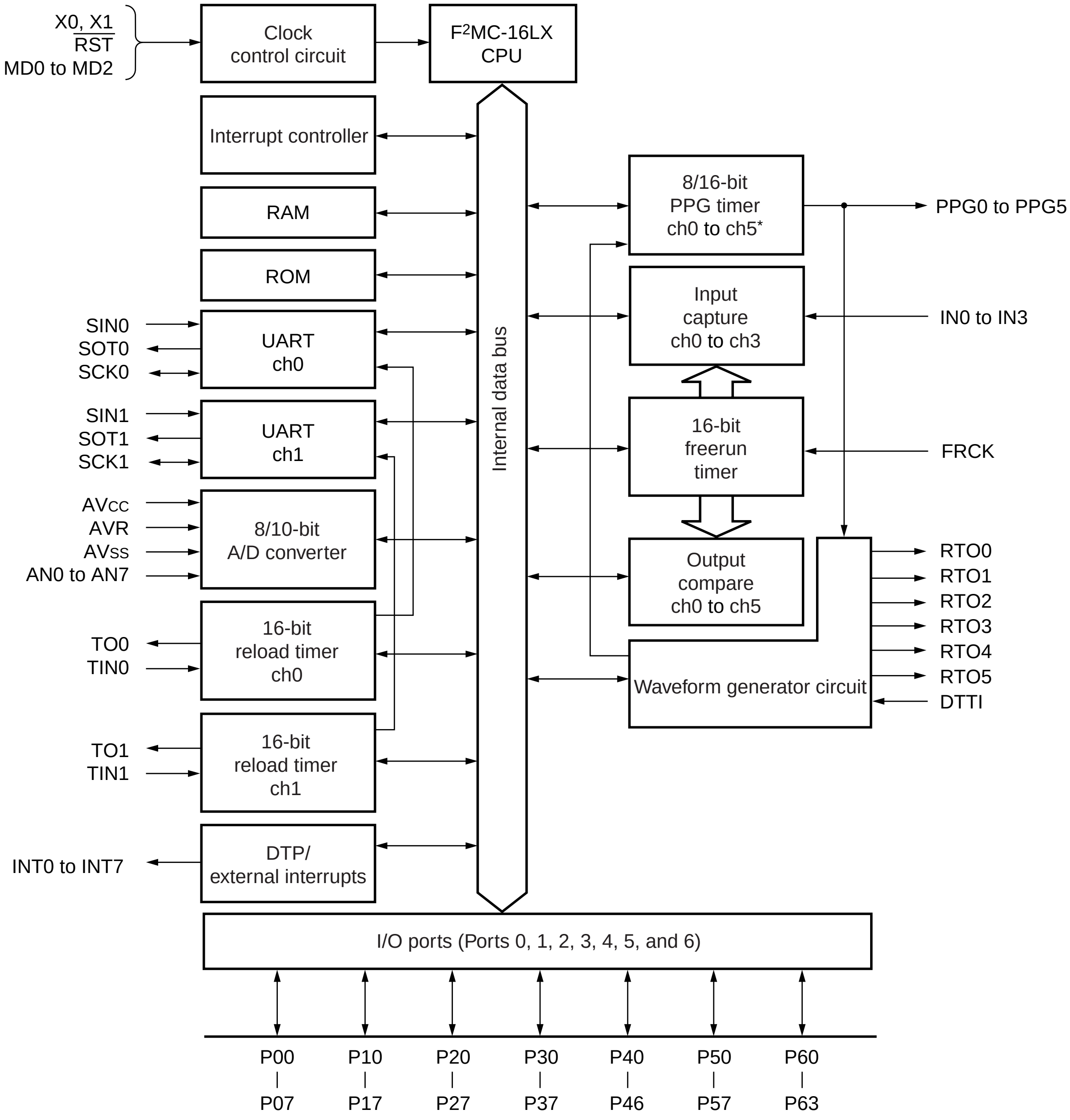
(11) Notes on using REALOS

The extended intelligent I/O service (EI^2OS) cannot be used when using REALOS.

(12) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the self oscillation circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

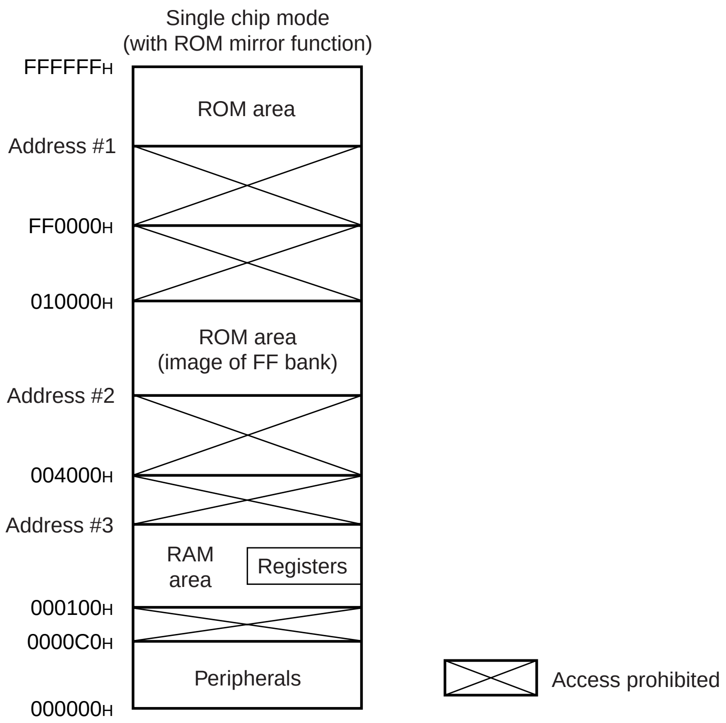
■ BLOCK DIAGRAM


X0, X1
RST
MD0 to MD2
Clock control circuit
F2MC-16LX CPU
Interrupt controller
RAM
ROM
SIN0
SOT0
SCK0
UART ch0
SIN1
SOT1
SCK1
UART ch1
AVCC
AVR
AVSS
AN0 to AN7
8/10-bit A/D converter
TO0
TIN0
16-bit reload timer ch0
TO1
TIN1
16-bit reload timer ch1
INT0 to INT7
DTP/ external interrupts
Internal data bus
8/16-bit PPG timer ch0 to ch5*
PPG0 to PPG5
Input capture ch0 to ch3
IN0 to IN3
16-bit freerun timer
FRCK
Output compare ch0 to ch5
Waveform generator circuit
RTO0
RTO1
RTO2
RTO3
RTO4
RTO5
DTTI
I/O ports (Ports 0, 1, 2, 3, 4, 5, and 6)
P00 | P07
P10 | P17
P20 | P27
P30 | P37
P40 | P46
P50 | P57
P60 | P63

* : Channel numbers when used as 8-bit timers. Three channels (ch1, ch3, and ch5) are available when used as 16-bit timers.

Note: The I/O ports share pins with the various peripheral functions (resources) .
See the Pin Assignment and Pin Description sections for details.
Note that, if a pin is used by a peripheral function (resource) , it may not be used as an I/O port.

■ MEMORY MAP


Single chip mode
(with ROM mirror function)
FFFFFFH
ROM area
Address #1
FF0000H
010000H
ROM area
(image of FF bank)
Address #2
004000H
Address #3
RAM
area
Registers
000100H
0000C0H
Peripherals
000000H
Access prohibited

Part No.	Address#1	Address#2	Address#3
MB90561/A	FF8000$_H$	008000$_H$	000500$_H$
MB90562/A	FF0000$_H$	004000$_H$	000900$_H$
MB90F562/B	FF0000$_H$	004000$_H$	000900$_H$
MB90567	FE8000$_H$	004000$_H$	001100$_H$
MB90568	FE0000$_H$	004000$_H$	001100$_H$
MB90F568	FE0000$_H$	004000$_H$	001100$_H$
MB90V560	FE0000$_H$*	004000$_H$*	001100$_H$

* : “V” products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Memory map of MB90560/565 series

Notes :
- When specified in the ROM mirror function register, the upper part of 00 bank (“004000$_H$ to 00FFFF$_H$”) contains a mirror of the data in the upper part of FF bank (“FF4000$_H$ to FFFFFF$_H$”) .
- See “10. ROM Mirror Function Selection Module” in the Peripheral Functions section for details of the ROM mirror function settings.

Remarks :
- The ROM mirror function is provided so the C compiler’s small memory model can be used.
- The lower 16 bits of the FF bank and 00 bank addresses are the same. However, as the FF bank ROM area exceeds 48 KBytes, the entire ROM data area cannot be mirrored in 00 bank.
- When using the C compiler’s small memory model, locating data tables in the area “FF4000$_H$ to FFFFFF$_H$” makes the image of the data visible in the “004000$_H$ to 00FFFF$_H$” area. This means that data tables located in ROM can be referenced without needing to declare far pointers.

■ I/O MAP

Address	Abbreviated Register Name	Register name	Read/ Write	Resource Name	Initial Value
000000$_H$	PDR0	Port 0 data register	R/W	Port 0	XXXXXXXX$_B$
000001$_H$	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXX$_B$
000002$_H$	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXX$_B$
000003$_H$	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXX$_B$
000004$_H$	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXX$_B$
000005$_H$	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXX$_B$
000006$_H$	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXX$_B$
000007$_H$ to 00000F$_H$	Access prohibited				
000010$_H$	DDR0	Port 0 direction register	R/W	Port 0	0 0 0 0 0 0 0 0$_B$
000011$_H$	DDR1	Port 1 direction register	R/W	Port 1	0 0 0 0 0 0 0 0$_B$
000012$_H$	DDR2	Port 2 direction register	R/W	Port 2	0 0 0 0 0 0 0 0$_B$
000013$_H$	DDR3	Port 3 direction register	R/W	Port 3	0 0 0 0 0 0 0 0$_B$
000014$_H$	DDR4	Port 4 direction register	R/W	Port 4	X 0 0 0 0 0 0 0$_B$
000015$_H$	DDR5	Port 5 direction register	R/W	Port 5	0 0 0 0 0 0 0 0$_B$
000016$_H$	DDR6	Port 6 direction register	R/W	Port 6	XXXX 0 0 0 0$_B$
000017$_H$	ADER	Analog input enable register	R/W	Port 5, A/D converter	1 1 1 1 1 1 1 1$_B$
000018$_H$ to 00001F$_H$	Access prohibited				
000020$_H$	SMR0	Mode register ch0	R/W	UART0	0 0 0 0 0 X 0 0$_B$
000021$_H$	SCR0	Control register ch0	W, R/W		0 0 0 0 0 1 0 0$_B$
000022$_H$	SIDR0	Input data register ch0	R		XXXXXXXX$_B$
	SODR0	Output data register ch0	W		
000023$_H$	SSR0	Status register ch0	R, R/W		0 0 0 0 1 0 0 0$_B$
000024$_H$	SMR1	Mode register ch1	R/W	UART1	0 0 0 0 0 X 0 0$_B$
000025$_H$	SCR1	Control register ch1	W, R/W		0 0 0 0 0 1 0 0$_B$
000026$_H$	SIDR1	Input data register ch1	R		XXXXXXXX$_B$
	SODR1	Output data register ch1	W		
000027$_H$	SSR1	Status register ch1	R, R/W		0 0 0 0 1 0 0 0$_B$
000028$_H$	Access prohibited				
000029$_H$	CDCR0	Communication prescaler control register ch0	R/W	Communication prescaler	0 XXX 0 0 0 0$_B$

(Continued)

Address	Abbreviated Register Name	Register name	Read/ Write	Resource Name	Initial Value
00002A$_H$	Access prohibited				
00002B$_H$	CDCR1	Communication prescaler control register ch1	R/W	Communication prescaler	0 XXX 0 0 0 0$_B$
00002C$_H$ to 00002F$_H$	Access prohibited				
000030$_H$	ENIR	DTP/external interrupt enable register	R/W	DTP/external interrupts	0 0 0 0 0 0 0 0$_B$
000031$_H$	EIRR	DTP/external interrupt request register	R/W		XXXXXXXX$_B$
000032$_H$	ELVR	Request level setting register (lower)	R/W		0 0 0 0 0 0 0 0$_B$
000033$_H$		Request level setting register (upper)	R/W		0 0 0 0 0 0 0 0$_B$
000034$_H$	ADCS0	A/D control status register (lower)	R/W	8/10-bit A/D converter	0 0 0 0 0 0 0 0$_B$
000035$_H$	ADCS1	A/D control status register (upper)	W, R/W		0 0 0 0 0 0 0 0$_B$
000036$_H$	ADCR0	A/D data register (lower)	R		XXXXXXXX$_B$
000037$_H$	ADCR1	A/D data register (upper)	R, W		0 0 0 0 0 XXX$_B$
000038$_H$	PRLL0	PPG reload register ch0 (lower)	R/W	8/16-bit PPG timer	XXXXXXXX$_B$
000039$_H$	PRLH0	PPG reload register ch0 (upper)	R/W		XXXXXXXX$_B$
00003A$_H$	PRLL1	PPG reload register ch1 (lower)	R/W		XXXXXXXX$_B$
00003B$_H$	PRLH1	PPG reload register ch1 (upper)	R/W		XXXXXXXX$_B$
00003C$_H$	PPGC0	PPG control register ch0 (lower)	R/W		0 0 0 0 0 0 0 1$_B$
00003D$_H$	PPGC1	PPG control register ch1 (upper)	R/W		0 0 0 0 0 0 0 1$_B$
00003E$_H$	PCS01	PPG clock control register ch0, ch1	R/W		0 0 0 0 0 0 XX$_B$
00003F$_H$	Access prohibited				
000040$_H$	PRLL2	PPG reload register ch2 (lower)	R/W	8/16-bit PPG timer	XXXXXXXX$_B$
000041$_H$	PRLH2	PPG reload register ch2 (upper)	R/W		XXXXXXXX$_B$
000042$_H$	PRLL3	PPG reload register ch3 (lower)	R/W		XXXXXXXX$_B$
000043$_H$	PRLH3	PPG reload register ch3 (upper)	R/W		XXXXXXXX$_B$
000044$_H$	PPGC2	PPG control register ch2 (lower)	R/W		0 0 0 0 0 0 0 1$_B$
000045$_H$	PPGC3	PPG control register ch3 (upper)	R/W		0 0 0 0 0 0 0 1$_B$
000046$_H$	PCS23	PPG clock control register ch2, ch3	R/W		0 0 0 0 0 0 XX$_B$
000047$_H$	Access prohibited				
000048$_H$	PRLL4	PPG reload register ch4 (lower)	R/W	8/16-bit PPG timer	XXXXXXXX$_B$
000049$_H$	PRLH4	PPG reload register ch4 (upper)	R/W		XXXXXXXX$_B$
00004A$_H$	PRLL5	PPG reload register ch5 (lower)	R/W		XXXXXXXX$_B$
00004B$_H$	PRLH5	PPG reload register ch5 (upper)	R/W		XXXXXXXX$_B$
00004C$_H$	PPGC4	PPG control register ch4 (lower)	R/W		0 0 0 0 0 0 0 1$_B$

(Continued)

Address	Abbreviated Register Name	Register name	Read/ Write	Resource Name	Initial Value
00004D$_H$	PPGC5	PPG control register ch5 (upper)	R/W	8/16-bit PPG timer	0 0 0 0 0 0 0 1$_B$
00004E$_H$	PCS45	PPG clock control register ch4, ch5	R/W		0 0 0 0 0 0 XX$_B$
00004F$_H$	Access prohibited				
000050$_H$	TMRR0	8-bit reload register ch0	R/W	Waveform generator	XXXXXXXX$_B$
000051$_H$	DTCR0	8-bit timer control register ch0	R/W		0 0 0 0 0 0 0 0$_B$
000052$_H$	TMRR1	8-bit reload register ch1	R/W		XXXXXXXX$_B$
000053$_H$	DTCR1	8-bit timer control register ch1	R/W		0 0 0 0 0 0 0 0$_B$
000054$_H$	TMRR2	8-bit reload register ch2	R/W		XXXXXXXX$_B$
000055$_H$	DTCR2	8-bit timer control register ch2	R/W		0 0 0 0 0 0 0 0$_B$
000056$_H$	SIGCR	Waveform control register	R/W		0 0 0 0 0 0 0 0$_B$
000057$_H$	Access prohibited				
000058$_H$	CPCLR	Compare clear register (lower)	R/W	16-bit freerun timer	XXXXXXXX$_B$
000059$_H$		Compare clear register (upper)	R/W		XXXXXXXX$_B$
00005A$_H$	TCDT	Timer data register (lower)	R/W		0 0 0 0 0 0 0 0$_B$
00005B$_H$		Timer data register (upper)	R/W		0 0 0 0 0 0 0 0$_B$
00005C$_H$	TCCS	Timer control/status register (lower)	R/W		0 0 0 0 0 0 0 0$_B$
00005D$_H$		Timer control/status register (upper)	R/W		0 XX 0 0 0 0 0$_B$
00005E$_H$	Access prohibited				
00005F$_H$					
000060$_H$	IPCP0	Input capture data register ch0 (lower)	R	Input capture	XXXXXXXX$_B$
000061$_H$		Input capture data register ch0 (upper)	R		XXXXXXXX$_B$
000062$_H$	IPCP1	Input capture data register ch1 (lower)	R		XXXXXXXX$_B$
000063$_H$		Input capture data register ch1 (upper)	R		XXXXXXXX$_B$
000064$_H$	IPCP2	Input capture data register ch2 (lower)	R		XXXXXXXX$_B$
000065$_H$		Input capture data register ch2 (upper)	R		XXXXXXXX$_B$
000066$_H$	IPCP3	Input capture data register ch3 (lower)	R		XXXXXXXX$_B$
000067$_H$		Input capture data register ch3 (upper)	R		XXXXXXXX$_B$
000068$_H$	ICS01	Input capture control register 01	R/W		0 0 0 0 0 0 0 0$_B$
000069$_H$	Access prohibited				
00006A$_H$	ICS23	Input capture control register 23	R/W	Input capture	0 0 0 0 0 0 0 0$_B$
00006B$_H$ to 00006E$_H$	Access prohibited				

(Continued)

Address	Abbreviat-ed Register Name	Register name	Read/ Write	Resource Name	Initial Value
00006F$_H$	ROMM	ROM mirror function selection register	W	ROM mirror function selection module	XXXXXXX 1$_B$
000070$_H$	OCCP0	Compare register ch0 (lower)	R/W	Output compare	XXXXXXXX$_B$
000071$_H$		Compare register ch0 (upper)	R/W		XXXXXXXX$_B$
000072$_H$	OCCP1	Compare register ch1 (lower)	R/W		XXXXXXXX$_B$
000073$_H$		Compare register ch1 (upper)	R/W		XXXXXXXX$_B$
000074$_H$	OCCP2	Compare register ch2 (lower)	R/W		XXXXXXXX$_B$
000075$_H$		Compare register ch2 (upper)	R/W		XXXXXXXX$_B$
000076$_H$	OCCP3	Compare register ch3 (lower)	R/W		XXXXXXXX$_B$
000077$_H$		Compare register ch3 (upper)	R/W		XXXXXXXX$_B$
000078$_H$	OCCP4	Compare register ch4 (lower)	R/W		XXXXXXXX$_B$
000079$_H$		Compare register ch4 (upper)	R/W		XXXXXXXX$_B$
00007A$_H$	OCCP5	Compare register ch5 (lower)	R/W		XXXXXXXX$_B$
00007B$_H$		Compare register ch5 (upper)	R/W		XXXXXXXX$_B$
00007C$_H$	OCS0	Compare control register ch0 (lower)	R/W		0 0 0 0 XX 0 0$_B$
00007D$_H$	OCS1	Compare control register ch1 (upper)	R/W		XXX 0 0 0 0 0$_B$
00007E$_H$	OCS2	Compare control register ch2 (lower)	R/W		0 0 0 0 XX 0 0$_B$
00007F$_H$	OCS3	Compare control register ch3 (upper)	R/W		XXX 0 0 0 0 0$_B$
000080$_H$	OCS4	Compare control register ch4 (lower)	R/W		0 0 0 0 XX 0 0$_B$
000081$_H$	OCS5	Compare control register ch5 (upper)	R/W		XXX 0 0 0 0 0$_B$
000082$_H$	TMCSR0 : L	Timer control status register ch0 (lower)	R/W	16-bit reload timer	0 0 0 0 0 0 0 0$_B$
000083$_H$	TMCSR0 : H	Timer control status register ch0 (upper)	R/W		XXXX 0 0 0 0$_B$
000084$_H$	TMR0	16-bit timer register ch0 (lower)	R		XXXXXXXX$_B$
	TMRLR0	16-bit reload register ch0 (lower)	W		XXXXXXXX$_B$
000085$_H$	TMR0	16-bit timer register ch0 (upper)	R		XXXXXXXX$_B$
	TMRHR0	16-bit reload register ch0 (upper)	W		XXXXXXXX$_B$
000086$_H$	TMCSR1 : L	Timer control status register ch1 (lower)	R/W		0 0 0 0 0 0 0 0$_B$
000087$_H$	TMCSR1 : H	Timer control status register ch1 (upper)	R/W		XXXX 0 0 0 0$_B$
000088$_H$	TMR1	16-bit timer register ch1 (lower)	R		XXXXXXXX$_B$
	TMRLR1	16-bit reload register ch1 (lower)	W		XXXXXXXX$_B$
000089$_H$	TMR1	16-bit timer register ch1 (upper)	R		XXXXXXXX$_B$
	TMRHR1	16-bit reload register ch1 (upper)	W		XXXXXXXX$_B$

(Continued)

Address	Abbreviat-ed Register Name	Register name	Read/ Write	Resource Name	Initial Value
00008A$_H$ to 00008B$_H$	Access prohibited				
00008C$_H$	RDR0	Port 0 pull-up resistor setting register	R/W	Port 0	0 0 0 0 0 0 0 0$_B$
00008D$_H$	RDR1	Port 1 pull-up resistor setting register	R/W	Port 1	0 0 0 0 0 0 0 0$_B$
00008E$_H$ to 00009D$_H$	Access prohibited				
00009E$_H$	PACSR	Program address detection control status register	R/W	Address match detection	0 0 0 0 0 0 0 0$_B$
00009F$_H$	DIRR	Delayed interrupt request/clear register	R/W	Delayed interrupt	XXXXXXX 0$_B$
0000A0$_H$	LPMCR	Low power consumption mode register	W, R/W	Low power consumption control circuit	0 0 0 1 1 0 0 0$_B$
0000A1$_H$	CKSCR	Clock selection register	R, R/W	Clock	1 1 1 1 1 1 0 0$_B$
0000A2$_H$ to 0000A7$_H$	Access prohibited				
0000A8$_H$	WDTC	Watchdog control register	R/W	Watchdog timer	1 XXXX 1 1 1$_B$
0000A9$_H$	TBTC	Timebase timer control register	W, R/W	Timebase timer	1 XX 0 0 1 0 0$_B$
0000AA$_H$ to 0000AD$_H$	Access prohibited				
0000AE$_H$	FMCS	Flash memory control status register	R, W, R/W	Flash memory	0 0 0 0 0 0 0 0$_B$
0000AF$_H$	Access prohibited				
0000B0$_H$	ICR00	Interrupt control register 00 (for writing)	W, R/W	Interrupts	XXXX 0 1 1 1$_B$
		Interrupt control register 00 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000B1$_H$	ICR01	Interrupt control register 01 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 01 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000B2$_H$	ICR02	Interrupt control register 02 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 02 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000B3$_H$	ICR03	Interrupt control register 03 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 03 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000B4$_H$	ICR04	Interrupt control register 04 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 04 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000B5$_H$	ICR05	Interrupt control register 05 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 05 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$

(Continued)

Address	Abbreviated Register Name	Register name	Read/ Write	Resource Name	Initial Value
0000B6$_H$	ICR06	Interrupt control register 06 (for writing)	W, R/W	Interrupts	XXXX 0 1 1 1$_B$
		Interrupt control register 06 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000B7$_H$	ICR07	Interrupt control register 07 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 07 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000B8$_H$	ICR08	Interrupt control register 08 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 08 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000B9$_H$	ICR09	Interrupt control register 09 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 09 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000BA$_H$	ICR10	Interrupt control register 10 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 10 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000BB$_H$	ICR11	Interrupt control register 11 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 11 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000BC$_H$	ICR12	Interrupt control register 12 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 12 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000BD$_H$	ICR13	Interrupt control register 13 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 13 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000BE$_H$	ICR14	Interrupt control register 14 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 14 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000BF$_H$	ICR15	Interrupt control register 15 (for writing)	W, R/W		XXXX 0 1 1 1$_B$
		Interrupt control register 15 (for reading)	R, R/W		XX 0 0 0 1 1 1$_B$
0000C0$_H$ to 0000FF$_H$	Unused area				
000100$_H$ to #$_H$	RAM area				
#$_H$ to 001FEF$_H$	Reserved area				
001FF0$_H$	PADR0	Program address detection register ch0 (lower)	R/W	Address match detection	XXXXXXXX$_B$
001FF1$_H$		Program address detection register ch0 (middle)	R/W		XXXXXXXX$_B$
001FF2$_H$		Program address detection register ch0 (lower)	R/W		XXXXXXXX$_B$

(Continued)

(Continued)

Address	Abbreviat-ed Register Name	Register name	Read/ Write	Resource Name	Initial Value
001FF3H	PADR1	Program address detection register ch1 (lower)	R/W	Address match detection	XXXXXXXXB
001FF4H		Program address detection register ch1 (middle)	R/W		XXXXXXXXB
001FF5H		Program address detection register ch1 (lower)	R/W		XXXXXXXXB
001FF6H to 001FFFH	Unused area				

- Read/write notation

R/W : Reading and writing permitted
R : Read-only
W : Write-only

- Initial value notation

0 : Initial value is “0”.
1 : Initial value is “1”.
X : Initial value is undefined.

■ INTERRUPTS, INTERRUT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt	EI^{2}OS Support	Interrupt Vector			Interrupt Control Register		Priority
		No.*		Address	ICR	Address	
Reset	×	#08	08$_H$	FFFFDC$_H$	—	—	High
INT 9 instruction	×	#09	09$_H$	FFFFD8$_H$	—	—	
Exception	×	#10	0A$_H$	FFFFD4$_H$	—	—	
A/D converter conversion complete	○	#11	0B$_H$	FFFFD0$_H$	ICR00	0000B0$_H$	
Output compare channel 0 match	△	#13	0D$_H$	FFFFC8$_H$	ICR01	0000B1$_H$	
8/16-bit PPG timer 0 counter borrow	△	#14	0E$_H$	FFFFC4$_H$			
Output compare channel 1 match	△	#15	0F$_H$	FFFFC0$_H$	ICR02	0000B2$_H$	
8/16-bit PPG timer 1 counter borrow	△	#16	10$_H$	FFFFBC$_H$			
Output compare channel 2 match	△	#17	11$_H$	FFFFB8$_H$	ICR03	0000B3$_H$	
8/16-bit PPG timer 2 counter borrow	△	#18	12$_H$	FFFFB4$_H$			
Output compare channel 3 match	△	#19	13$_H$	FFFFB0$_H$	ICR04	0000B4$_H$	
8/16-bit PPG timer 3 counter borrow	△	#20	14$_H$	FFFFAC$_H$			
Output compare channel 4 match	△	#21	15$_H$	FFFFA8$_H$	ICR05	0000B5$_H$	
8/16-bit PPG timer 4 counter borrow	△	#22	16$_H$	FFFFA4$_H$			
Output compare channel 5 match	△	#23	17$_H$	FFFFA0$_H$	ICR06	0000B6$_H$	
8/16-bit PPG timer 5 counter borrow	△	#24	18$_H$	FFFF9C$_H$			
DTP/external interrupt channel 0/1 detection	△	#25	19$_H$	FFFF98$_H$	ICR07	0000B7$_H$	
DTP/external interrupt channel 2/3 detection	△	#26	1A$_H$	FFFF94$_H$			
DTP/external interrupt channel 4/5 detection	△	#27	1B$_H$	FFFF90$_H$	ICR08	0000B8$_H$	
DTP/external interrupt channel 6/7 detection	△	#28	1C$_H$	FFFF8C$_H$			
8-bit timer 0/1/2 counter borrow	×	#29	1D$_H$	FFFF88$_H$	ICR09	0000B9$_H$	
16-bit reload timer 0 underflow	○	#30	1E$_H$	FFFF84$_H$			
16-bit freerun timer overflow	×	#31	1F$_H$	FFFF80$_H$	ICR10	0000BA$_H$	
16-bit reload timer 1 underflow	○	#32	20$_H$	FFFF7C$_H$			
Input capture channel 0/1	○	#33	21$_H$	FFFF78$_H$	ICR11	0000BB$_H$	
16-bit freerun timer clear	×	#34	22$_H$	FFFF74$_H$			
Input capture channel 2/3	○	#35	23$_H$	FFFF70$_H$	ICR12	0000BC$_H$	
Timebase timer	×	#36	24$_H$	FFFF6C$_H$			
UART1 receive	◎	#37	25$_H$	FFFF68$_H$	ICR13	0000BD$_H$	
UART1 send	△	#38	26$_H$	FFFF64$_H$			
UART0 receive	◎	#39	27$_H$	FFFF60$_H$	ICR14	0000BE$_H$	
UART0 send	△	#40	28$_H$	FFFF5C$_H$			
Flash memory status	×	#41	29$_H$	FFFF58$_H$	ICR15	0000BF$_H$	
Delay interrupt output module	×	#42	2A$_H$	FFFF54$_H$			Low

○ : Supported

× : Not supported

◎ : Supported, includes EI^{2}OS stop function

△ : Available if the interrupt that shares the same ICR is not used.

* : If two or more interrupts with the same level occur simultaneously, the interrupt with the lower interrupt vector number has priority

■ PERIPHERAL FUNCTIONS

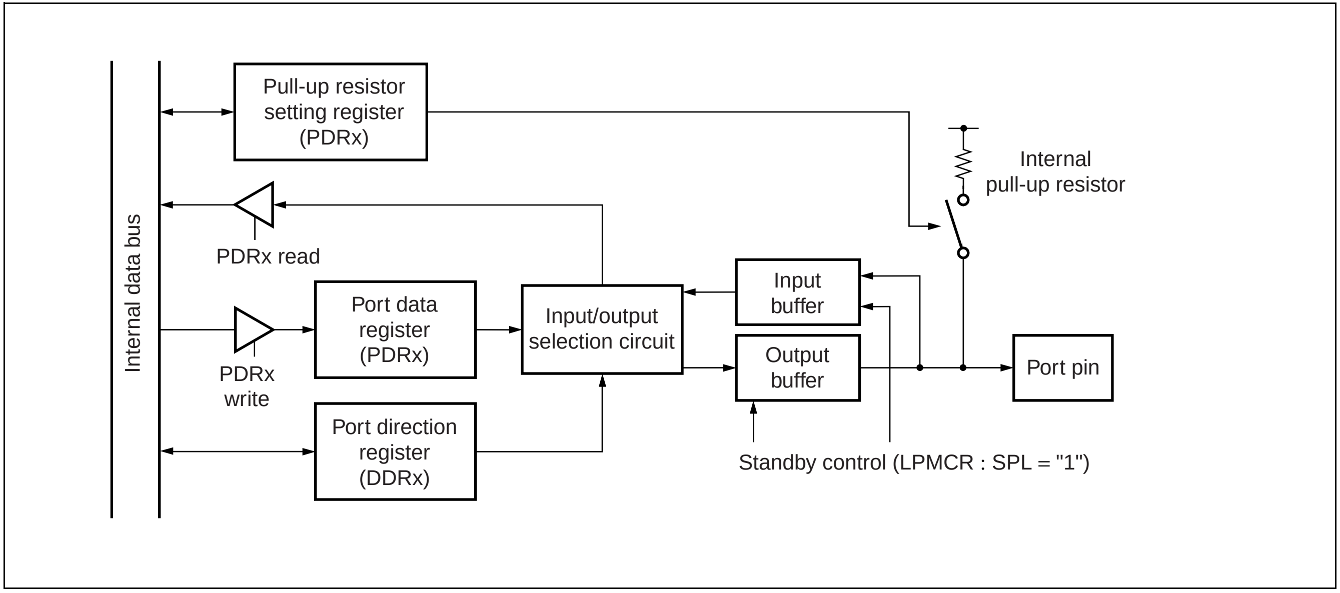
1. I/O Ports

- The I/O ports can be used as general-purpose I/O ports (parallel I/O ports) . The MB90560/565 series have 7 ports (51 pins) . The ports share pins with the inputs and outputs of the peripheral functions.
- The port data registers (PDR) are used to output data to the I/O pins and read the data input from the I/O ports. Similarly, the port direction registers (DDR) set the I/O direction (input or output) for each individual port bit.
- The following table lists the I/O ports and the peripheral functions with which they share pins.

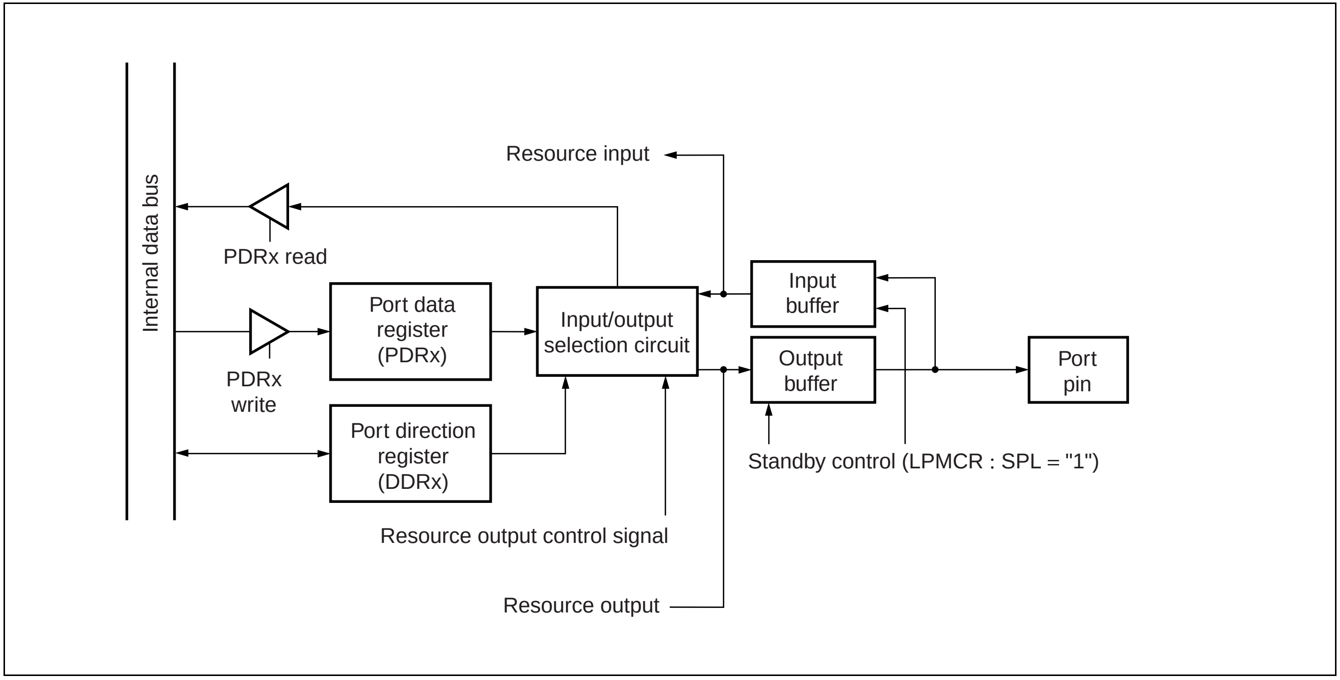
	Pin Name (Port)	Pin Name (Peripheral)	Peripheral Function that Shares Pin
Port 0	P00-P07	—	Not shared
Port 1	P10-P16	INT0-INT6	External interrupts
	P17	FRCK	Freerun timer external input
Port 2	P20-P23	TIN0, TO0, TIN1, TO1	16-bit reload timer 0 and 1
	P24-P27	IN0-IN3	Input capture 0 to 3
Port 3	P30-P35	RTO0-RTO5	Output compare
	P36, P37	SIN0, SOT0	UART0
Port 4	P40	SCK0	UART0
	P41-P46	PPG0-PPG5	8/16-bit PPG timer
Port 5	P50-P57	AN0-AN7	8/10-bit A/D converter
Port 6	P60-P62	SIN1, SOT1, SCK1	UART1
	P63	INT7	External interrupts
		DTTI	Waveform generator

Notes : • Pins P30 to P35 of port 3 can drive a maximum of I_{OL} = 12 mA.
• Port 5 shares pins with the analog inputs. When using port 5 pins as a general-purpose ports, ensure that the corresponding analog input enable register (ADER) bits are set to “0_B”. ADER is initialized to “FF_H” after a reset.

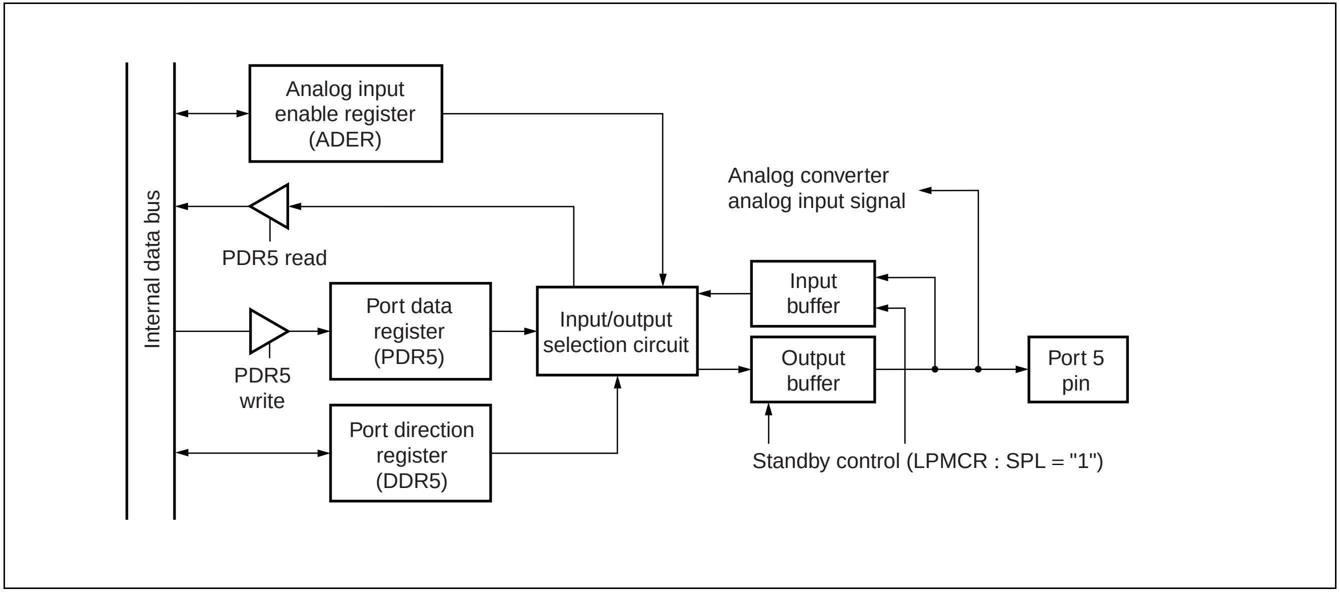
- **Block diagram for port 0 and 1 pins**


Internal data bus
Pull-up resistor setting register (PDRx)
Internal pull-up resistor
PDRx read
Port data register (PDRx)
Input/output selection circuit
Input buffer
Output buffer
Port pin
PDRx write
Port direction register (DDRx)
Standby control (LPMCR : SPL = "1")

- **Block diagram for port 2, 3, 4, and 6 pins**


Internal data bus
Resource input
PDRx read
Port data register (PDRx)
Input/output selection circuit
Input buffer
Output buffer
Port pin
PDRx write
Port direction register (DDRx)
Standby control (LPMCR : SPL = "1")
Resource output control signal
Resource output

- **Block diagram for port 5 pins**


Internal data bus
Analog input enable register (ADER)
Analog converter analog input signal
PDR5 read
Port data register (PDR5)
Input/output selection circuit
Input buffer
Output buffer
Port 5 pin
PDR5 write
Port direction register (DDR5)
Standby control (LPMCR : SPL = "1")

Notes : • When using as an input port, set the corresponding bit in the port 5 direction register (DDR5) to “0” and set the corresponding bit in the analog input enable register (ADER) to “0”.

- When using as an analog input pin, set the corresponding bit in the port 5 direction register (DDR5) to “0” and set the corresponding bit in the analog input enable register (ADER) to “1”.

2. Timebase Timer

- The timebase timer is an 18-bit freerun timer (timebase timer/counter) that counts up synchronized with the main clock (oscillation clock : HCLK divided into 2) .
- The timer can generate interrupt requests at a specified interval, with four different interval time settings available.
- The timer supplies the operating clock for peripheral functions including the oscillation stabilization delay timer and watchdog timer.

- **Timebase timer interval settings**

Internal Count Clock Period	Interval Time
2/HCLK (0.5 µs)	2^{12}/HCLK (approx. 1.024 ms)
	2^{14}/HCLK (approx. 4.096 ms)
	2^{16}/HCLK (approx. 16.384 ms)
	2^{19}/HCLK (approx. 131.072 ms)

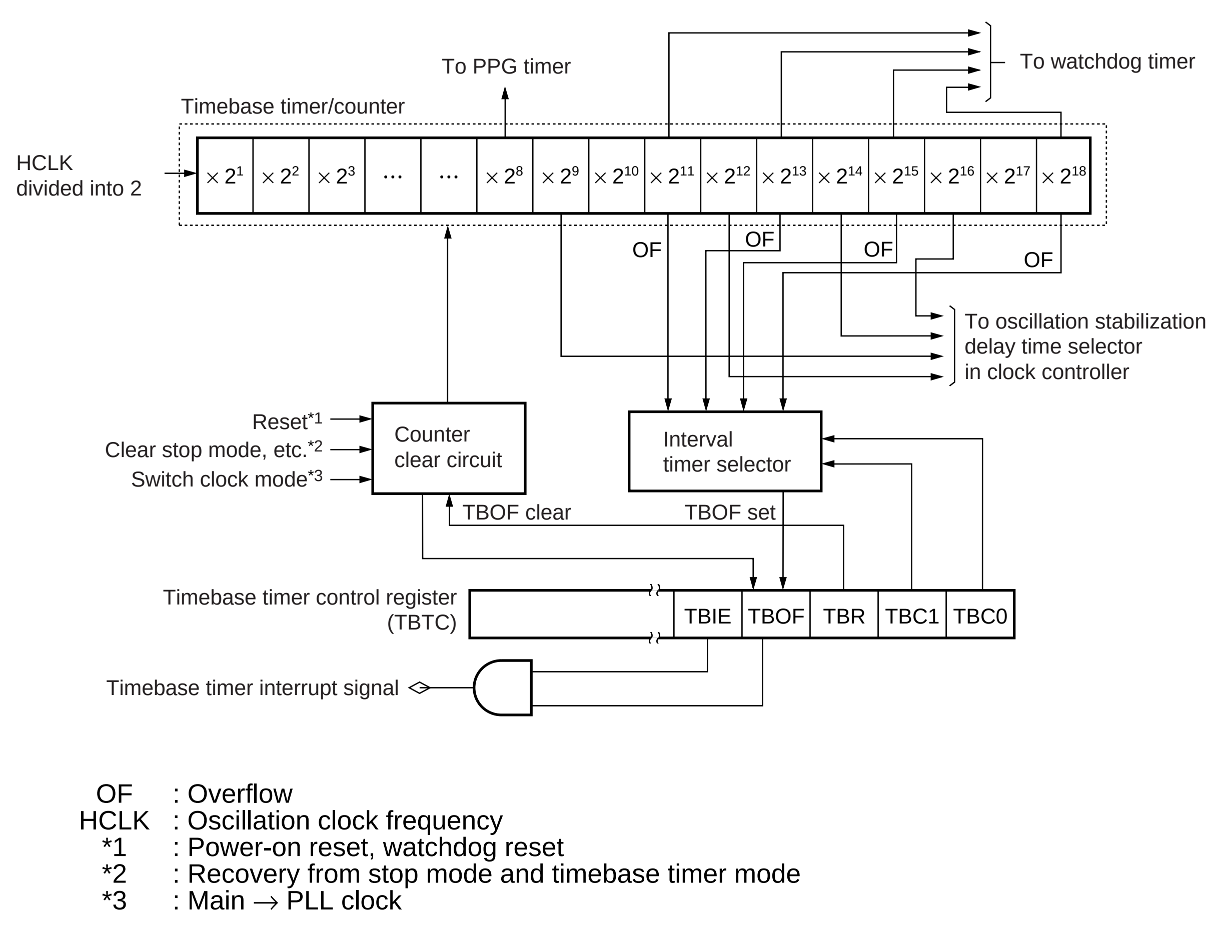
Notes : • HCLK : Oscillation clock frequency
• The values enclosed in ( ) indicate the times for a clock frequency of 4 MHz.

- **Period of clocks supplied from timebase timer**

Peripheral Function	Clock Period
Oscillation stabilization delay for the main clock	2^{10}/HCLK (approx. 0.256 ms)
	2^{13}/HCLK (approx. 2.048 ms)
	2^{15}/HCLK (approx. 8.192 ms)
	2^{17}/HCLK (approx. 32.768 ms)
Watchdog timer	2^{12}/HCLK (approx. 1.024 ms)
	2^{14}/HCLK (approx. 4.096 ms)
	2^{16}/HCLK (approx. 16.384 ms)
	2^{19}/HCLK (approx. 131.072 ms)

Notes : • HCLK : Oscillation clock frequency
• The values enclosed in ( ) indicate the times for a clock frequency of 4 MHz.

- **Block diagram**


To PPG timer
To watchdog timer
Timebase timer/counter
HCLK
divided into 2
$\times 2^{1}$
$\times 2^{2}$
$\times 2^{3}$
···
···
$\times 2^{8}$
$\times 2^{9}$
$\times 2^{10}$
$\times 2^{11}$
$\times 2^{12}$
$\times 2^{13}$
$\times 2^{14}$
$\times 2^{15}$
$\times 2^{16}$
$\times 2^{17}$
$\times 2^{18}$
OF
OF
OF
OF
To oscillation stabilization
delay time selector
in clock controller
Reset*1
Clear stop mode, etc.*2
Switch clock mode*3
Counter
clear circuit
Interval
timer selector
TBOF clear
TBOF set
Timebase timer control register
(TBTC)
TBIE
TBOF
TBR
TBC1
TBC0
Timebase timer interrupt signal

OF : Overflow
HCLK : Oscillation clock frequency
*1 : Power-on reset, watchdog reset
*2 : Recovery from stop mode and timebase timer mode
*3 : Main → PLL clock

The actual interrupt request number for the timebase timer is :
Interrupt request number : #36 (24_H)

3. Watchdog Timer

- The watchdog timer is a timer/counter used to detect faults such as program runaway.
- The watchdog timer is a 2-bit counter that counts the clock signal from the timebase timer or clock timer.
- Once started, the watchdog timer must be cleared before the 2-bit counter overflows. If an overflow occurs, the CPU is reset.

- **Interval time for the watchdog timer**

HCLK : Oscillation Clock (4 MHz)		
Min.	**Max.**	**Clock Period**
Approx. 3.58 ms	Approx. 4.61 ms	$2^{14} \pm 2^{11}$ / HCLK
Approx. 14.33 ms	Approx. 18.30 ms	$2^{16} \pm 2^{13}$ / HCLK
Approx. 57.23 ms	Approx. 73.73 ms	$2^{18} \pm 2^{15}$ / HCLK
Approx. 458.75 ms	Approx. 589.82 ms	$2^{18} \pm 2^{15}$ / HCLK

Notes : • The difference between the maximum and minimum watchdog timer interval times is due to the timing when the counter is cleared.

• As the watchdog timer is a 2-bit counter that counts the carry-up signal from the timebase timer or clock timer, clearing the timebase timer (when operating on HCLK) or the clock timer (when operating on SCLK) lengthens the time until the watchdog timer reset is generated.

- **Watchdog timer count clock**

WTC : WDCS	HCLK : Oscillation clock PCLK : PLL clock
“0”	Prohibited setting
“1”	Count the timebase timer output.

- **Events that stop the watchdog timer**

1 : Stop due to a power-on reset

2 : Watchdog reset

- **Events that clear the watchdog timer**

1 : External reset input from the $\overline{\text{RST}}$ pin.

2 : Writing “0” to the software reset bit.

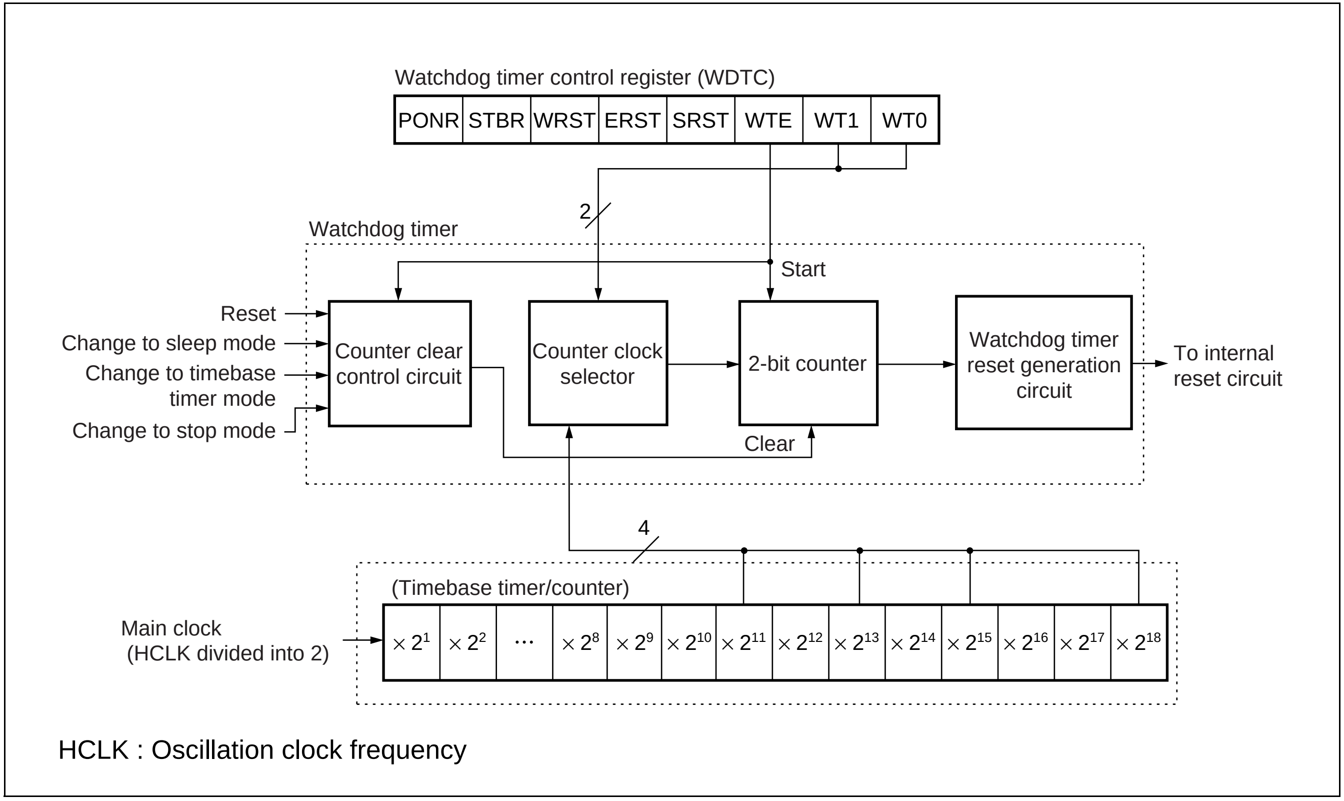
3 : Writing “0” to the watchdog control bit (second and subsequent times) .

4 : Changing to sleep mode (clears the watchdog timer and temporarily halts the count) .

5 : Changing to timebase timer mode (clears the watchdog timer and temporarily halts the count) .

6 : Changing to stop mode (clears the watchdog timer and temporarily halts the count) .

- **Block diagram**


Watchdog timer control register (WDTC)
PONR
STBR
WRST
ERST
SRST
WTE
WT1
WT0
2
Watchdog timer
Start
Reset
Change to sleep mode
Change to timebase timer mode
Change to stop mode
Counter clear control circuit
Counter clock selector
2-bit counter
Watchdog timer reset generation circuit
To internal reset circuit
Clear
4
(Timebase timer/counter)
Main clock (HCLK divided into 2)
× 2^1
× 2^2
…
× 2^8
× 2^9
× 2^10
× 2^11
× 2^12
× 2^13
× 2^14
× 2^15
× 2^16
× 2^17
× 2^18
HCLK : Oscillation clock frequency

4. 16-Bit Reload Timers 0 and 1 (With Event Count Function)

- The 16-bit reload timers have the following functions.
- The count clock can be selected from three internal clocks or the external event clock.
- An interrupt to the CPU can be generated when an underflow occurs on 16-bit reload timer 0 or 1. This interrupt allows the timers to be used as interval timers.
- Two different operation modes can be selected when an underflow occurs on 16-bit reload timer 0 or 1: one-shot mode in which timer operation halts when an underflow occurs or reload mode in which the value in the reload register is loaded into the timer and counting continues.
- Extended intelligent I/O service (EI^{2}OS) is supported.
- The MB90560/565 series contains two 16-bit reload timer channels.

- **16-bit reload timer operation modes**

Count Clock	Start Trigger	Operation When an Underflow Occurs
Internal clock	Software trigger	One-shot mode
		Reload mode
	External trigger	One-shot mode
		Reload mode
Event count mode (external clock mode)	Software trigger	One-shot mode
		Reload mode

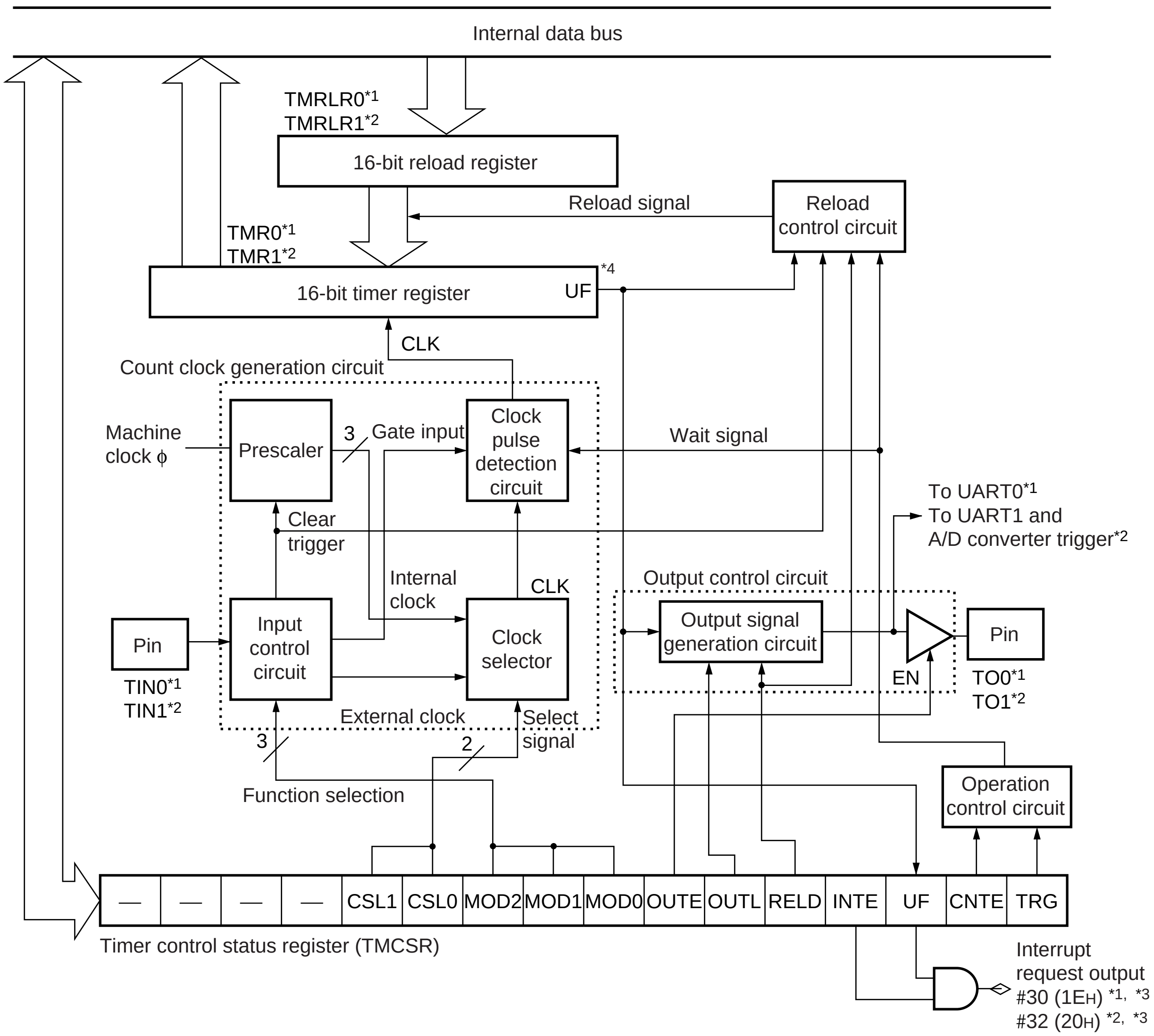
- **Interval times for the 16-bit reload timers**

Count Clock	Count Clock Period	Example of Interval Times
Internal clock	$2^1/\phi$ (0.125 μs)	0.125 μs to 8.192 ms
	$2^3/\phi$ (0.5 μs)	0.5 μs to 32.768 ms
	$2^5/\phi$ (2.0 μs)	2.0 μs to 131.1 ms
Event count mode	$2^3/\phi$ or longer	0.5 μs or longer

Note : The values enclosed in ( ) and the example of interval times is for a machine clock frequency of 16 MHz.
ϕ is the machine clock frequency value for the calculation.

Remarks : 16-bit reload timer 0 can be used to generate the baud rate for UART0.
16-bit reload timer 1 can be used to generate the baud rate for UART1 and activation trigger for the A/D converter.

- **Block diagram**


Internal data bus
TMRLR0*1
TMRLR1*2
16-bit reload register
Reload signal
Reload control circuit
TMR0*1
TMR1*2
16-bit timer register
UF
*4
CLK
Count clock generation circuit
Machine clock ϕ
Prescaler
3
Gate input
Clock pulse detection circuit
Wait signal
Clear trigger
To UART0*1
To UART1 and A/D converter trigger*2
Internal clock
CLK
Output control circuit
Pin
Input control circuit
Clock selector
Output signal generation circuit
Pin
TIN0*1
TIN1*2
EN
TO0*1
TO1*2
External clock
Select signal
3
2
Function selection
Operation control circuit
—
—
—
—
CSL1
CSL0
MOD2
MOD1
MOD0
OUTE
OUTL
RELD
INTE
UF
CNTE
TRG
Timer control status register (TMCSR)
Interrupt request output
#30 (1EH) *1, *3
#32 (20H) *2, *3

*1 : Channel 0
*2 : Channel 1
*3 : Interrupt number
*4 : Underflow

5. Multi-Function Timer

- Based on the 16-bit freerun timer, the multi-function timer can be used to generate 12 independent waveform outputs and to measure input pulse widths and external clock periods.

- **Structure of multi-function timer**

16-bit freerun timer	16-bit output compare	16-bit input capture	8/16-bit PPG timer	Waveform generator
1 ch	6 ch	4 ch	8 bit × 6 ch 16 bit × 3 ch	8-bit timer × 3 ch

- **16-bit freerun timer (1 channel)**

The 16-bit freerun timer consists of a 16-bit up-counter (timer data register (TCDT)) , compare clear register (CPCLR) , timer control status register (TCCS) , and prescaler.

The count output value from the 16-bit freerun timer provides the base time for the input capture and output compare functions.

- The count clock can be selected from the following eight clocks :
  1/φ, 2/φ, 4/φ, 8/φ, 16/φ, 32/φ, 64/φ, 128/φ
  φ : Machine clock frequency
- An interrupt can be generated when the 16-bit freerun timer overflows or when the 16-bit freerun timer count is cleared to “0000_H” due to a match occurring between the value in the compare clear register (CPCLR) and the count in the 16-bit freerun timer (TCCS : ICRE = “1”, MODE = “1”) .
- The 16-bit freerun timer is cleared to “0000_H” when a reset occurs, on setting the timer clear bit (SCLR) in the timer control status register (TCCS) , when a compare match occurs between the 16-bit freerun timer count and the value in the compare clear register (CPCLR) (TCCS : MODE = “1”) , or by writing “0000_H” to the timer data register (TCDT) .

- **Output compare (6 channels)**

The output compare unit consists of compare registers (OCCP0 to OCCP5) , compare control registers (OCS0 to OCS5) , and compare output latches.

When a match occurs between a compare register (OCCP0 to OCCP5) value and the count from the 16-bit freerun timer, the output compare can invert the level of the corresponding output compare pin and generate an interrupt.

- The compare registers (OCCP0 to OCCP5) operate independently for each channel. Each of the compare registers (OCCP0 to OCCP5) has a corresponding output pin and an interrupt request flag in the channel’s compare control register (lower) (OCS0, OCS2, OCS4) .
- Two channels of the compare registers (OCCP0 to OCCP5) can be used to invert the output pins.
- An interrupt can be output when a match occurs between a compare register (OCCP0 to OCCP5) and the count from the 16-bit freerun timer (OCS0, OCS2, OCS4 : IOP0 = “1”, IOP1 = “1”) . (OCS0, OCS2, OCS4 : IOE0 = “1”, IOE1 = “1”)
- The initial output levels for the output compare pins can be set.

- **Input capture (4 channels)**

The input capture consists of external input pins (IN0 to IN3) , corresponding input capture data registers (IPCP0 to IPCP3) , and input capture control status registers (ICS01, ICS23) .
The input capture can transfer the count value from the 16-bit freerun timer to the input capture data register (IPCP0 to IPCP3) and output an interrupt on detecting an active edge on the signal input from the external input pin.

- Each channel of the input capture operates independently.
- The active edge (rising edge, falling edge, or either edge) on the external signal can be specified.

- An interrupt can be generated when an active edge is detected on the external signal (ICS01, ICS23 : ICE0 = “1”, ICE1 = “1”, ICE2 = “1”, ICE3 = “1”) .

- **8/16-bit PPG timer (8-bit : 6 channels, 16-bit : 3 channels)**

The 8/16-bit PPG timer consists of an 8-bit down counter (PCNT) , PPG control registers (PPGC0 to PPGC 5) , PPG clock control registers (PCS01, PCS23, PCS45) , and PPG reload registers (PRLL0 to PRLL5, PRLH0 to PRLH5) .
When used as an 8/16-bit reload timer, the PPG operates as an event timer. The PPG can also be used to output pulses with specified frequency and duty ratio.

- 8-bit PPG mode
  Each channel operates as an independent 8-bit PPG.
- 8-bit prescaler + 8-bit PPG mode
  ch0 (ch2, ch4) operates as an 8-bit prescaler and ch1 (ch3, ch5) operates as a variable frequency PPG by counting up on the borrow output from ch0 (ch2, ch4) .
- 16-bit PPG mode
  ch0 (ch2, ch4) and ch1 (ch3, ch5) operate together as a 16-bit PPG.
- PPG operation
  Outputs pulses with the specified frequency and duty ratio (ratio of “H” level period and “L” level period), and can also be used as a D/A converter when combined with an external circuit.

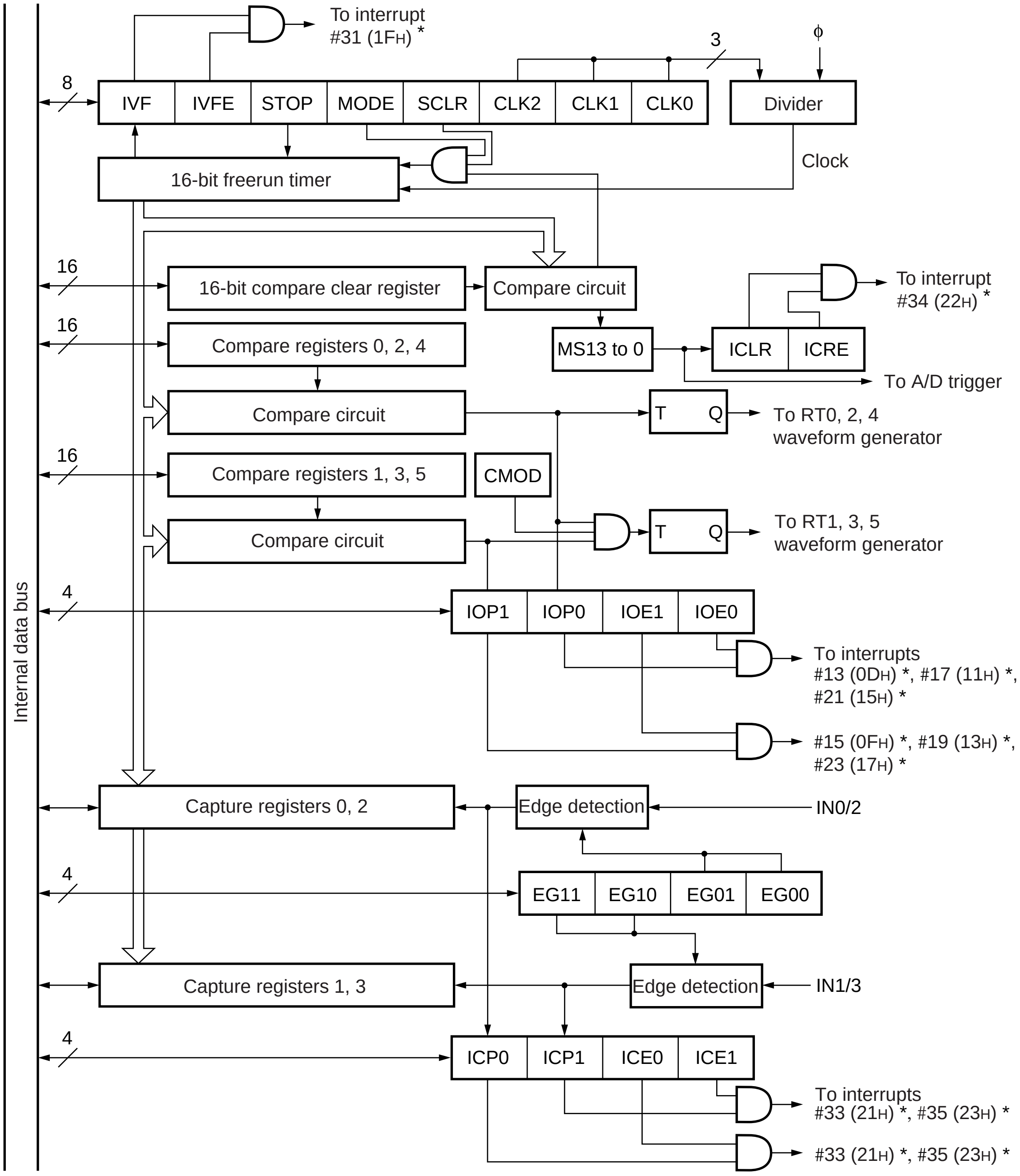
- **Waveform generator**

The waveform generator consists of an 8-bit timer, 8-bit timer control registers (DTCR0 to DTCR2) , 8-bit reload registers (TMRR0 to TMRR2) , and waveform control register (SIGCR) .

The waveform generator can generate a DC chopper output or non-overlapping three-phase waveform output for inverter control using the realtime outputs (RT0 to RT5) and 8/16-bit PPG timer.

- A non-overlapping waveform can be generated by using the 8-bit timer as a deadtime timer and adding a non-overlap time delay to the PPG timer pulse output. (Deadtime timer function)
- A non-overlapping waveform can be generated by using the 8-bit timer as a deadtime timer and adding a non-overlap time delay to the realtime outputs (RT1, RT3, RT5) . (Deadtime timer function)
- A GATE signal can be generated when a match occurs between the count from the 16-bit freerun timer and compare register in the output compare (OCCP0 to OCCP5) (rising edge on realtime output (RT)) to control the PPG timer operation. (GATE function)
- Can control the RTO0 to RTO5 pin outputs using the DTTI pin input.
  By making the DTTI pin input clockless, the pins can be controlled externally even when the oscillation clock is halted. (The level for each pin can be set by the program.) However, the I/O ports (P30 to P35) must have been set beforehand as outputs and the output values set in the port 3 data register (PDR3) .

- **Block diagram**
- **16-bit freerun timer, input capture, and output compare**

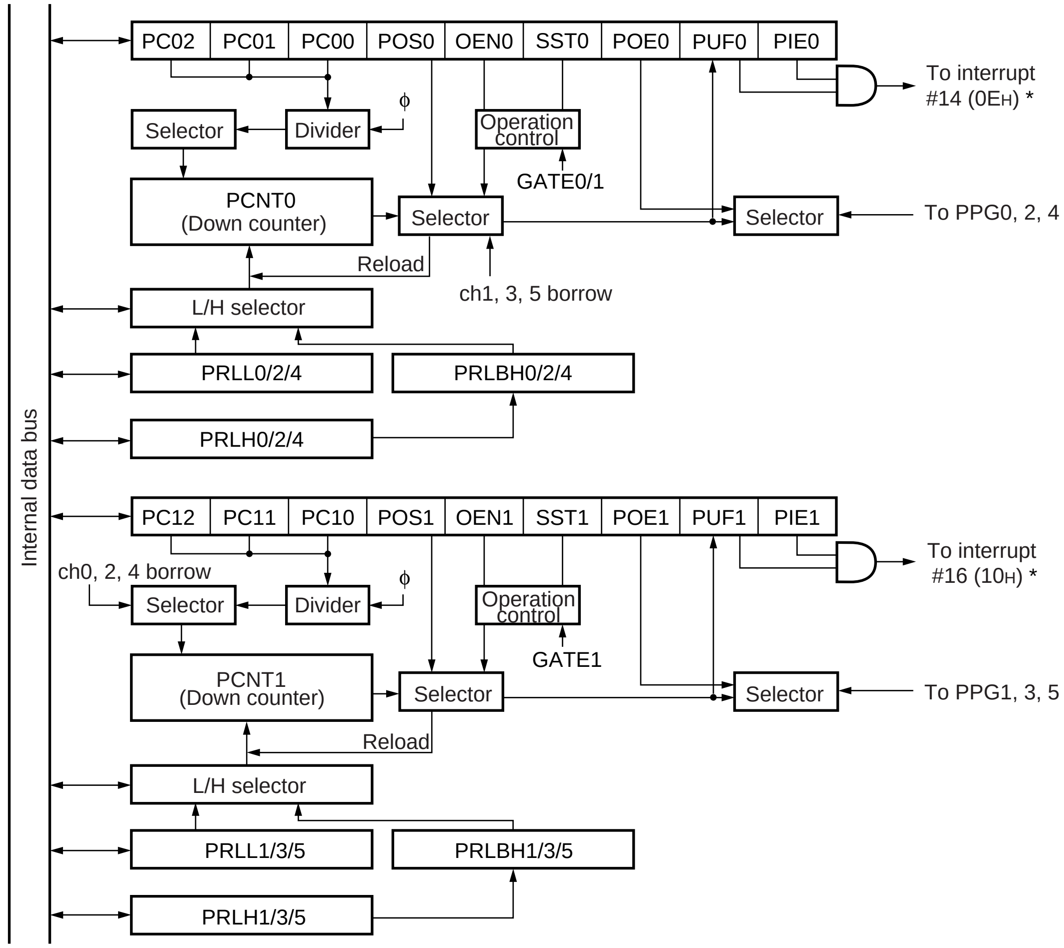


To interrupt #31 (1FH) *
3
ϕ
8
IVF
IVFE
STOP
MODE
SCLR
CLK2
CLK1
CLK0
Divider
Clock
16-bit freerun timer
16
16-bit compare clear register
Compare circuit
To interrupt #34 (22H) *
16
Compare registers 0, 2, 4
MS13 to 0
ICLR
ICRE
To A/D trigger
Compare circuit
T
Q
To RT0, 2, 4 waveform generator
16
Compare registers 1, 3, 5
CMOD
Compare circuit
T
Q
To RT1, 3, 5 waveform generator
Internal data bus
4
IOP1
IOP0
IOE1
IOE0
To interrupts #13 (0DH) *, #17 (11H) *, #21 (15H) *
#15 (0FH) *, #19 (13H) *, #23 (17H) *
Capture registers 0, 2
Edge detection
IN0/2
4
EG11
EG10
EG01
EG00
Capture registers 1, 3
Edge detection
IN1/3
4
ICP0
ICP1
ICE0
ICE1
To interrupts #33 (21H) *, #35 (23H) *
#33 (21H) *, #35 (23H) *

* : Interrupt number

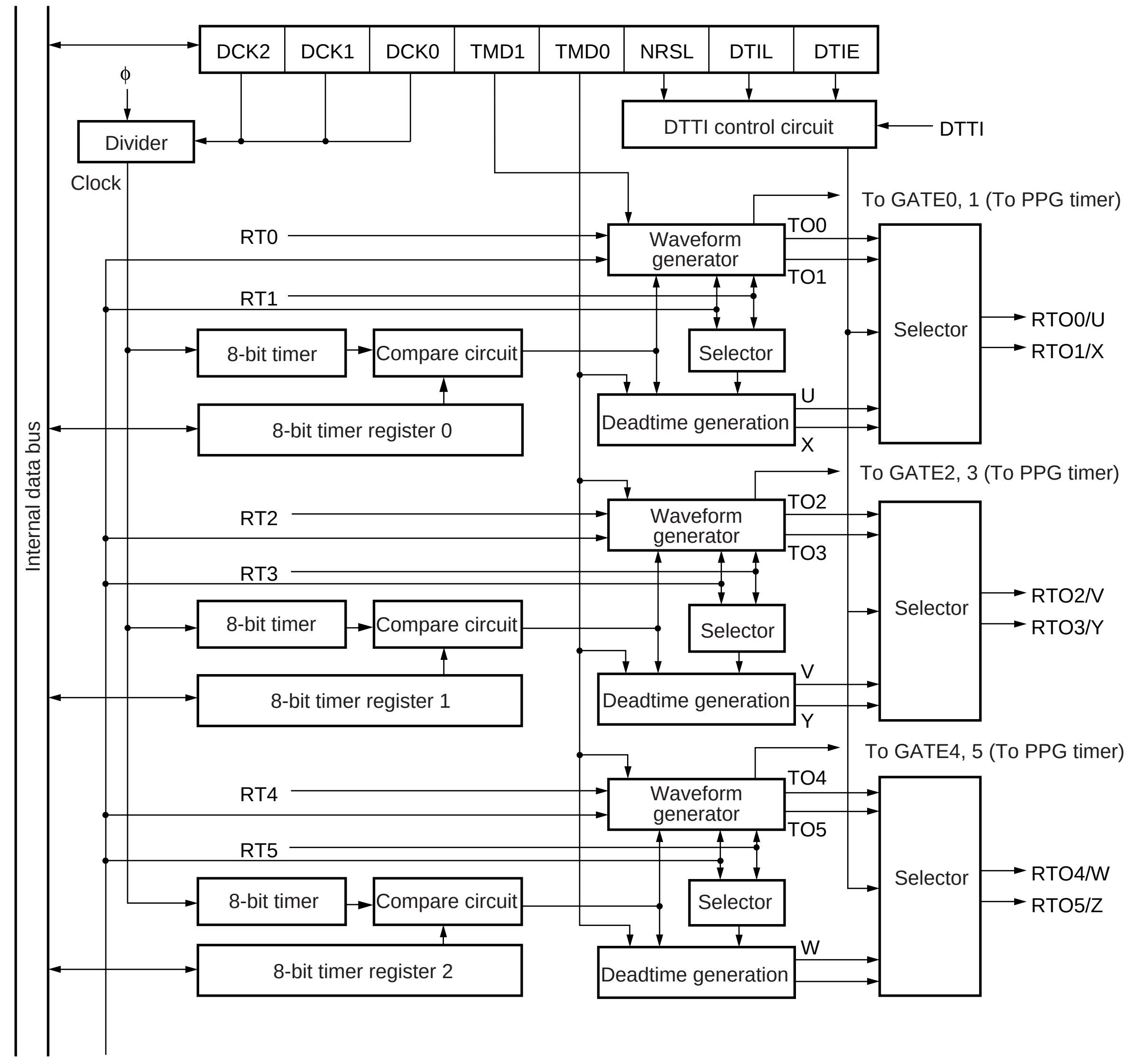
ϕ : Machine clock frequency

- **Block diagram of 8/16-bit PPG timer**


PC02
PC01
PC00
POS0
OEN0
SST0
POE0
PUF0
PIE0
To interrupt #14 (0EH) *
ϕ
Selector
Divider
Operation control
GATE0/1
PCNT0 (Down counter)
Selector
Selector
To PPG0, 2, 4
Reload
ch1, 3, 5 borrow
L/H selector
PRLL0/2/4
PRLBH0/2/4
PRLH0/2/4
Internal data bus
PC12
PC11
PC10
POS1
OEN1
SST1
POE1
PUF1
PIE1
To interrupt #16 (10H) *
ch0, 2, 4 borrow
ϕ
Selector
Divider
Operation control
GATE1
PCNT1 (Down counter)
Selector
Selector
To PPG1, 3, 5
Reload
L/H selector
PRLL1/3/5
PRLBH1/3/5
PRLH1/3/5

* : Interrupt number
ϕ : Machine clock frequency

- **Block diagram of waveform generator**


DCK2
DCK1
DCK0
TMD1
TMD0
NRSL
DTIL
DTIE
ϕ
Divider
Clock
DTTI control circuit
DTTI
To GATE0, 1 (To PPG timer)
RT0
Waveform generator
TO0
TO1
RT1
Selector
RTO0/U
RTO1/X
8-bit timer
Compare circuit
Selector
Deadtime generation
U
X
8-bit timer register 0
Internal data bus
To GATE2, 3 (To PPG timer)
RT2
Waveform generator
TO2
TO3
RT3
Selector
RTO2/V
RTO3/Y
8-bit timer
Compare circuit
Selector
Deadtime generation
V
Y
8-bit timer register 1
To GATE4, 5 (To PPG timer)
RT4
Waveform generator
TO4
TO5
RT5
Selector
RTO4/W
RTO5/Z
8-bit timer
Compare circuit
Selector
Deadtime generation
W
8-bit timer register 2

ϕ : Machine clock frequency

6. UART

(1) Overview

- The UART is a general-purpose serial communications interface for performing synchronous or asynchronous (start-stop synchronization) communications with external devices.
- The interface provides both a bi-directional communication function (normal mode) and a master-slave communication function (multi-processor mode) .
- The UART can generate interrupt requests at receive complete, receive error detected, and transmit complete timings. Also the UART supports EI^{2}OS.

- **UART functions**

The UART is a general-purpose serial communications interface for sending serial data to and from other CPUs and peripheral devices.

	Function
Data buffer	Full-duplex double-buffered
Transmission modes	• Clock synchronous (no start and stop bits) • Clock asynchronous (start-stop synchronization)
Baud rate	• Max. 2 MHz (for a 16 MHz machine clock) • Baud rate generated by dedicated baud rate generator • Baud rate generated by external clock (clock input from SCK0 and SCK1 pins) • Baud rate generated by internal clock (clock supplied from 16-bit reload timer) • Eight different baud rate settings are available.
Number of data bits	• 7 bits (asynchronous normal mode only) • 8 bits
Signal format	Non return to zero (NRZ) format
Receive error detection	• Framing errors • Overrun errors • Parity errors (not available in multi-processor mode)
Interrupt requests	• Receive interrupt (Receive complete or receive error detected) • Transmit interrupt (Transmission complete) • Both transmit and receive support the extended intelligent I/O service (EI^{2}OS) .
Master/slave communication function (multi-processor mode)	Used for 1 (master) to n (slave) communications. (Can only be used as master)

Note : The UART does not add the start and stop bits in clock synchronous mode. In this case, only data is transmitted.

- **UART operation modes**

Operation Mode		No. of Data Bits		Synchronization	No. of Stop Bits
		No Parity	With Parity		
0	Normal mode	7 or 8 bits		Asynchronous	1 or 2 bits[*2]
1	Multi-processor mode	8 + 1[*1]	—	Asynchronous	
2	Clock synchronous mode	8	—	Synchronous	None

— : Not available

*1 : The “+1” represents the address/data (A/D) bit used for communication control.

*2 : Only 1 stop bit supported for receiving.

- **UART interrupts and EI²OS**

Interrupt	Interrupt No.	Interrupt Control Register		Vector Table Address			EI²OS
		Register Name	Address	Lower	Upper	Bank	
UART1 receive interrupt	#37 (25$_H$)	ICR13	0000BD$_H$	FFFF68$_H$	FFFF69$_H$	FFFF6A$_H$	◎
UART1 send interrupt	#38 (26$_H$)	ICR13	0000BD$_H$	FFFF64$_H$	FFFF65$_H$	FFFF66$_H$	△
UART0 receive interrupt	#39 (27$_H$)	ICR14	0000BE$_H$	FFFF60$_H$	FFFF61$_H$	FFFF62$_H$	◎
UART0 send interrupt	#40 (28$_H$)	ICR14	0000BE$_H$	FFFF5C$_H$	FFFF5D$_H$	FFFF5E$_H$	△

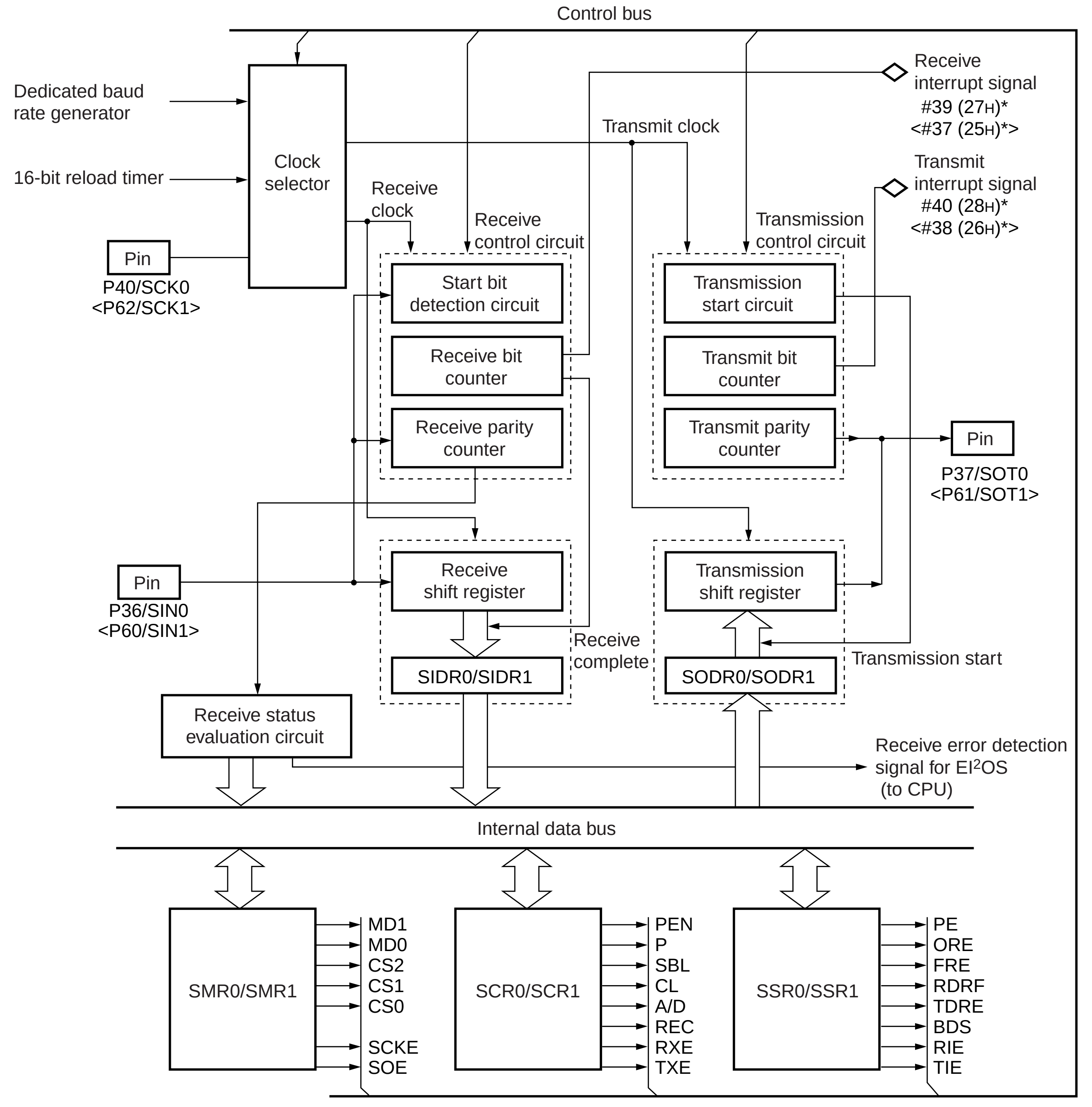
◎ : The UART has a function to halt EI²OS if a receive error is detected.
△ : Available when the interrupt shared with ICR13 or ICR14 is not used.

(2) UART structure

The UART consists of the following 11 blocks:

- Clock selector
- Receive control circuit
- Transmission control circuit
- Receive status evaluation circuit
- Receive shift register
- Transmission shift register
- Mode registers (SMR0, SMR1)
- Control registers (SCR0, SCR1)
- Status registers (SSR0, SSR1)
- Input data registers (SIDR0, SIDR1)
- Output data registers (SODR0, SODR1)

- **Block diagram**


Control bus
Dedicated baud rate generator
16-bit reload timer
Clock selector
Pin
P40/SCK0
<P62/SCK1>
Receive clock
Receive control circuit
Transmit clock
Transmission control circuit
Receive interrupt signal
#39 (27H)*
<#37 (25H)*>
Transmit interrupt signal
#40 (28H)*
<#38 (26H)*>
Start bit detection circuit
Receive bit counter
Receive parity counter
Transmission start circuit
Transmit bit counter
Transmit parity counter
Pin
P37/SOT0
<P61/SOT1>
Pin
P36/SIN0
<P60/SIN1>
Receive shift register
Transmission shift register
Receive complete
Transmission start
SIDR0/SIDR1
SODR0/SODR1
Receive status evaluation circuit
Receive error detection signal for EI^{2}OS (to CPU)
Internal data bus
SMR0/SMR1
MD1
MD0
CS2
CS1
CS0
SCKE
SOE
SCR0/SCR1
PEN
P
SBL
CL
A/D
REC
RXE
TXE
SSR0/SSR1
PE
ORE
FRE
RDRF
TDRE
BDS
RIE
TIE

* : Interrupt number

- **Clock selector**

Selects the send/receive clock from either the dedicated baud rate generator, external input clock (clock input to SCK0 or SCK1 pin) , or internal clock (clock supplied by 16-bit reload timer) .

- **Receive control circuit**

The receive control circuit consists of a receive bit counter, start bit detection circuit, and receive parity counter. The receive bit counter counts the received data bits and outputs a receive interrupt request when the required number of data bits have been received. The start bit detection circuit detects the start bit on the serial input signal. On detecting a start bit, the receive data is shifted to the input data register (SIDR0 or SIDR1) in accordance with the specified transfer speed. The receive parity counter calculates the parity of the received data if parity is selected.

- **Transmission control circuit**

The transmission control circuit consists of a transmission bit counter, transmission start circuit, and transmission parity counter. The transmission bit counter counts the transmitted data bits and outputs a transmit interrupt request when the required number of data bits have been sent. The transmission start circuit starts transmission when data is written to the output data register (SODR0 or SODR1) . The transmission parity counter generates the parity bit for the transmitted data when parity is selected.

- **Receive shift register**

The receive shift register captures the data input from the SIN0 or SIN1 pin by shifting one bit at a time then transfers the received data to the input data register (SIDR0 or SIDR1) when reception completes.

- **Transmission shift register**

The transmission data is transferred from the output data register (SODR0 or SODR1) to the transmission shift register and output from the SOT0 or SOT1 pin by shifting one bit at a time.

- **Mode register (SMR0, SMR1)**

Set the operation mode, baud rate clock and serial clock input/output control, and enables output for the serial data pin.

- **Control register (SCR0, SCR1)**

Specifies whether to use parity, the type of parity, number of stop bits and data bits and the frame data format for operation mode 1, to clear the receive error flag bit, and to enable or disable send and receive operation.

- **Status register (SSR0, SSR1)**

Stores the send/receive and error status information, set the serial data transfer direction, and enables or disables the send and receive interrupt requests.

- **Input data register (SIDR0, SIDR1)**

Stores the received data.

- **Output data register (SODR0, SODR1)**

Set the transmission data. The data set in the output data register is converted to serial format and output.

7. DTP/External Interrupt Circuit

(1) Overview of the DTP/external interrupt circuit

The DTP (Data Transfer Peripheral) /external interrupt circuit detects interrupt requests input to the external interrupt input pins (INT7 to INT0) and outputs interrupt requests.

- **DTP/external interrupt circuit functions**

The DTP/external interrupt function detects edge or level signals input to the external interrupt input pins (INT7 to INT0) and outputs interrupt requests.

The interrupt request is received by the CPU and, if the extended intelligent I/O service (EI^{2}OS) is enabled, EI^{2}OS performs automatic data transfer (DTP function) then passes control to the interrupt handler routine on completion. If EI^{2}OS is disabled, control passes directly to the interrupt handler routine without performing automatic data transfer (DTP function) .

- **Overview of the DTP/external interrupt circuit**

	External Interrupt	DTP Function
Input pins	8 channels (P10/INT0 to P16/INT6, P63/INT7)	
Interrupt conditions	The level or edge to detect can be set independently for each pin in the detection level setup register (ELVR) .	
	“L” level, “H” level, rising edge, or falling edge input	
Interrupt number	#25 (19_H) to #28 ($1C_H$)	
Interrupt control	Interrupts can be enabled or disabled in the DTP/external interrupt enable register (ENIR) .	
Interrupt flag	The DTP/external interrupt request register (ENRR) stores interrupt requests.	
Processing selection	Set EI^{2}OS to disabled (ICR : ISE = 0)	Set EI^{2}OS to enabled (ICR : ISE = 1)
Operation	Jumps to interrupt handler routine	Jumps to interrupt handler routine after automatic data transfer by EI^{2}OS completes.

ICR : Interrupt control register

- **DTP/external interrupt circuit interrupts and EI^{2}OS**

Channel	Interrupt No.	Interrupt Control Register		Vector Table Address			EI^{2}OS
		Register Name	Address	Lower	Upper	Bank	
INT0/INT1	#25 (19_H)	ICR07	$0000B7_H$	$FFFF98_H$	$FFFF99_H$	$FFFF9A_H$	△
INT2/INT3	#26 ($1A_H$)			$FFFF94_H$	$FFFF95_H$	$FFFF96_H$	
INT4/INT5	#27 ($1B_H$)	ICR08	$0000B8_H$	$FFFF90_H$	$FFFF91_H$	$FFFF92_H$	
INT6/INT7	#28 ($1C_H$)			$FFFF8C_H$	$FFFF8D_H$	$FFFF8E_H$	

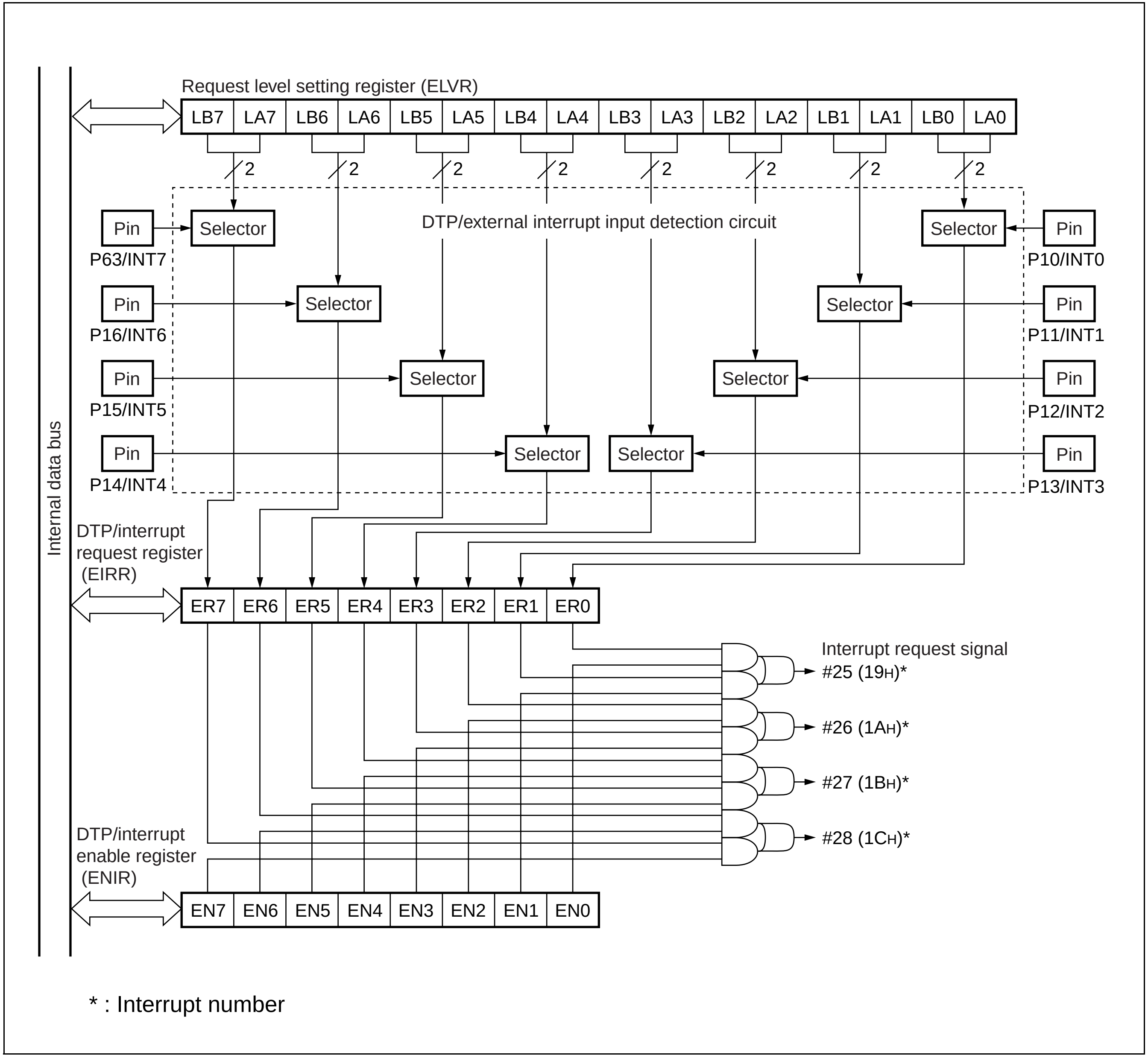
△ : Available when the interrupt shared with ICR07 or ICR08 is not used.

(2) Structure of the DTP/external interrupt circuit

The DTP/external interrupt circuit consists of the following four blocks :

- DTP/interrupt detection circuit
- DTP/interrupt request register (EIRR)
- DTP/interrupt enable register (ENIR)
- Request level setting register (ELVR)

- **Block diagram**


Request level setting register (ELVR)
LB7 LA7 LB6 LA6 LB5 LA5 LB4 LA4 LB3 LA3 LB2 LA2 LB1 LA1 LB0 LA0
2
DTP/external interrupt input detection circuit
Pin
Selector
P63/INT7
P16/INT6
P15/INT5
P14/INT4
P10/INT0
P11/INT1
P12/INT2
P13/INT3
Internal data bus
DTP/interrupt request register (EIRR)
ER7 ER6 ER5 ER4 ER3 ER2 ER1 ER0
Interrupt request signal
#25 (19H)*
#26 (1AH)*
#27 (1BH)*
#28 (1CH)*
DTP/interrupt enable register (ENIR)
EN7 EN6 EN5 EN4 EN3 EN2 EN1 EN0

* : Interrupt number

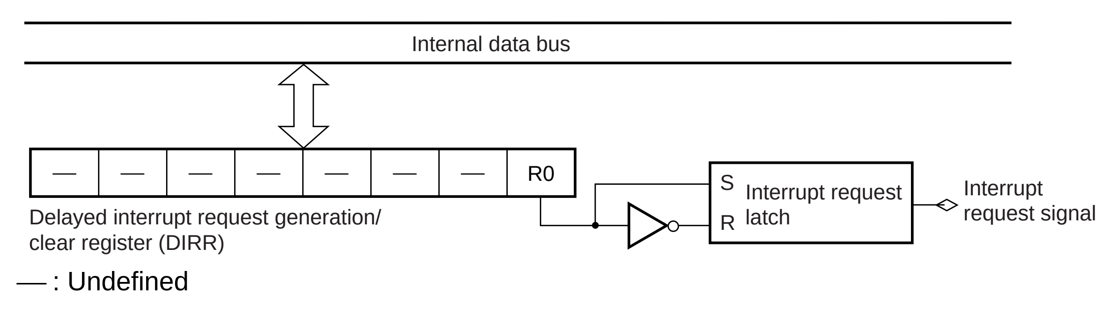
8. Delayed Interrupt Generation Module

- The delayed interrupt generation module is used to generate the task switching interrupt. Generation of this hardware interrupt can be specified by software.

- **Delayed interrupt generation module functions**

	Function and Control
Interrupt trigger	• Writing “1” to bit R0 of the delayed interrupt request generation/clear register (DIRR : R0 = 1) generates an interrupt request. • Writing “0” to bit R0 of the delayed interrupt request generation/clear register (DIRR : R0 = 1) clears the interrupt request.
Interrupt control	• No enable/disable register is provided for this interrupt.
Interrupt flag	• Set in bit R0 of the delayed interrupt request generation/clear register (DIRR : R0) .
EI²OS support	• Not supported by the extended intelligent I/O service (EI²OS) .

- **Block diagram**


Internal data bus
—
—
—
—
—
—
—
R0
Delayed interrupt request generation/ clear register (DIRR)
S
R
Interrupt request latch
Interrupt request signal
— : Undefined

9. 8/10-Bit A/D Converter

- **Overview of the 8/10-bit A/D converter**
- The 8/10-bit A/D converter uses RC successive approximation to convert analog input voltages to an 8-bit or 10-bit digital value.
- The input signals can be selected from the eight analog input pin channels.

- **8/10-bit A/D converter functions**

A/D conversion time	The minimum conversion time is 6.13 µs (for a 16 MHz machine clock, including sampling time) . The minimum sampling time is 2.0 µs (for a 16 MHz machine clock)
Conversion method	RC successive approximation with sample & hold circuit
Resolution	8-bit or 10-bit, selectable
Analog input pins	Eight analog input pin channels are available. The input pin can be selected by the program.
Interrupts	An interrupt request can be generated and EI²OS invoked when A/D conversion completes. The conversion data protection function operates when A/D conversion is performed with the interrupt enabled.
A/D conversion start trigger	The conversion start trigger can be set from the following options : software, output of 16-bit reload timer 1 (rising edge) , or zero detection edge from 16-bit freerun timer.
EI²OS support	Supported by the extended intelligent I/O service (EI²OS) .

- **8/10-bit A/D converter conversion modes**

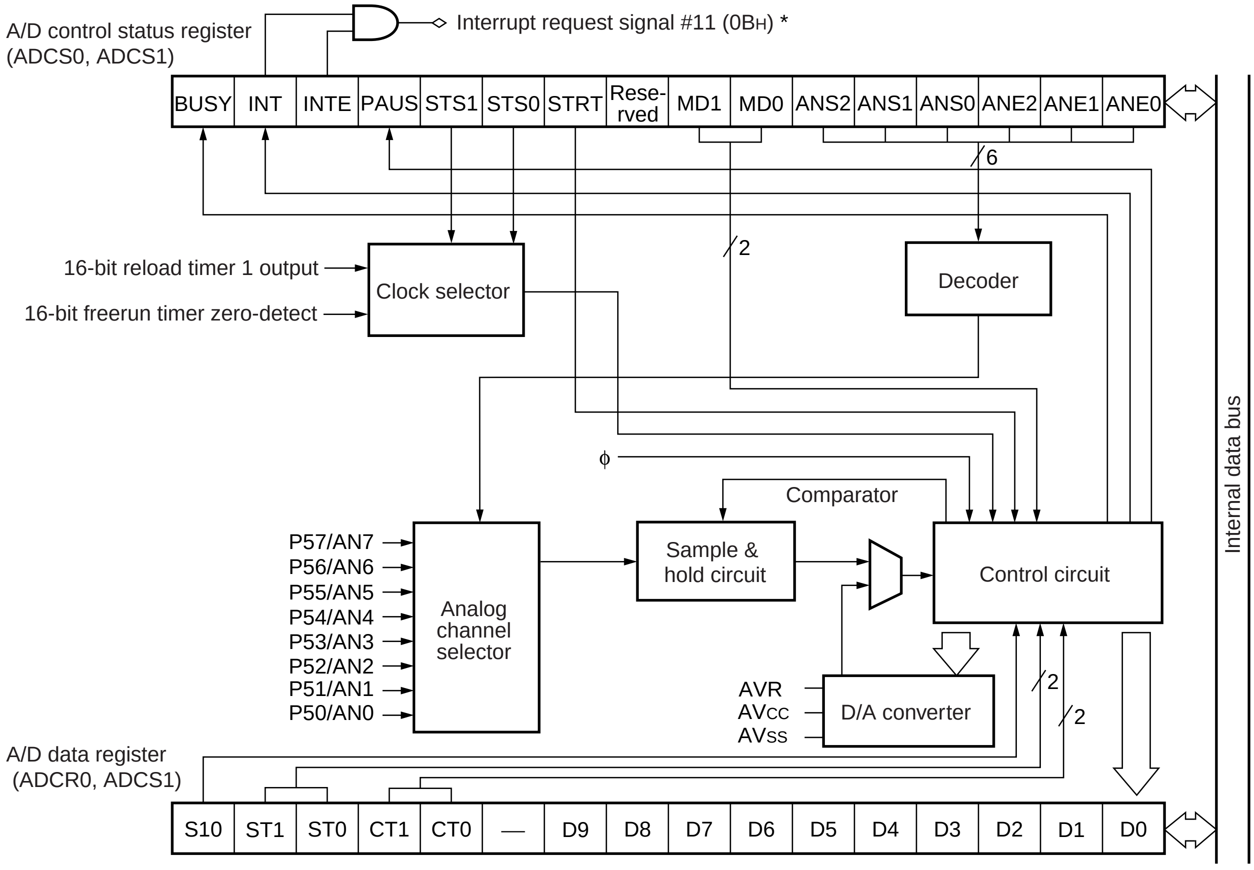
Conversion Mode	Single Conversion Mode Operation	Scan Conversion Mode Operation
Single-shot conversion mode 1 Single-shot conversion mode 2	Performs one conversion for the specified channel (1 channel) then halts.	Sequentially performs one conversion for multiple channels (up to 8 channels can be set) , then halts.
Continuous conversion mode	Performs repeated conversions for the specified channel (1 channel) .	Performs repeated conversions for the specified channels (up to 8 channels can be set) .
Incremental conversion mode	Performs one conversion for the specified channel (1 channel) then halts and waits for the next activation.	Sequentially performs one conversion for multiple channels (up to 8 channels can be set) , then halts and waits for the next activation.

- **8/10-bit A/D converter interrupts and EI²OS**

Interrupt No.	Interrupt Control Register		Vector Table Address			EI²OS
	Register Name	Address	Lower	Upper	Bank	
#11 (0B$_H$)	ICR00	0000B0$_H$	FFFFD0$_H$	FFFFD1$_H$	FFFFD2$_H$	○

○ : Available

- **Block diagram**


A/D control status register
(ADCS0, ADCS1)
Interrupt request signal #11 (0BH) *
BUSY
INT
INTE
PAUS
STS1
STS0
STRT
Rese-rved
MD1
MD0
ANS2
ANS1
ANS0
ANE2
ANE1
ANE0
6
2
16-bit reload timer 1 output
16-bit freerun timer zero-detect
Clock selector
Decoder
Internal data bus
ϕ
Comparator
P57/AN7
P56/AN6
P55/AN5
P54/AN4
P53/AN3
P52/AN2
P51/AN1
P50/AN0
Analog channel selector
Sample & hold circuit
Control circuit
AVR
AVCC
AVSS
D/A converter
2
2
A/D data register
(ADCR0, ADCS1)
S10
ST1
ST0
CT1
CT0
—
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0

ϕ : Machine clock
* : Interrupt number

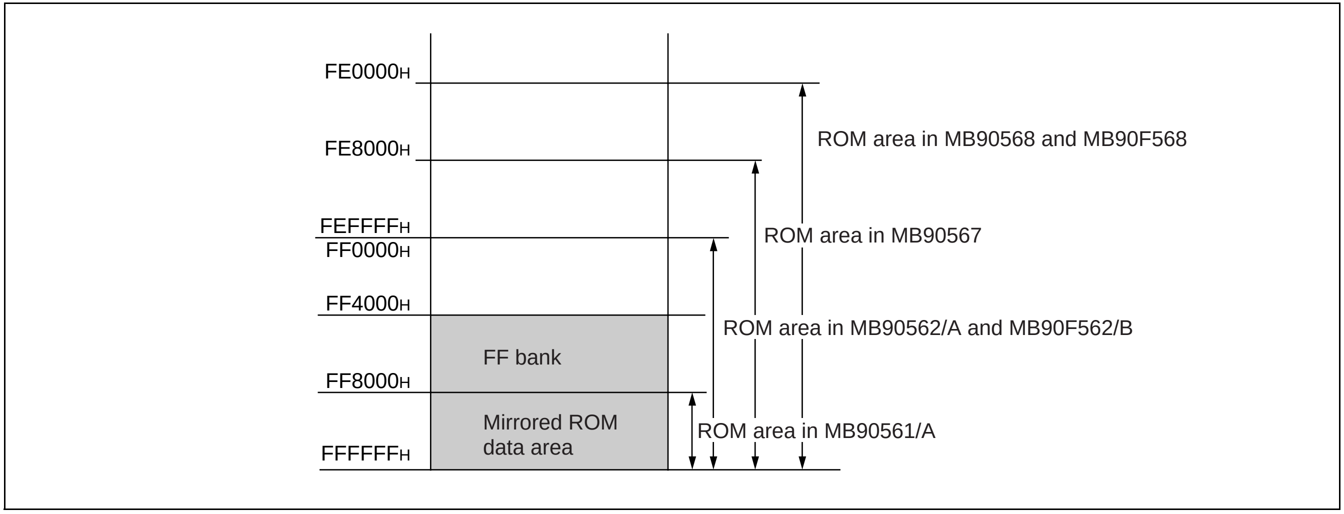
10. ROM Mirror Function Selection Module

- The ROM mirror function selection module enables ROM data in FF bank to be read by accessing 00 bank.

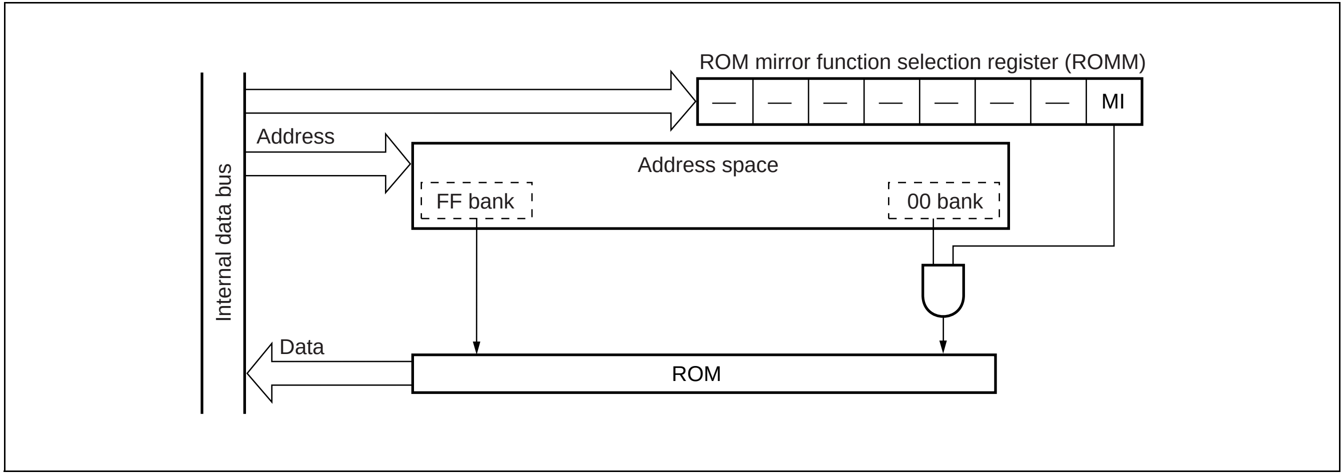
- **ROM mirror function selection module functions**

	Function
Mirror setting address	• Data in FFFFFF$_H$ to FF4000$_H$ in FF bank can be read from 00FFFF$_H$ to 004000$_H$ in 00 bank.
Interrupts	• None
EI²OS support	• Not supported by the extended intelligent I/O service (EI²OS) .

- **Relationship between addresses in the ROM mirror function**


FE0000H
FE8000H
FEFFFFH
FF0000H
FF4000H
FF8000H
FFFFFFH
FF bank
Mirrored ROM data area
ROM area in MB90568 and MB90F568
ROM area in MB90567
ROM area in MB90562/A and MB90F562/B
ROM area in MB90561/A

- **Block diagram**


ROM mirror function selection register (ROMM)
—
—
—
—
—
—
—
MI
Address
Address space
FF bank
00 bank
Internal data bus
Data
ROM

11. Low Power Consumption (Standby) Modes

- The power consumption of F²MC-16LX devices can be reduced by various settings that control the operating clock selection.

- **Functions of each CPU operation mode**

CPU Operation Clock	Operation Mode	Function
PLL clock	Normal Run	The CPU and peripheral functions operate using the oscillation clock (HCLK) multiplied by the PLL circuit.
	Sleep	The peripheral functions only operate using the oscillation clock (HCLK) multiplied by the PLL circuit.
	Pseudo-clock	The timebase timer only operates using the oscillation clock (HCLK) multiplied by the PLL circuit.
	Stop	The oscillation clock is stopped and the CPU and peripherals halt operation.
Main clock	Normal Run	The CPU and peripheral functions operate using the oscillation clock (HCLK) divided into 2.
	Sleep	The peripheral functions only operate using the oscillation clock (HCLK) divided into 2.
	Stop	The oscillation clock is stopped and the CPU and peripherals halt operation.
CPU intermittent operation	Normal Run	The oscillation clock (HCLK) divided into 2 operates intermittently for fixed time intervals.

12. 512 Kbit Flash Memory

- This section describes the flash memory on the MB90F562/B and does not apply to evaluation and mask ROM versions.
- The flash memory is located in bank FF in the CPU memory map.

- **Flash memory functions**

	Function
Memory size	• 512 Kbit (64 KBytes)
Memory configuration	• 64 KWords × 8 bits or 32 KWords × 16 bits
Sector configuration	• 16 KBytes + 8 KBytes + 8 KBytes + 32 KBytes
Sector protect function	• Selectable for each sector
Programming algorithm	• Automatic programming algorithm (Embedded Algorithm* : Equivalent to MBM29F400TA)
Operation commands	• Compatible with JEDEC standard commands • Includes an erase pause and restart function • Write/erase completion detection by data polling or toggle bit • Erasing by sector available (sectors can be combined in any combination)
No. of write/erase cycles	• Min. 10,000 guaranteed
Memory write/erase method	• Can be written and erased using a parallel writer (Ando Denki AF9704, AF9705, AF9706, AF9708, and AF9709) • Can be written and erased using a dedicated serial writer (Yokogawa Digital Computer Corporation AF200, AF210, AF120, and AF110) • Can be written and erased by the program
Interrupts	• Write and erase completion interrupts
EI^{2}OS support	• Not supported by the extended intelligent I/O service (EI^{2}OS) .

* : Embedded Algorithm is a trademark of Advanced Micro Devices.

- **Sector configuration of flash memory**

Flash memory	CPU address	Writer address*
SA1 (32 Kbyte)	FF0000H FF7FFFH	70000H 77FFFH
SA2 (8 Kbyte)	FF8000H FF9FFFH	78000H 79FFFH
SA3 (8 Kbyte)	FFA000H FFBFFFH	7A000H 7BFFFH
SA4 (16 Kbyte)	FFC000H FEFFFFH	7C000H 7FFFFH

* : The writer address is the address to be used instead of the CPU address when writing data from a parallel flash memory writer. Use the writer address when programming or erasing with a general-purpose parallel writer.

13. 1 Mbit Flash Memory

- This section describes the flash memory on the MB90F568 and does not apply to evaluation and mask ROM versions.
- The flash memory is located in banks FE to FF in the CPU memory map.

- **Flash memory functions**

	Function
Memory size	• 1 Mbit (128 KBytes)
Memory configuration	• 128 KWords × 8 bits or 64 KWords × 16 bits
Sector configuration	• 16 KBytes + 8 KBytes + 8 KBytes + 32 KBytes + 64 KBytes
Sector protect function	• Selectable for each sector
Programming algorithm	• Automatic programming algorithm (Embedded Algorithm* : Equivalent to MBM29F400TA)
Operation commands	• Compatible with JEDEC standard commands • Includes an erase pause and restart function • Write/erase completion detection by data polling or toggle bit • Erasing by sector available (sectors can be combined in any combination)
No. of write/erase cycles	• Min. 10,000 guaranteed
Memory write/erase method	• Can be written and erased using a parallel writer (Ando Denki AF9704, AF9705, AF9706, AF9708, and AF9709) • Can be written and erased using a dedicated serial writer (Yokogawa Digital Computer Corporation AF200, AF210, AF120, and AF110) • Can be written and erased by the program
Interrupts	• Write and erase completion interrupts
EI^{2}OS support	• Not supported by the extended intelligent I/O service (EI^{2}OS) .

* : Embedded Algorithm is a trademark of Advanced Micro Devices.

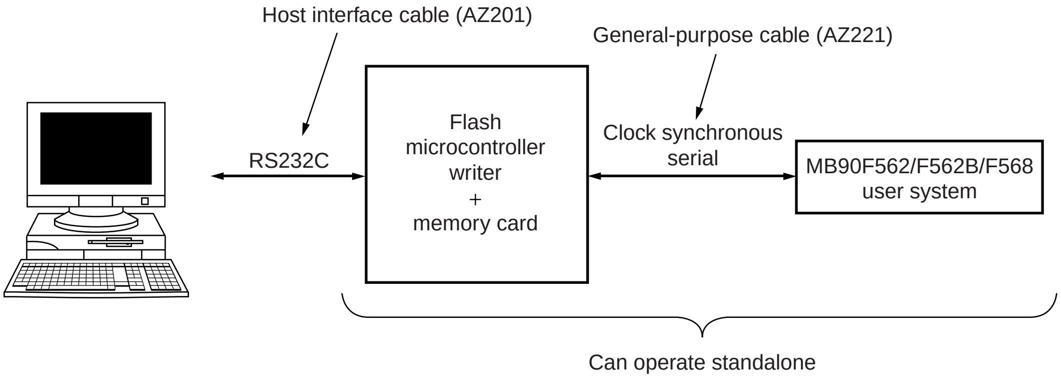
- **Sector configuration of flash memory**

Flash memory	CPU address	Writer address*
SA0 (64 Kbyte)	FE0000H FEFFFH	60000H 6FFFFH
SA1 (32 Kbyte)	FF0000H FF7FFFH	70000H 77FFFH
SA2 (8 Kbyte)	FF8000H FF9FFFH	78000H 79FFFH
SA3 (8 Kbyte)	FFA000H FFBFFFH	7A000H 7BFFFH
SA4 (16 Kbyte)	FFC000H FEFFFFH	7C000H 7FFFFH

* : The writer address is the address to be used instead of the CPU address when writing data from a parallel flash memory writer. Use the writer address when programming or erasing with a general-purpose parallel writer.

- **Standard configuration for Fujitsu standard serial on-board programming**

Fujitsu standard serial on-board programming uses a flash microcontroller writer from Yokogawa Digital Computer Corporation (AF220, AF210, AF120, or AF210) .

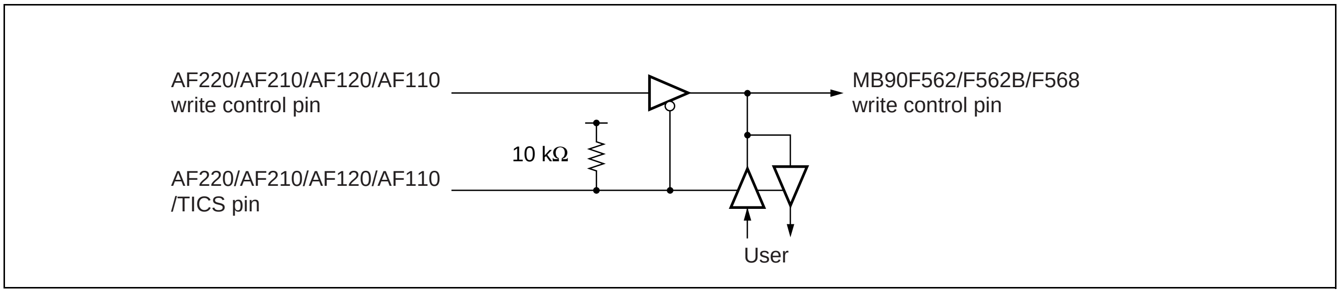

Host interface cable (AZ201)
General-purpose cable (AZ221)
RS232C
Flash microcontroller writer + memory card
Clock synchronous serial
MB90F562/F562B/F568 user system
Can operate standalone

Note : Contact Yokogawa Digital Computer Corporation for details of the functions and operation of the flash microcontroller writer (AF220, AF210, AF120, or AF110) , standard connection cable (AZ221) , and connectors.

- **Pins used for Fujitsu standard serial on-board programming**

Symbol	Pin name	Function
MD2, MD1, MD0	Mode input pins	Setting MD2 = 1, MD1 = 1, and MD0 = 0 selects serial programming mode.
X0, X1	Oscillation input pin	As flash memory serial programming mode uses the PLL clock with the multiplier set to 1 as the internal CPU operation clock, the internal operation clock frequency is the same as the oscillation clock frequency. Accordingly, the frequency that can be input to the high speed oscillation input pin when performing serial programming is between 1 MHz and 16 MHz.
P00, P01	Write program activation pins	Input P00 = “L” level and P01 = “H” level.
$\overline{\text{RST}}$	Reset input pin	—
SIN1	Serial data input pin	Uses UART0 and UART1 in clock synchronous mode. In programming mode, the pins used by UART0 in clock synchronous mode are SIN1, SOT1, and SCK0.
SOT1	Serial data output pin	
SCK0	Serial clock input pin	
C	Capacitor/power supply input pin	Capacitor pin for power supply stabilization. Connect an external ceramic capacitor of approx. 0.1 µF.
V_{CC}	Power supply input pins	If the user system provides the programming voltage (MB90F562 : 5 V ± 10%, MB90F568 : 3 V ± 10%) , these do not need to be connected to the flash microcontroller writer.
V_{SS}	GND pin	Connect to common GND with the flash microcontroller writer.

The control circuit shown in the figure is required when the P00, P01, SIN1, SOT1, and SCK0 pins are used on the user system. Use the /TICS signal from the flash microcontroller writer to disconnect the user circuit during serial on-board programming.



Control circuit

Use the formula below to calculate the serial clock frequency able to be input to the MB90F562/F562B/F568. Set up the flash microcontroller writer to use a serial clock input frequency that is permitted for the oscillation clock frequency you are using.

Permitted input serial clock frequency = 0.125 × oscillation clock frequency

- **Maximum serial clock frequency**

Oscillation Clock Frequency	Maximum Serial Clock Frequency that can be Input to Microcontroller	Maximum Serial Clock Frequency that can be Set on the AF220/AF210/AF120/AF110	Maximum Serial Clock Frequency that can be Set on the AF200
4 MHz	500 kHz	500 kHz	500 kHz
8 MHz	1 MHz	850 kHz	500 kHz
16 MHz	2 MHz	1.25 MHz	500 kHz

- **System configuration of flash microcontroller writer (AF220/AF210/AF120/AF110) (Supplier : Yokogawa Digital Computer Corporation)**

Model		Function	
Unit	AF200/AC4P	Internal Ethernet interface model	/100 V to 220 V power adapter
	AF210/AC4P	Standard model	/100 V to 220 V power adapter
	AF120/AC4P	Single key, Internal Ethernet interface model	/100 V to 220 V power adapter
	AF110/AC4P	Single key model	/100 V to 220 V power adapter
AZ221		Special RS232C cable for connecting writer to PC/AT	
AZ210		Standard target probe (a) Length : 1 m	
FF201		Control module for Fujitsu F^{2}MC-16LX flash microcontrollers	
AZ290		Remote controller	
AZ264		Power supply regulator (MB90F568 : Required to supply 3 V versions from the flash microcontroller writer.)	
/P2		2 MB PC card (option) Supports FLASH memory sizes up to 128 KB	
/P4		4 MB PC card (option) Supports FLASH memory sizes up to 512 KB	

Contact : Yokogawa Digital Computer Corporation Tel : 042-333-6224

Note : The AF200 flash microcontroller writer is an obsolete model but can still be used with the FF201 control module.

■ ELECTRICAL CHARACTERISTICS (MB90560 SERIES)

1. Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} \geq AV_{CC}$ *1
	AVR	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVR \geq 0$ V *1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
"L" level maximum output current	I_{OL1}	—	15	mA	*3, *4
	I_{OL2}	—	20	mA	*3, *5
"L" level average output current	I_{OLAV1}	—	4	mA	Average value (operating current × operating ratio) *4
	I_{OLAV2}	—	12	mA	Average value (operating current × operating ratio) *5
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Average value (operating current × operating ratio)
"H" level maximum output current	I_{OH}	—	–15	mA	*3
"H" level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating ratio)
"H" level total maximum output current	ΣI_{OH}	—	–100	mA	
"H" level total average output current	ΣI_{OHAV}	—	–50	mA	Average value (operating current × operating ratio)
Power consumption	Pd	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : AV_{CC} and AVR must not exceed V_{CC}. Also, AVR must not exceed AV_{CC}.

*2 : V_I and V_O must not exceed $V_{CC} + 0.3$ V.

*3 : The maximum output current is the peak value for a single pin.

*4 : Pins other than P30/RTO0 to P35/RTO5

*5 : P30/RTO0 to P35/RTO5 pins

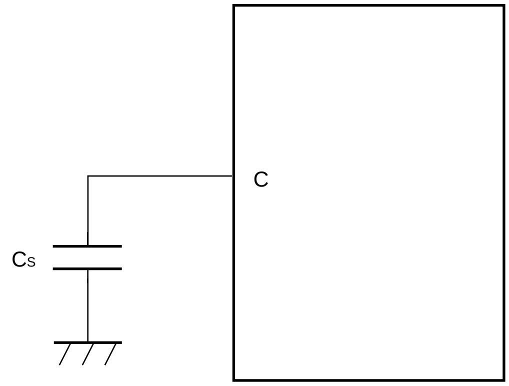
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	5.5	V	Normal operation (MB90562, 562A, 561, 561A, and V560)
		4.5	5.5	V	Normal operation (MB90F562 and F562B)
	V_{CC}	3.0	5.5	V	Maintaining state in stop mode
Input "H" voltage	V_{IH}	0.7 V_{CC}	$V_{CC} + 0.3$	V	CMOS input pin
	V_{IHS}	0.8 V_{CC}	$V_{CC} + 0.3$	V	CMOS hysteresis input pin
	V_{IHM}	$V_{CC} - 0.3$	$V_{CC} + 0.3$	V	MD input pin
Input "L" voltage	V_{IL}	$V_{SS} - 0.3$	0.3 V_{CC}	V	CMOS input pin
	V_{ILS}	$V_{SS} - 0.3$	0.2 V_{CC}	V	CMOS hysteresis input pin
	V_{ILM}	$V_{SS} - 0.3$	$V_{SS} + 0.3$	V	MD input pin
Smoothing capacitor	C_S	0.1	1.0	µF	Use a ceramic capacitor or other capacitor with equivalent frequency characteristics. The capacitance of the smoothing capacitor connected to the V_{CC} pin must be greater than C_S.
Operating temperature	T_A	–40	+85	°C	

- C pin diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Sym-bol	Pin Name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Output “H” voltage	V_{OH}	All output pins	V_{CC} = 4.5 V I_{OH} = –2.0 mA	V_{CC} – 0.5	—	—	V	
Output “L” voltage	V_{OL1}	Pins other than P30/RTO0 to P35/RTO5	V_{CC} = 4.5 V I_{OL1} = 2.0 mA	—	—	0.4	V	
	V_{OL2}	P30/RTO0 to P35/RTO5	V_{CC} = 4.5 V I_{OL2} = 12.0 mA	—	—	0.8	V	
Input leak current	I_{IL}	All output pins	V_{CC} = 5.5 V $V_{SS} < V_I < V_{CC}$	–5	—	5	µA	
Power supply current*	I_{CC}	V_{CC}	For V_{CC} = 5 V, internal frequency = 16 MHz, normal operation	—	50	80	mA	MB90562/A, MB90561/A
				—	40	50	mA	MB90F562/B
			For V_{CC} = 5 V, internal frequency = 16 MHz, A/D operation in progress	—	55	85	mA	MB90562/A, MB90561/A
				—	45	55	mA	MB90F562/B
			Flash write or erase	—	45	60	mA	MB90F562/B
	I_{CCS}		For V_{CC} = 5 V, internal frequency = 16 MHz, sleep mode	—	15	20	mA	MB90562/A, MB90561/A MB90F562/B*
	I_{CCH}		Stop mode, TA = 25 °C	—	5	20	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, C, V_{CC}, and V_{SS}	—	—	10	80	pF	
Pull-up resistor	R_{UP}	P00 to P07 P10 to P17 $\overline{RST}$, MD0, MD1	—	15	30	100	kΩ	
Pull-down resistor	R_{DOWN}	MD2	—	15	30	100	kΩ	

* : Value when low power mode bits (LPM0, 1) is set to “01” with an internal operating frequency of 4 MHz.

Note : Current values are provisional and are subject to change without notice to allow for improvements to the characteristics. The power supply current is measured with an external clock.

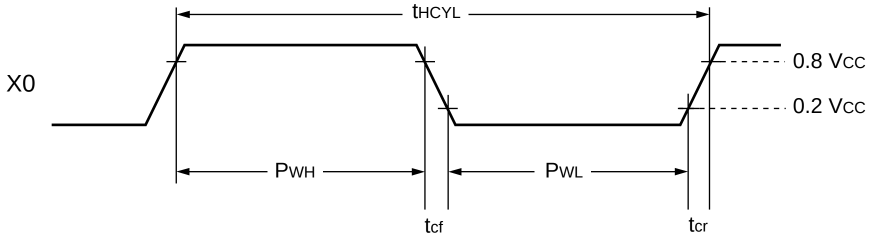
4. AC Characteristics

(1) Clock Timings

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

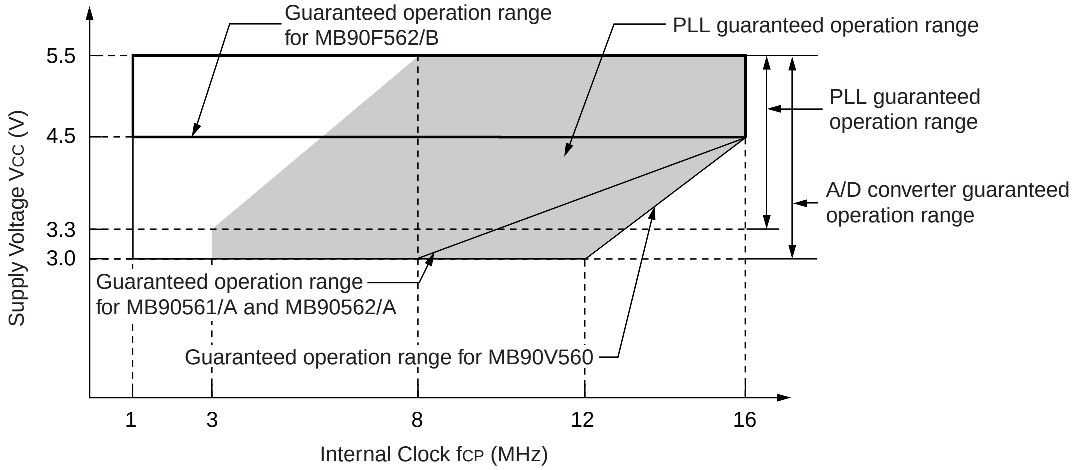
Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	f_C	X0, X1	—	3	—	16	MHz	With a PLL circuit
				1	—	16		Without a PLL circuit
Clock cycle time	t_{HCYL}	X0, X1		62.5	—	333	ns	With a PLL circuit
				62.5	—	1000		Without a PLL circuit
Input clock pulse width	P_{WH} P_{WL}	X0		10	—	—	ns	Recommended duty ratio = 30% to 70%
Input clock rise/fall time	t_{cr} t_{cf}	X0		—	—	5	ns	When using an external clock
Internal operating clock frequency	f_{CP}	—		1.5	—	16	MHz	When using a main clock
Internal operating clock cycle time	t_{CP}	—		62.5	—	333	ns	When using a main clock

- **X0 and X1 clock timing**

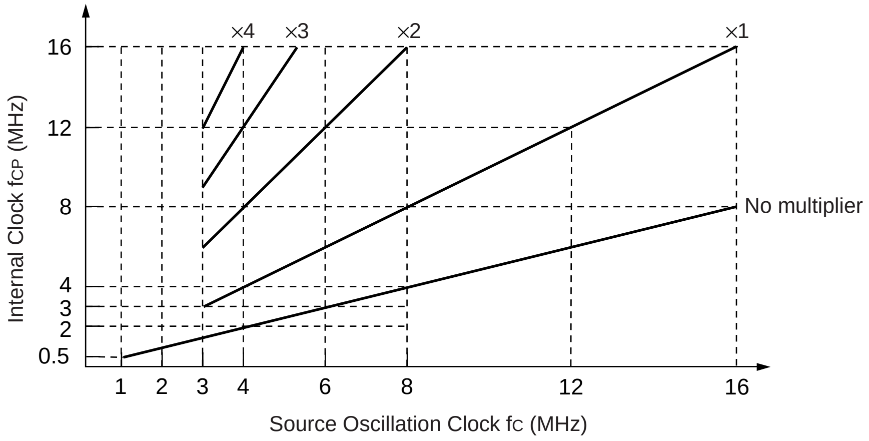


- **PLL guaranteed operation range**

Relationship between internal operating clock frequency and power supply voltage



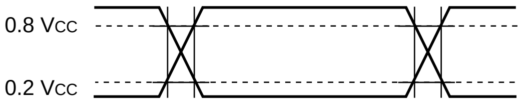
Relationship between oscillation frequency and internal operating clock frequency



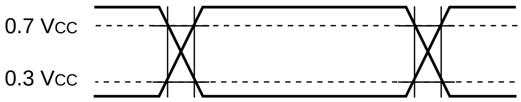
The AC ratings are specified for the following measurement reference voltages.

- **Input signal waveform**

Hysteresis input pin

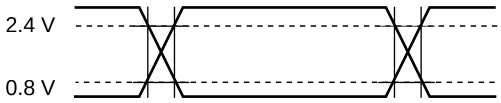


Pins other than hysteresis input or MD input pins



- **Output signal waveform**

Output pin



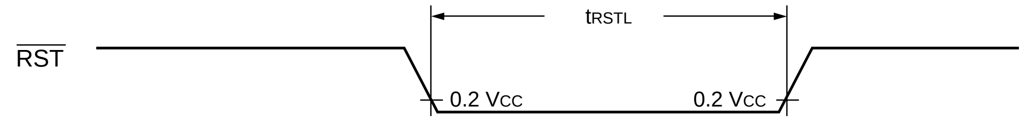
(2)Reset

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

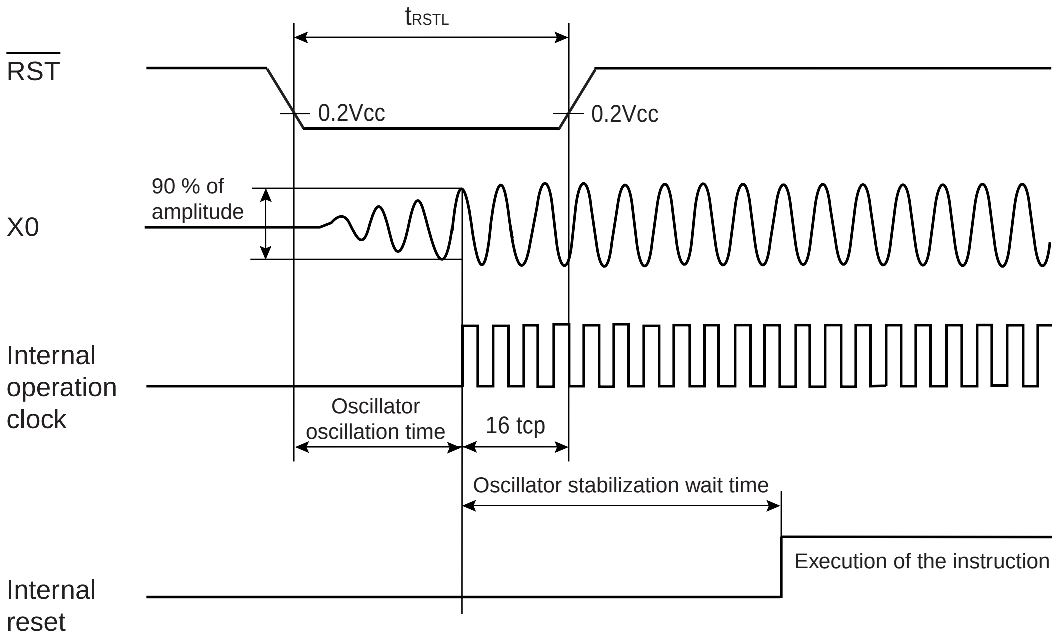
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	**Max.**		
Reset input time	t_{RSTH}	$\overline{RST}$	—	16 t_{CP}	—	ns	In normal operation
				Oscillator oscillation time* + 16 t_{CP}	—	ms	In stop mode

*: Oscillator oscillation time is the time to reach 90% amplitude. For a crystal oscillator, this is a few to several dozen ms; for a FAR/ceramic oscillator, this is several hundred µs to a few ms, and for an external clock this is 0 ms.

- In normal operation


t_{RSTL}
$\overline{RST}$
0.2 V_{CC}
0.2 V_{CC}

- In stop mode


t_{RSTL}
$\overline{RST}$
0.2Vcc
0.2Vcc
90 % of amplitude
X0
Internal operation clock
Oscillator oscillation time
16 tcp
Oscillator stabilization wait time
Execution of the instruction
Internal reset

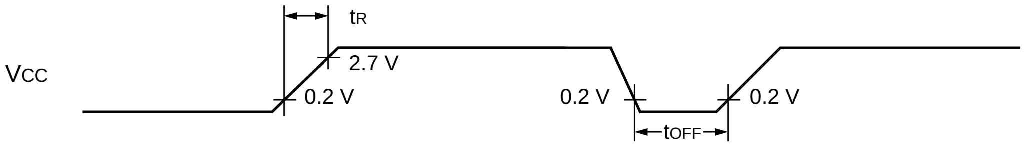
(3) Power-On Reset

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

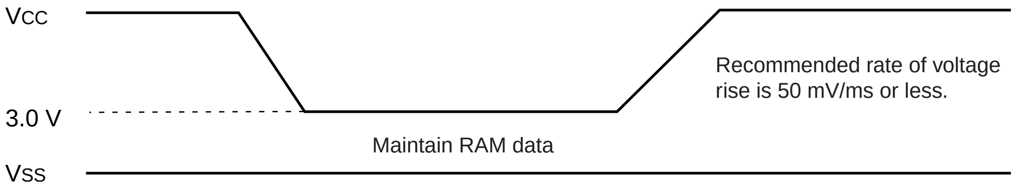
Parameter	Symbol	Pin Name	Condi-tion	Value		Unit	Remarks
				Min.	Max.		
Power supply rise time	t_R	V_{CC}	—	0.05	30	ms	
Power supply cutoff time	t_{OFF}	V_{CC}		4	—	ms	For repeated operation

* : V_{CC} must be less than 0.2 V before power-on.

Notes :
- The above rating values are for generating a power-on reset.
- Some internal registers are only initialized by a power-on reset. Always apply the power supply in accordance with the above ratings if you wish to initialize these registers.


tR
VCC
2.7 V
0.2 V
0.2 V
0.2 V
tOFF

Sudden changes in the power supply voltage may cause a power-on reset.
The recommended practice if you wish to change the power supply voltage while the device is operating is to raise the voltage smoothly as shown below. Also, changes to the supply voltage should be performed when the PLL clock is not in use. The PLL clock may be used, however, if the rate of voltage change is 1 V/s or less.


VCC
3.0 V
VSS
Recommended rate of voltage rise is 50 mV/ms or less.
Maintain RAM data

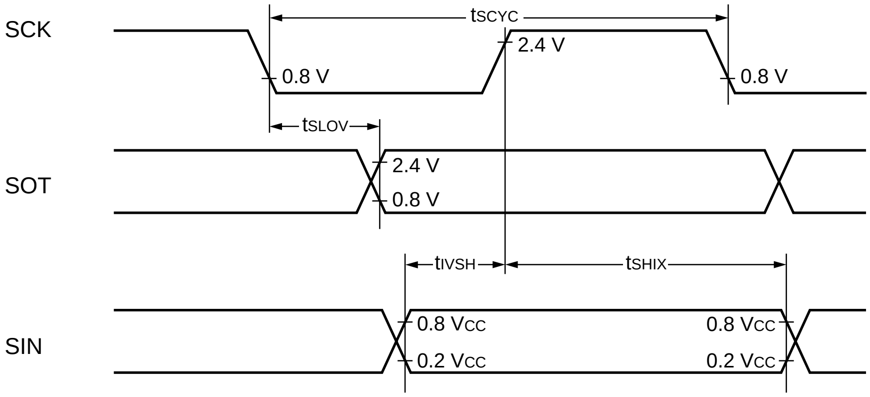
(4) UART0, UART1, and I/O Expansion Serial Timings

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

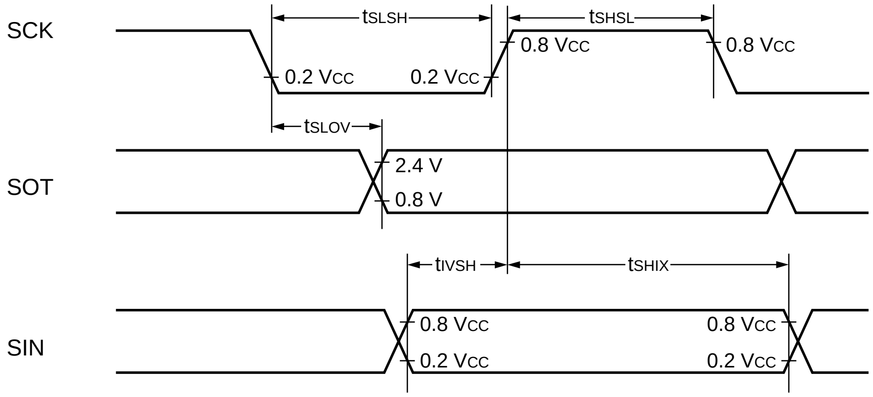
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal shift clock mode, output pin load is CL = 80 pF + 1 TTL	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1 SOT0, SOT1		–80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1 SIN0, SIN1		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1 SIN0, SIN1		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0, SCK1	External shift clock mode, output pin load is CL = 80 pF + 1 TTL	4 t_{CP}	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0, SCK1		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1 SOT0, SOT1		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1 SIN0, SIN1		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1 SIN0, SIN1		60	—	ns	

Notes :
- These are the AC ratings for CLK synchronous mode.
- C_L is the load capacitor connected to the pin for testing.
- t_{CP} is the machine cycle period (unit = ns)

- **Internal shift clock mode**


SCK
tSCYC
2.4 V
0.8 V
0.8 V
tSLOV
SOT
2.4 V
0.8 V
tIVSH
tSHIX
SIN
0.8 VCC
0.2 VCC
0.8 VCC
0.2 VCC

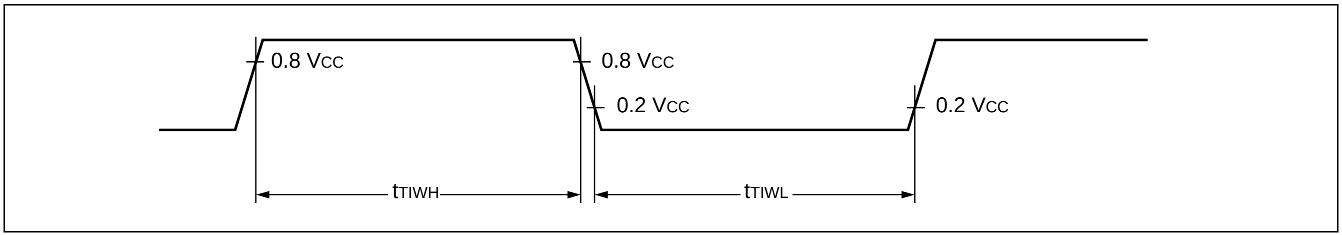
- **External shift clock mode**


SCK
tSLSH
tSHSL
0.2 VCC
0.2 VCC
0.8 VCC
0.8 VCC
tSLOV
SOT
2.4 V
0.8 V
tIVSH
tSHIX
SIN
0.8 VCC
0.2 VCC
0.8 VCC
0.2 VCC

(5) Timer Input Timings

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

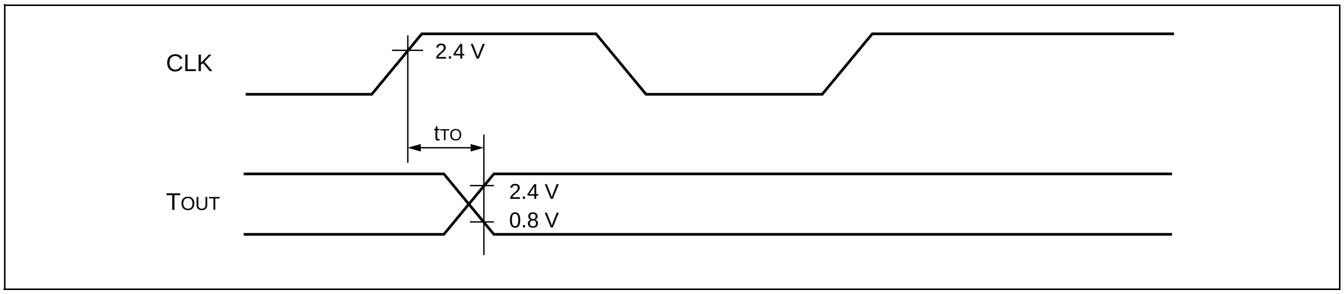
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH}, t_{TIWL}	FRCK, IN0, IN1, TIN0, TIN1	—	4 t_{CP}	—	ns	


0.8 Vcc
0.8 Vcc
0.2 Vcc
0.2 Vcc
tTIWH
tTIWL

(6) Timer Output Timings

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

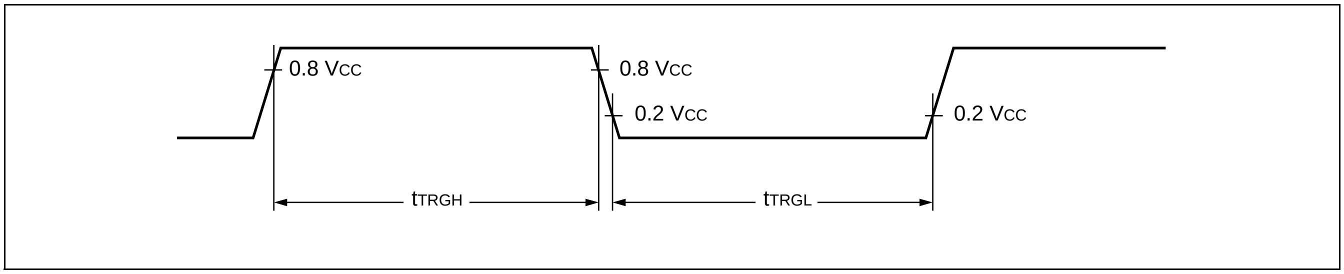
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
CLK ↑ → T_{OUT} change time	t_{TO}	RTO0 to RTO5, PPG0 to PPG5, TO0 to TO1	—	30	—	ns	


CLK
2.4 V
tTO
TOUT
2.4 V
0.8 V

(7) Trigger Input Timings

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TRGL}	INT0 to INT7, IN0 to IN3	—	5 t_{CP}	—	ns	In normal operation
				1	—	µs	In stop mode


0.8 Vcc
0.8 Vcc
0.2 Vcc
0.2 Vcc
tTRGH
tTRGL

5. Electrical Characteristics for the A/D Converter

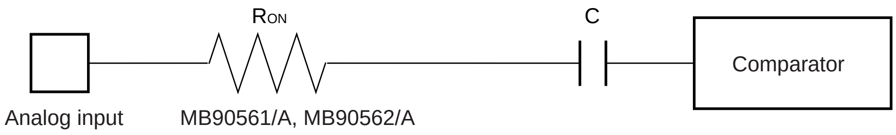
(T_A = –40 °C to +85 °C, 3.0 V ≤ AVR, V_{CC} = AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	10	—	bit	
Total error	—	—	—	—	±5.0	LSB	
Non-linearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} –3.5 LSB	+0.5	AV_{SS} +4.5 LSB	mV	1 LSB = AVRH/1024
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVR –6.5 LSB	AVR –1.5 LSB	AVR +1.5 LSB	mV	
Conversion time	—	—	—	176 t_{CP}	—	ns	
Sampling time	—	—	—	64 t_{CP}	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	0	—	AVR	V	
Reference voltage	—	AVR	2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVR	—	400	—	µA	
	I_{RH}	AVR	—	—	5	µA	*
Variation between channels	—	AN0 to AN7	—	—	4	LSB	

* : Current when A/D converter is not used and CPU is in stop mode (V_{CC} = AV_{CC} = AVR = 5.0 V)

Notes :
- The L reference voltage is fixed to AV_{SS}. The relative error increases as AVR becomes smaller.
- Ensure that the output impedance of the external circuit connected to the analog input meets the following condition :
  Output impedance of external circuit ≤ 10 kΩ (Sampling Time = 4.0 µs)
- If the output impedance of the external circuit is too high, the analog voltage sampling time may be too short.

- **Equivalent circuit of analog input circuit**



MB90561/A, MB90562/A
R_{ON} = 2.2 kΩ approx.
C = 45 pF approx.
MB90F562
R_{ON} = 3.2 kΩ approx.
C = 30 pF approx.
MB90F562/B
R_{ON} = 2.6 kΩ approx.
C = 28 pF approx.

Note : The values listed are an indication only.

6. Flash Memory Erase and Programming Performance

Parameter	Condition	Value			Units	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = + 25$ °C $V_{CC} = 5.0$ V	—	1	15	s	Excludes 00H programming prior erasure
Chip erase time		—	5	—	s	Excludes 00H programming prior erasure
Word (16 bit width) programming time		—	16	3,600	µs	Excludes system-level overhead
Erase/Program cycle	—	10,000	—	—	cycle	
Data holding time	—	100,000	—	—	h	

■ ELECTRICAL CHARACTERISTICS (MB90565 SERIES)

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	$V_{CC} \geq AV_{CC}$ *1
	AVR	V_{SS} – 0.3	V_{SS} + 4.0	V	$AV_{CC} \geq AVR \geq 0$ V *1
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
“L” level maximum output current	I_{OL}	—	15	mA	*3
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating ratio)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Average value (operating current × operating ratio)
“H” level maximum output current	I_{OH}	—	–15	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating ratio)
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	Average value (operating current × operating ratio)
Power consumption	Pd	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : AV_{CC} and AVR must not exceed V_{CC}. Also, AVR must not exceed AV_{CC}.

*2 : V_I and V_O must not exceed V_{CC} + 0.3 V.

*3 : The maximum output current is the peak value for a single pin.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	3.6	V	Normal operation (MB90V560)
		2.7	3.6	V	Normal operation (MB90F568, MB90567 and MB90568)
		2.5	3.6	V	Maintaining state in stop mode
Input “H” voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	CMOS input pin
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	CMOS hysteresis input pin
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD input pin
Input “L” voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	CMOS input pin
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	CMOS hysteresis input pin
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD input pin
Operating temperature	T_A	–40	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Output "H" voltage	V_{OH}	All output pins	V_{CC} = 3.0 V I_{OH} = –2.0 mA	V_{CC} – 0.5	V_{CC} – 0.3	—	V	
Output "L" voltage	V_{OL}	All output pins	V_{CC} = 3.0 V I_{OL} = 2.0 mA	—	0.2	0.4	V	
Input leak current	I_{IL}	All output pins	V_{CC} = 3.0 V V_{SS} < V_I < V_{CC}	–5	–1	5	µA	
Power supply current*	I_{CC}	V_{CC}	For V_{CC} = 3.3 V, internal frequency = 8 MHz, normal operation	—	14	22	mA	MB90567/568
			For V_{CC} = 3.3 V, internal frequency = 16 MHz, normal operation	—	27	40	mA	MB90567/568
			For V_{CC} = 3.3 V, internal frequency = 8 MHz, A/D operation in progress	—	18	27	mA	MB90567/568
			For V_{CC} = 3.3 V, internal frequency = 16 MHz, A/D operation in progress	—	32	45	mA	MB90567/568
			For V_{CC} = 3.3 V, internal frequency = 8 MHz, normal operation	—	18	28	mA	MB90F568
			For V_{CC} = 3.3 V, internal frequency = 16 MHz, normal operation	—	36	45	mA	MB90F568
			For V_{CC} = 3.3 V, internal frequency = 8 MHz, A/D operation in progress	—	23	33	mA	MB90F568
			For V_{CC} = 3.3 V, internal frequency = 16 MHz, A/D operation in progress	—	41	50	mA	MB90F568
			Flash write or erase	—	40	50	mA	MB90F568
	I_{CCS}		For V_{CC} = 3.3 V, internal frequency = 8 MHz, sleep mode	—	6	10	mA	MB90567/568 MB90F568*
			For V_{CC} = 3.3 V, internal frequency = 16 MHz, sleep mode	—	14	20	mA	MB90567/568 MB90F568*
	I_{CCH}		Stop mode, T_A = 25 °C	—	5	20	µA	

* : Value when low power mode bits (LPM0, 1) are set to "01" with an internal operating frequency of 8 MHz.

(Continued)

(Continued)

Parameter	**Sym-bol**	**Pin Name**	**Condition**	**Value**			**Unit**	**Remarks**
				Min.	**Typ.**	**Max.**		
Pull-up resistor	R_{UP}	P00 to P07 P10 to P17 $\overline{\text{RST}}$, MD0, MD1	—	20	65	200	kΩ	
Pull-down resistor	R_{DOWN}	MD2	—	20	65	200	kΩ	

Note : Current values are provisional and are subject to change without notice to allow for improvements to the characteristics. The power supply current is measured with an external clock.

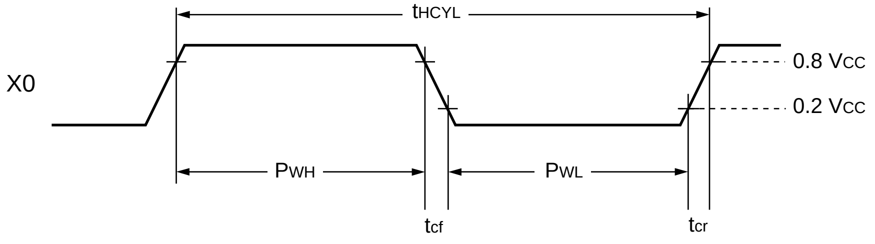
4. AC Characteristics

(1) Clock Timings

(MB90567/568/F568 : T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)
(MB90V560 : T_A = +25 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

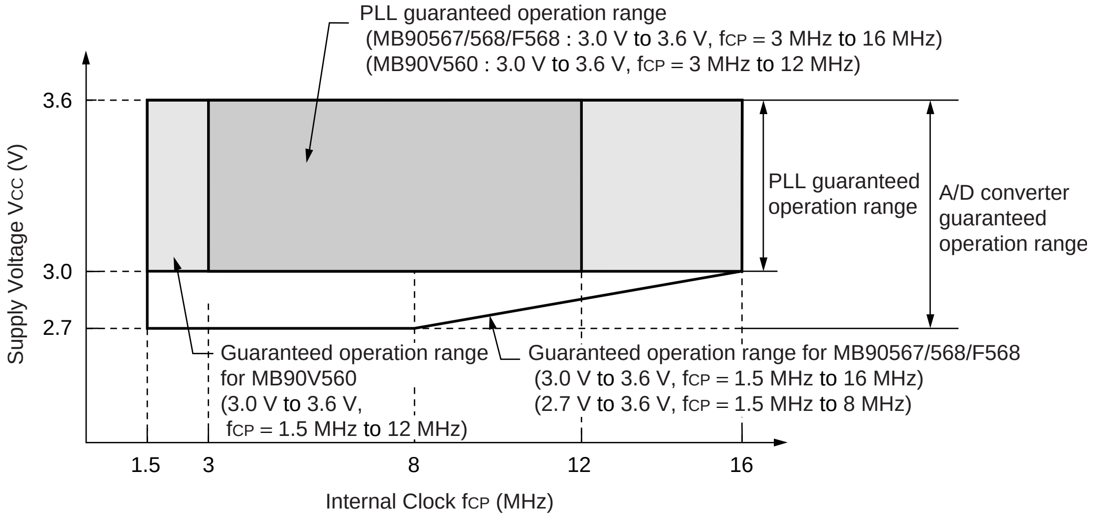
Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	f_C	X0, X1	—	3	—	12	MHz	MB90V560
				3	—	16	MHz	MB90567/568 MB90F568
Clock cycle time	t_{HCYL}	X0, X1		83.3	—	333	ns	MB90V560
				62.5	—	333	ns	MB90567/568 MB90F568
Input clock pulse width	P_{WH} P_{WL}	X0		10	—	—	ns	Recommended duty ratio = 30% to 70%
Input clock rise/fall time	tcr tcf	X0		—	—	5	ns	When using an external clock
Internal operating clock frequency	f_{CP}	—		1.5	—	12	MHz	MB90V560
				1.5	—	16	MHz	MB90567/568 MB90F568
Internal operating clock cycle time	t_{CP}	—		83.3	—	666	ns	MB90V560
				62.5	—	666	ns	MB90567/568 MB90F568

- **X0 and X1 clock timing**

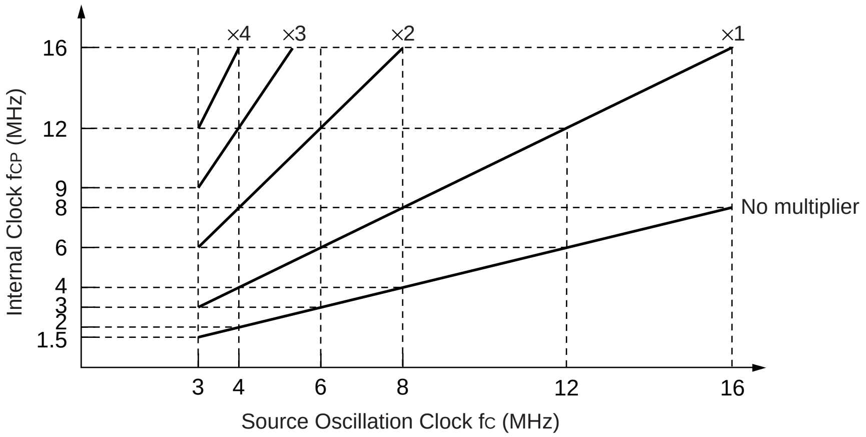


- **PLL guaranteed operation range**

Relationship between internal operating clock frequency and power supply voltage



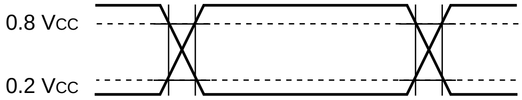
Relationship between oscillation frequency and internal operating clock frequency



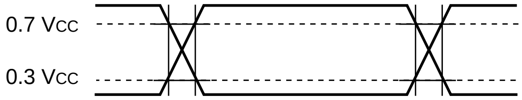
The AC ratings are specified for the following measurement reference voltages.

- **Input signal waveform**

Hysteresis input pin

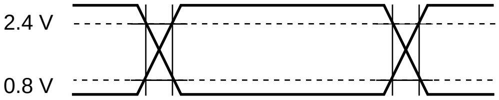


Pins other than hysteresis input or MD input pins



- **Output signal waveform**

Output pin



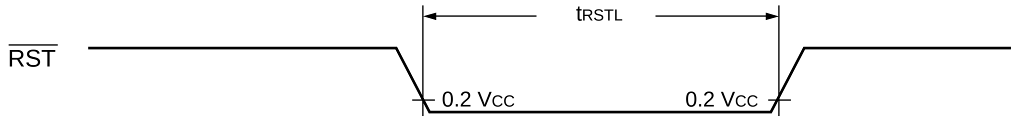
(2) Reset

(T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{\text{RST}}$	—	16 t_{CP}	—	ns	In normal operation
				Oscillator oscillation time* + 16 t_{CP}	—	ms	In stop mode

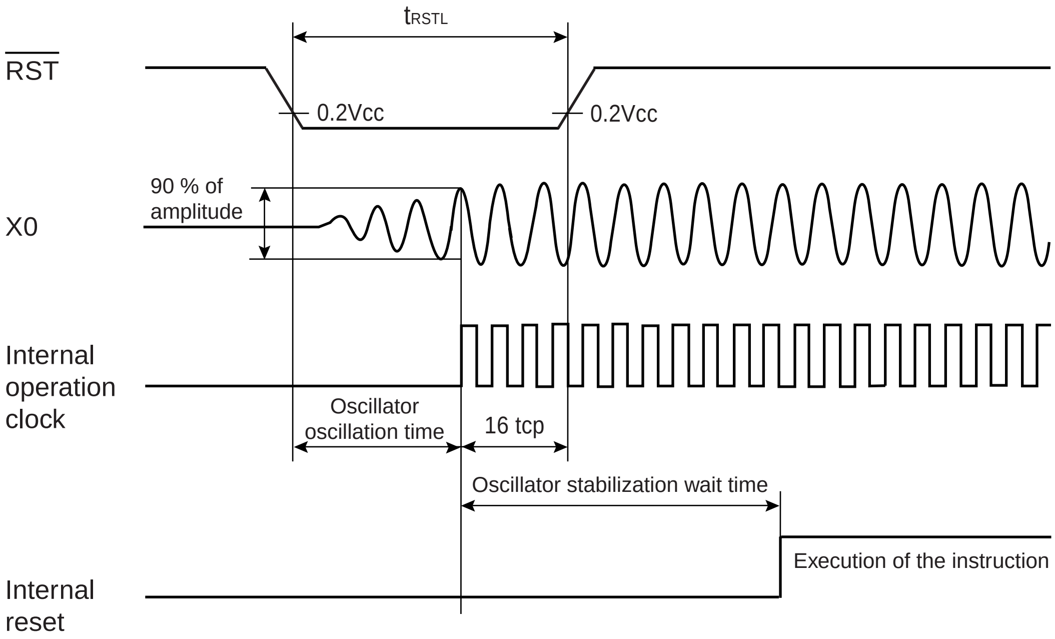
*: Oscillator oscillation time is the time to reach 90% amplitude. For a crystal oscillator, this is a few to several dozen ms; for a FAR/ceramic oscillator, this is several hundred µs to a few ms, and for an external clock this is 0 ms.

- In normal operation



tRSTL
RST
0.2 Vcc
0.2 Vcc

- In stop mode



tRSTL
RST
0.2Vcc
0.2Vcc
X0
90 % of amplitude
Internal operation clock
Oscillator oscillation time
16 tcp
Oscillator stabilization wait time
Execution of the instruction
Internal reset

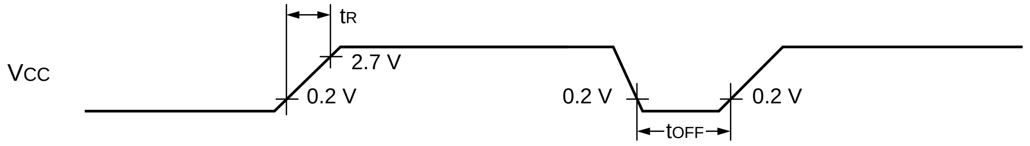
(3) Power-On Reset

(T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

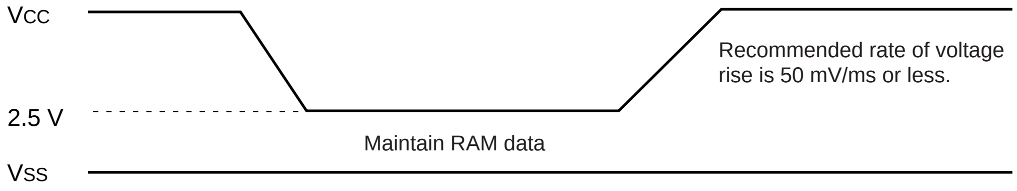
Parameter	Symbol	Pin Name	Condi-tion	Value		Unit	Remarks
				Min.	Max.		
Power supply rise time	t_R	V_{CC}*	—	0.05	30	ms	
Power supply cutoff time	t_{OFF}	V_{CC}		4	—	ms	For repeated operation

* : V_{CC} must be less than 0.2 V before power-on.

Notes :
- The above rating values are for generating a power-on reset.
- Some internal registers are only initialized by a power-on reset. Always apply the power supply in accordance with the above ratings if you wish to initialize these registers.



Sudden changes in the power supply voltage may cause a power-on reset.
The recommended practice if you wish to change the power supply voltage while the device is operating is to raise the voltage smoothly as shown below. Also, changes to the supply voltage should be performed when the PLL clock is not in use. The PLL clock may be used, however, if the rate of voltage change is 1 V/s or less.



Recommended rate of voltage rise is 50 mV/ms or less.

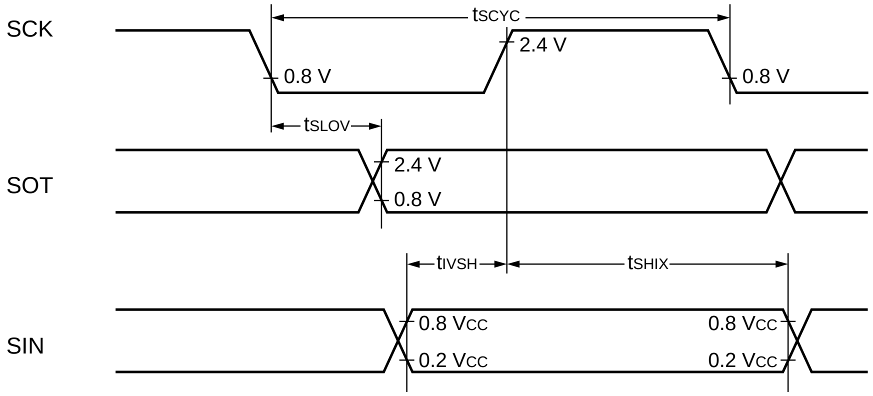
(4) UART0 and UART1

(T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

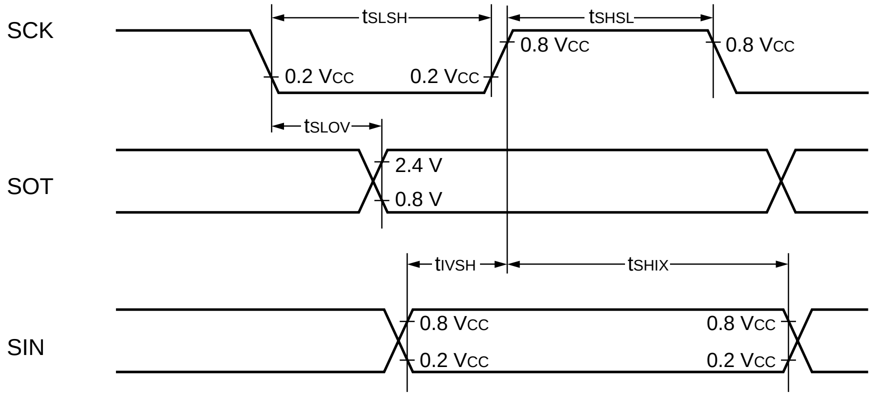
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal shift clock mode, output pin load is C_L = 80 pF + 1 TTL	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1 SOT0, SOT1		–80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1 SIN0, SIN1		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1 SIN0, SIN1		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0, SCK1	External shift clock mode, output pin load is C_L = 80 pF + 1 TTL	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0, SCK1		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1 SOT0, SOT1		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1 SIN0, SIN1		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1 SIN0, SIN1		60	—	ns	

Notes :
- These are the AC ratings for CLK synchronous mode.
- CV is the load capacitor connected to the pin for testing.
- t_{CP} is the machine cycle period (unit = ns)

- **Internal shift clock mode**


SCK
tSCYC
0.8 V
2.4 V
0.8 V
tSLOV
SOT
2.4 V
0.8 V
tIVSH
tSHIX
SIN
0.8 Vcc
0.2 Vcc
0.8 Vcc
0.2 Vcc

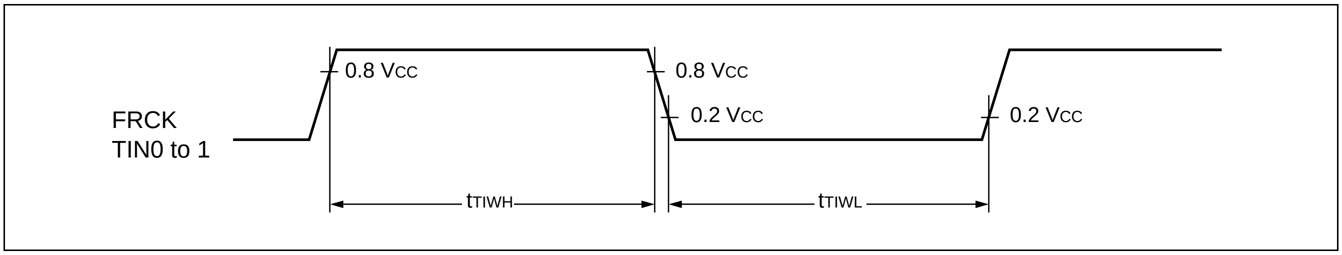
- **External shift clock mode**


SCK
tSLSH
tSHSL
0.2 Vcc
0.2 Vcc
0.8 Vcc
0.8 Vcc
tSLOV
SOT
2.4 V
0.8 V
tIVSH
tSHIX
SIN
0.8 Vcc
0.2 Vcc
0.8 Vcc
0.2 Vcc

(5) Timer Input Timings

(T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

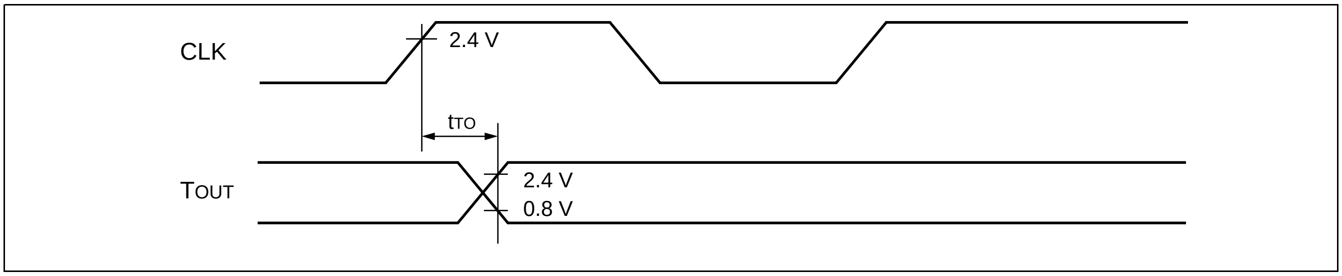
Parameter	Symbol	Pin Name	Condi-tion	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH}, t_{TIWL}	FRCK, TIN0, TIN1	—	4 t_{CP}	—	ns	


FRCK
TIN0 to 1
0.8 Vcc
0.8 Vcc
0.2 Vcc
0.2 Vcc
tTIWH
tTIWL

(6) Timer Output Timings

(T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

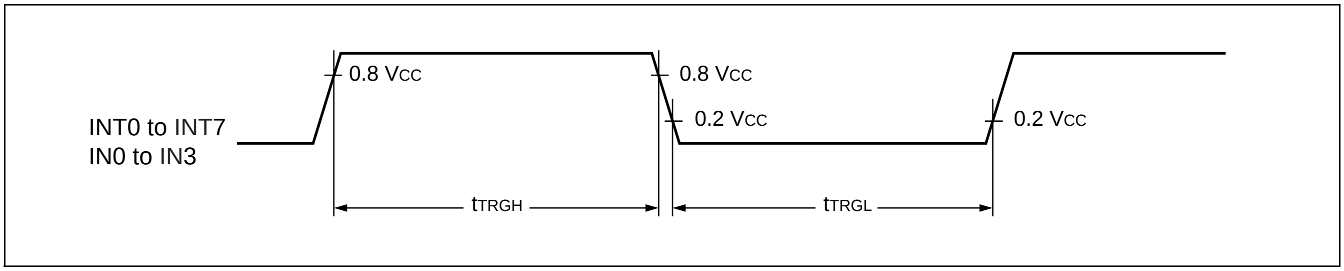
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
CLK ↑ → T_{OUT} change time	t_{TO}	RTO0 to RTO5, PPG0 to PPG5 TO0, TO1	—	30	—	ns	


CLK
2.4 V
tTO
TOUT
2.4 V
0.8 V

(7) Trigger Input Timings

(T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TRGL}	INT0 to INT7, IN0 to IN3	—	5 t_{CP}	—	ns	In normal operation
				1	—	µs	In stop mode


INT0 to INT7
IN0 to IN3
0.8 Vcc
0.8 Vcc
0.2 Vcc
0.2 Vcc
tTRGH
tTRGL

5. Electrical Characteristics for the A/D Converter

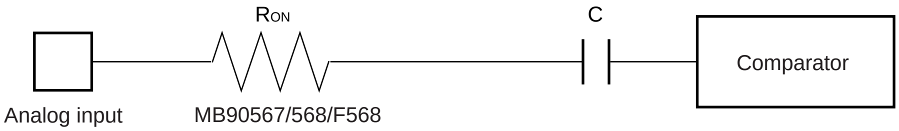
(MB90567/568/F568 : T_A = –40 °C to +85 °C, 2.7 V ≤ AVR, V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)
(MB90V560 : T_A = +25 °C, 3.0 V ≤ AVR, V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Non-linearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} –1.5 LSB	AV_{SS} +0.5	AV_{SS} +2.5 LSB	mV	1 LSB = AVRH/1024
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVR –3.5 LSB	AVR –1.5 LSB	AVR +0.5 LSB	mV	
Conversion time	—	—	—	66 t_{CP}	—	ns	
Sampling time	—	—	—	32 t_{CP}	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	0	—	AVR	V	
Reference voltage	—	AVR	2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	1	5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVR	—	100	200	µA	
	I_{RH}	AVR	—	—	5	µA	*
Variation between channels	—	AN0 to AN7	—	—	4	LSB	

* : Current when A/D converter is not used and CPU is in stop mode (V_{CC} = AV_{CC} = AVR = 3.3 V)

Notes :
- The L reference voltage is fixed to AV_{SS}. The relative error increases as AVR becomes smaller.
- Ensure that the output impedance of the external circuit connected to the analog input meets the following condition :
  Output impedance of MB90F568 external circuit ≤ 14 kΩ (Sampling Time = 4 µs)
  Output impedance of MB90567/568 external circuit ≤ 7 kΩ (Sampling Time = 4 µs)
- If the output impedance of the external circuit is too high, the analog voltage sampling time may be too short.

- **Equivalent circuit of analog input circuit**


RON
C
Comparator
Analog input
MB90567/568/F568

MB90567/568/F568
R_{ON} = 7.1 kΩ approx.
C = 48.3 pF approx.

Note : The values listed are an indication only.

6. Flash Memory Erase and Programming Performance

Parameter	Condition	Value			Units	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = + 25$ °C $V_{CC} = 3.3$ V	—	1	15	s	Excludes 00H programming prior erasure
Chip erase time		—	5	—	s	Excludes 00H programming prior erasure
Word (16 bit width) programming time		—	16	3,600	μs	Excludes system-level overhead
Erase/Program cycle	—	10,000	—	—	cycle	
Data holding time	—	100,000	—	—	h	

- **Points to note regarding the MB90F568, 567, and 568 specifications**

This section describes the specification differences between the MB90F568/567/568 and the MB90F562/F562B/562/562A/561/561A.

(1) Functional differences

1) The 5 V to 3 V regulator has been removed in the MB96565 series.
The C pin has been changed to an N.C. pin.

2) The A/D converter unit in the MB96565 series has changed from a 5 V version to a 3 V version.
However, the conversion time and sampling time remain the same.

3) The maximum voltage that can be applied to I/O pins has changed from 5 V to 3 V in the MB96565 series.

4) Added transfer counter clear function to UART in the MB96565 series.
This function restores the UART to its initial state when “0” is written to the UART reset bit.

(2) Points to note when using the devices

The MB90F562, F562B, and F568 use P60 (14) as SIN1, P61 (15) as SOT1, and P40 (60) as SCK0 when performing on-board programming.

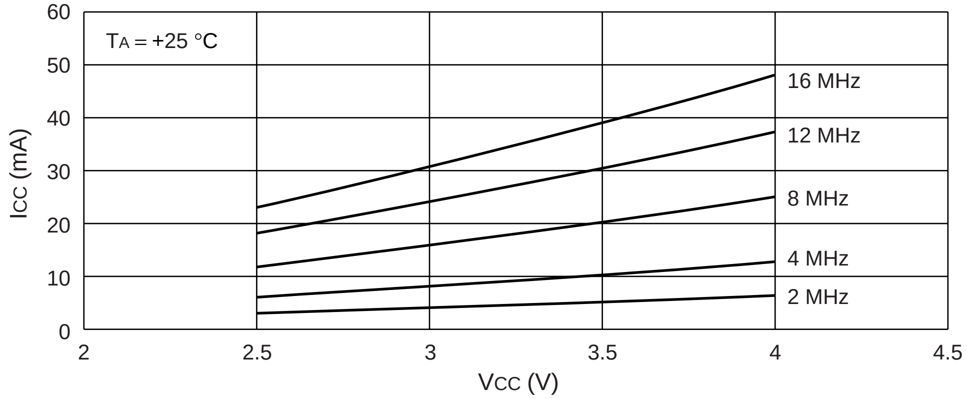
Use the following pin settings when performing on-board programming.

Pin Name	Pin I/O Level*	Remarks
MD2	“H” level	Serial write mode settings
MD1	“H” level	
MD0	“L” level	
SIN1	Serial data input	Normally shared with P60
SOT1	Serial data output	Normally shared with P61
SCK0	Serial clock	Normally shared with P40
P00	“L” level	
P01	“H” level	Input “L” level for PC writing

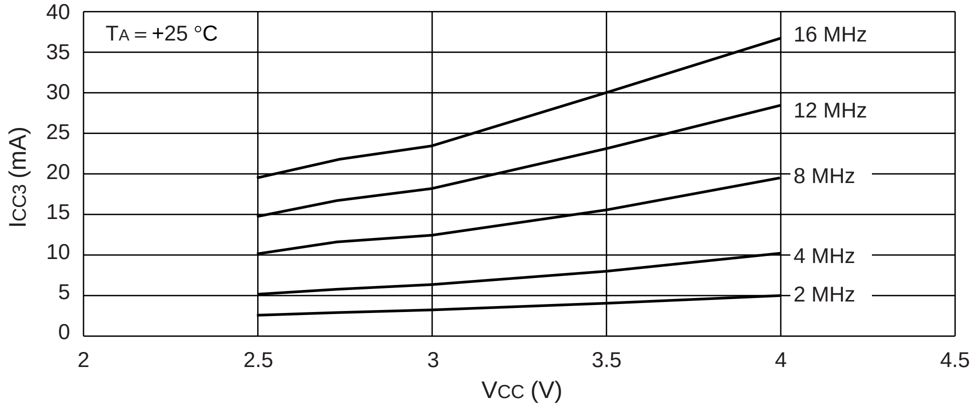
* : These settings are for using a Yokogawa Digital Computer Corporation writer for on-board programming. Alternatively, writing can be performed from a PC, but a special write program is required.

■ EXAMPLE CHARACTERISTICS

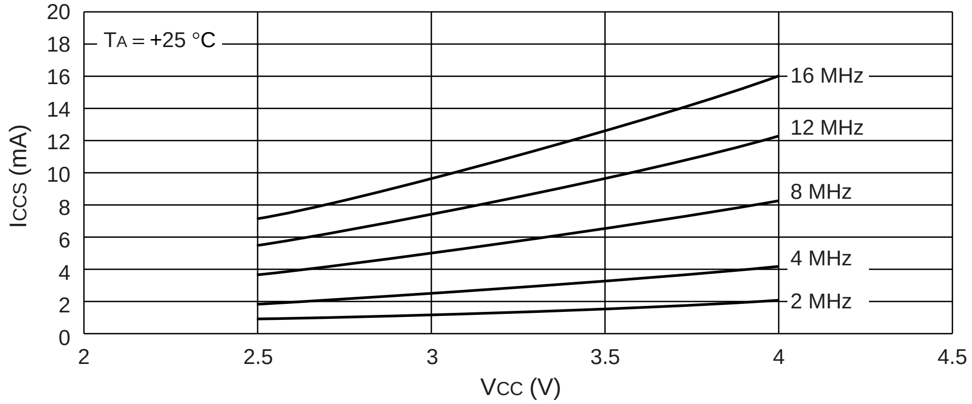
MB90F568 I_{CC} – V_{CC}



MB90568 I_{CC} – V_{CC}



MB90F568 I_{CCS} – V_{CC}



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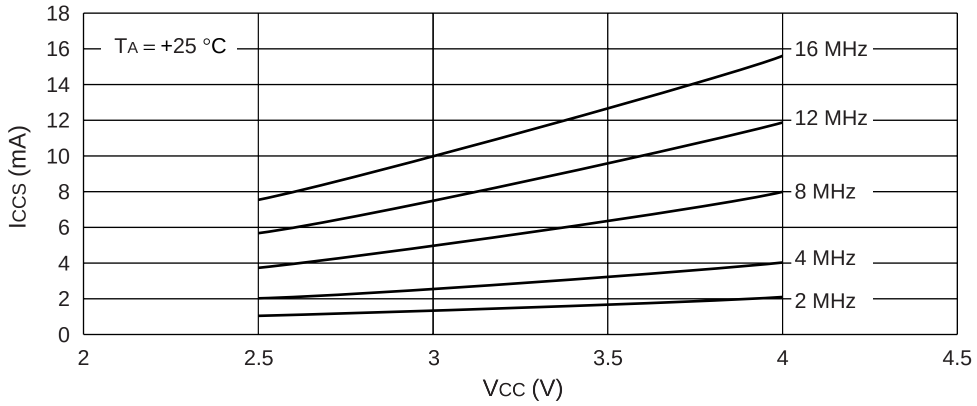
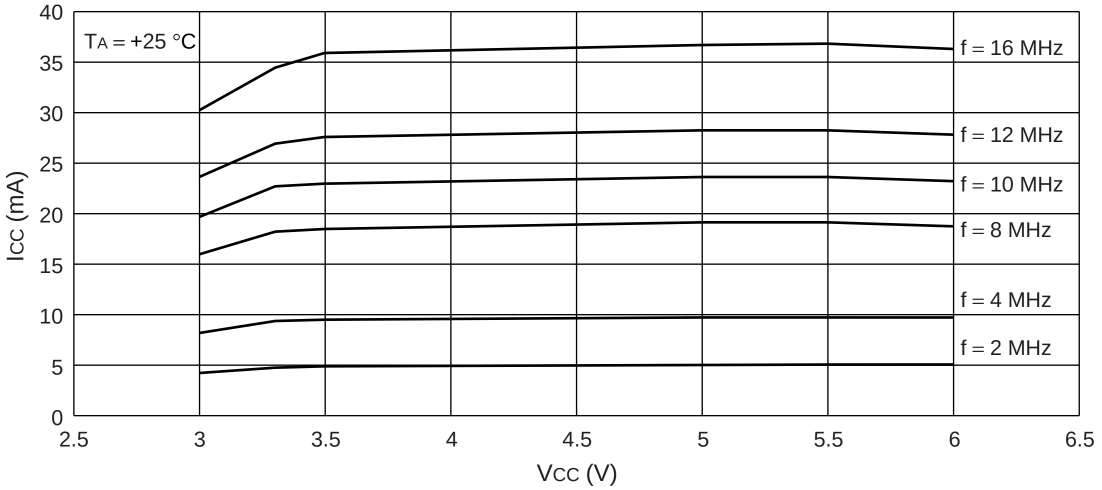
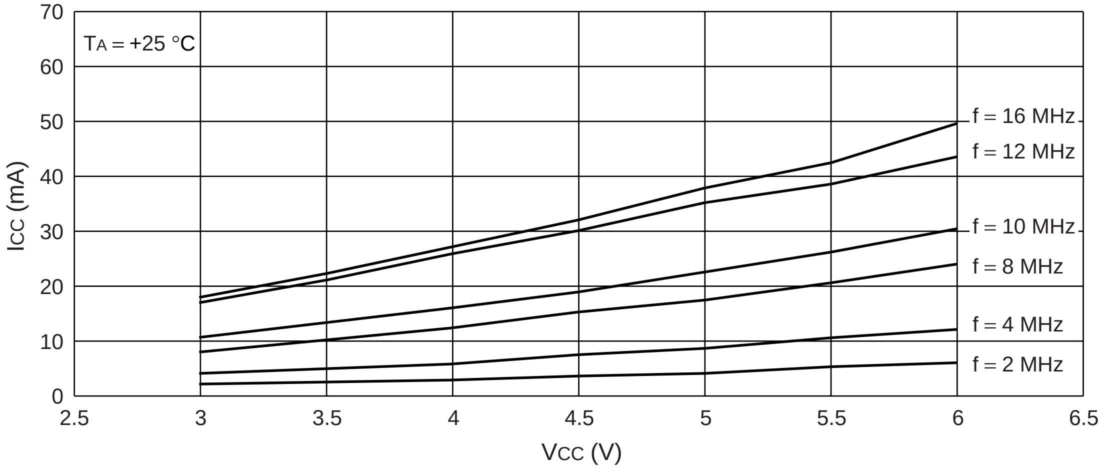
MB90568 I_{CCS} – V_{CC}



MB90F562 I_{CC} – V_{CC}



MB90562 I_{CC} – V_{CC}



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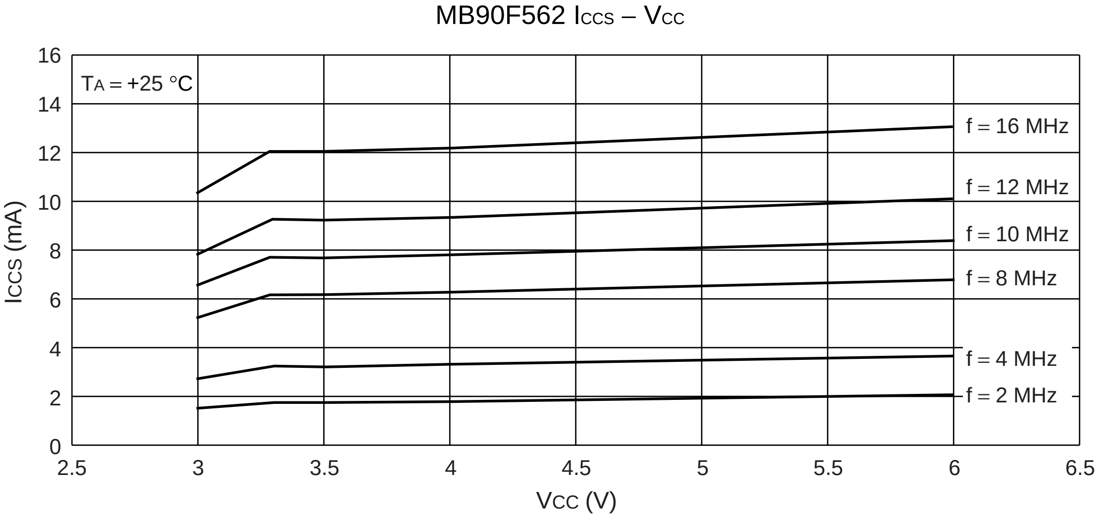
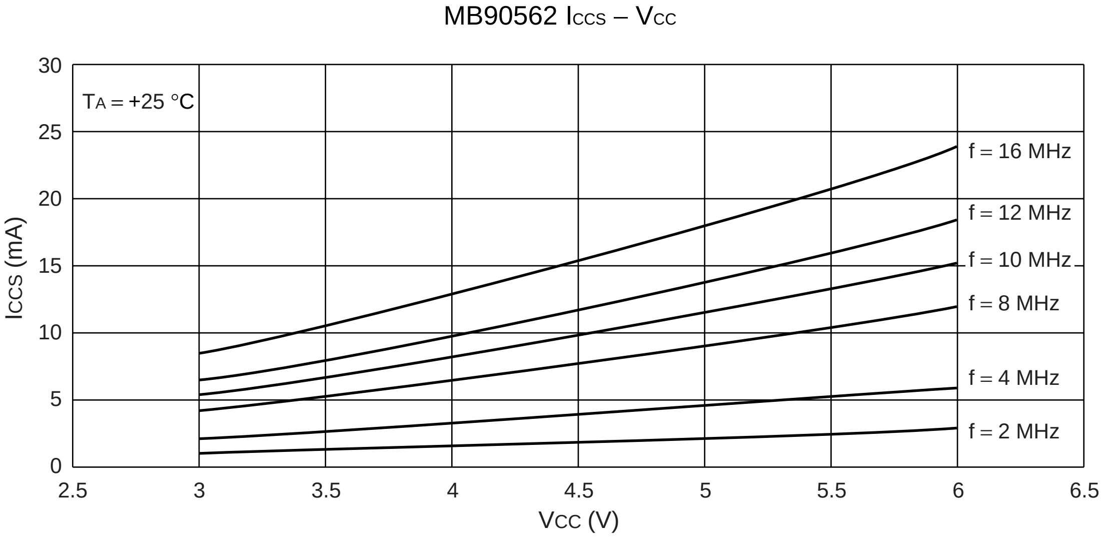

MB90F562 ICCS – VCC
TA = +25 °C
ICCS (mA)
VCC (V)
f = 16 MHz
f = 12 MHz
f = 10 MHz
f = 8 MHz
f = 4 MHz
f = 2 MHz
0
2
4
6
8
10
12
14
16
2.5
3
3.5
4
4.5
5
5.5
6
6.5


MB90562 ICCS – VCC
TA = +25 °C
ICCS (mA)
VCC (V)
f = 16 MHz
f = 12 MHz
f = 10 MHz
f = 8 MHz
f = 4 MHz
f = 2 MHz
0
5
10
15
20
25
30
2.5
3
3.5
4
4.5
5
5.5
6
6.5

■ ORDERING INFORMATION

- **MB90560 series**

Part No.	Package	Remarks
MB90561P MB90562P MB90561AP MB90562AP MB90F562P MB90F562BP	64-pin plastic SH-DIP (DIP-64P-M01)	
MB90561PF MB90562PF MB90561APF MB90562APF MB90F562PF MB90F562BPF	64-pin plastic QFP (FPT-64P-M06)	
MB90561PFM MB90562PFM MB90561APFM MB90562APFM MB90F562PFM MB90F562BPFM	64-pin plastic LQFP (FPT-64P-M09)	

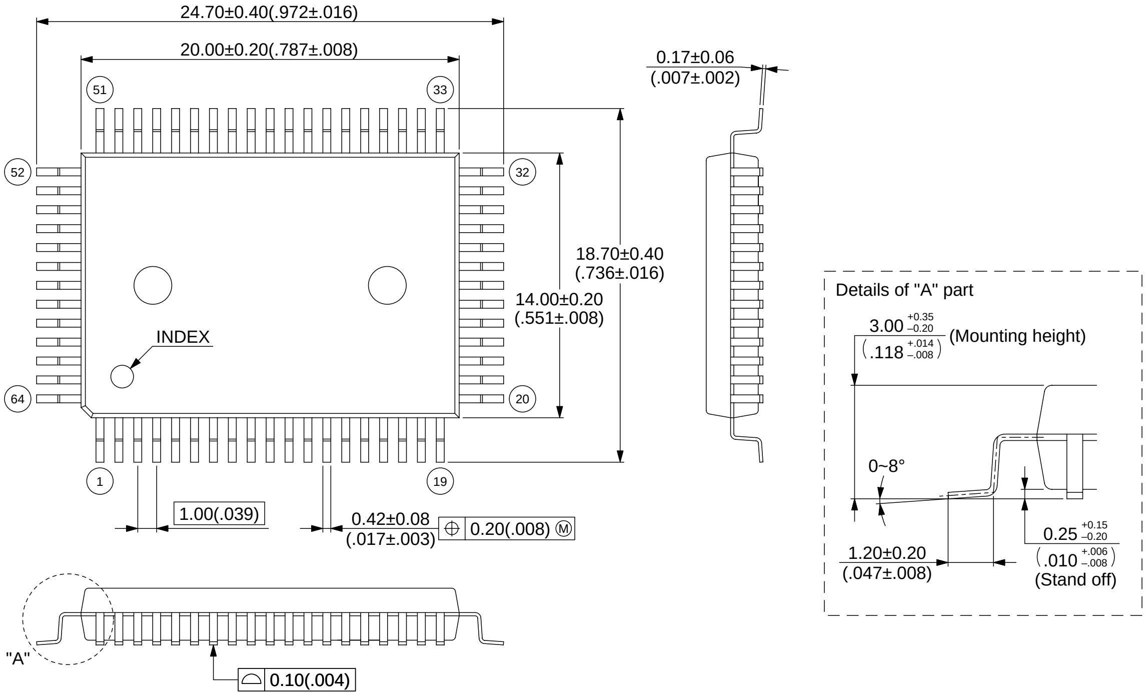
- **MB90565 series**

Part No.	Package	Remarks
MB90567PF MB90568PF MB90F568PF	64-pin plastic QFP (FPT-64P-M06)	
MB90567PFM MB90568PFM MB90F568PFM	64-pin plastic LQFP (FPT-64P-M09)	

■ PACKAGE DIMENSIONS

64-pin plastic QFP
(FPT-64P-M06)

Note : Pins width and pins thickness include plating thickness.


24.70±0.40(.972±.016)
20.00±0.20(.787±.008)
51
33
52
32
64
20
1
19
INDEX
18.70±0.40
(.736±.016)
14.00±0.20
(.551±.008)
0.17±0.06
(.007±.002)
1.00(.039)
0.42±0.08
(.017±.003)
0.20(.008) Ⓜ
"A"
0.10(.004)
Details of "A" part
3.00 +0.35 −0.20
(.118 +.014 −.008)
(Mounting height)
0~8°
1.20±0.20
(.047±.008)
0.25 +0.15 −0.20
(.010 +.006 −.008)
(Stand off)

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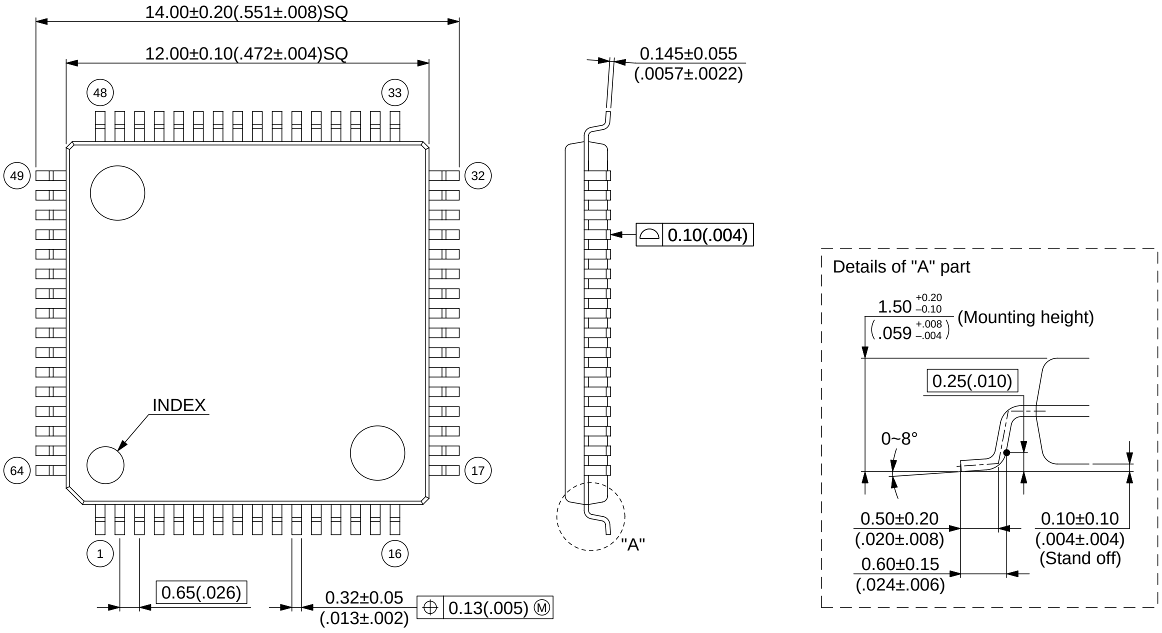
Dimensions in mm (inches)

(Continued)

64-pin plastic LQFP
(FPT-64P-M09)

Note : Pins width and pins thickness include plating thickness.


14.00±0.20(.551±.008)SQ
12.00±0.10(.472±.004)SQ
48
33
49
32
64
17
1
16
INDEX
0.65(.026)
0.32±0.05
(.013±.002)
⊕ 0.13(.005) Ⓜ
0.145±0.055
(.0057±.0022)
⌓ 0.10(.004)
"A"
Details of "A" part
1.50 +0.20 −0.10
(.059 +.008 −.004)
(Mounting height)
0.25(.010)
0~8°
0.50±0.20
(.020±.008)
0.60±0.15
(.024±.006)
0.10±0.10
(.004±.004)
(Stand off)

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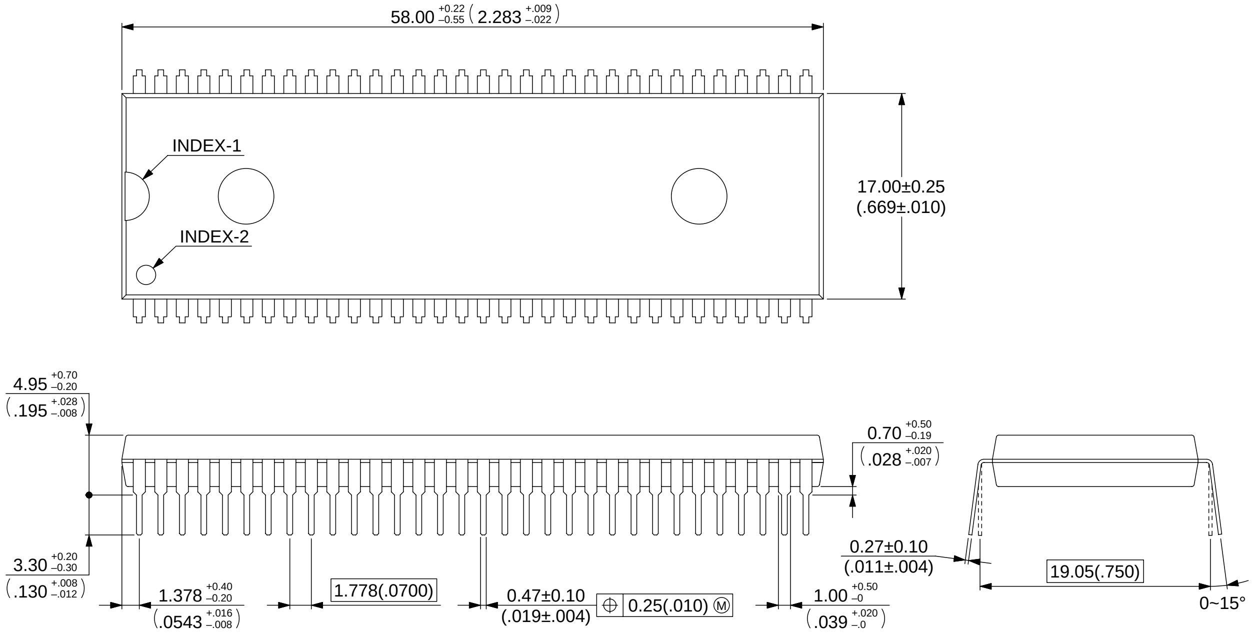
Dimensions in mm (inches)

(Continued)

(Continued)

64-pin plastic SH-DIP
(DIP-64P-M01)

Note : Pins width and pins thickness include plating thickness.


58.00 +0.22 −0.55 (2.283 +.009 −.022)
INDEX-1
INDEX-2
17.00±0.25
(.669±.010)
4.95 +0.70 −0.20
(.195 +.028 −.008)
0.70 +0.50 −0.19
(.028 +.020 −.007)
3.30 +0.20 −0.30
(.130 +.008 −.012)
1.378 +0.40 −0.20
(.0543 +.016 −.008)
1.778(.0700)
0.47±0.10
(.019±.004)
0.25(.010) Ⓜ
1.00 +0.50 −0
(.039 +.020 −.0)
0.27±0.10
(.011±.004)
19.05(.750)
0~15°

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Dimensions in mm (inches)

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