68360 FEATURES

- 25MHz Operating Frequency
- Military Temperature Range: -55°C to +125°C
- Packaging
  - 241 pin Ceramic PGA (P3)
  - 240 pin Ceramic Quad Flatpack, CQFP (Q3)
- CPU32+ Processor (4.5 MIPS at 25MHz)
  - 32-Bit Version of the CPU32 Core (Fully Compatible with the CPU32)
  - Background Debug Mode
  - Byte-Misaligned Addressing
- Up to 32-Bit Data Bus (Dynamic Bus Sizing for 8 and 16 Bits)
- Up to 32 Address Lines (At Least 28 Always Available)
- Complete Static Design (0-25MHz Operation)
- Slave Mode to Disable CPU32+ (Allows Use with External Processors)
- Memory Controller (eight banks)
- Four General-Purpose Timers
- Two Independent DMAs (IDMAs)
- System Intergration Module (SIM60)
- Interrupts:
  - Seven External IRQ Lines
  - 12 Port Pins with Interrupt Capability
  - 16 Internal Interrupt Sources
- Communications Processor Module (CPM)
- Four Baud Rate Generators
- Four SCCs
- Two SMCs
- One SPF
- Time Slot Assigner
- Supports Two TDM Channels

DESCRIPTION

The WC32P360 Intergrated Communication Controller is a flexible chip intergrated microprocessor and peripheral combination that can be used in various controller applications. It excels in communication activities. There are four serial communications controllers (SCCs) on the device with seven serial channels: four SCCs, two serial management controllers (SCMs), and one serial peripheral interface.

FIG. 1
BLOCK DIAGRAM

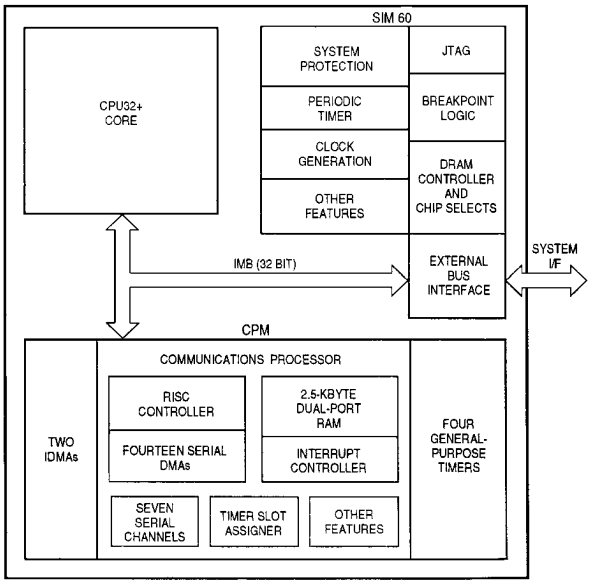


FIG. 2 PIN CONFIGURATION FOR WC32P360-25XM, CQFP (Q3)

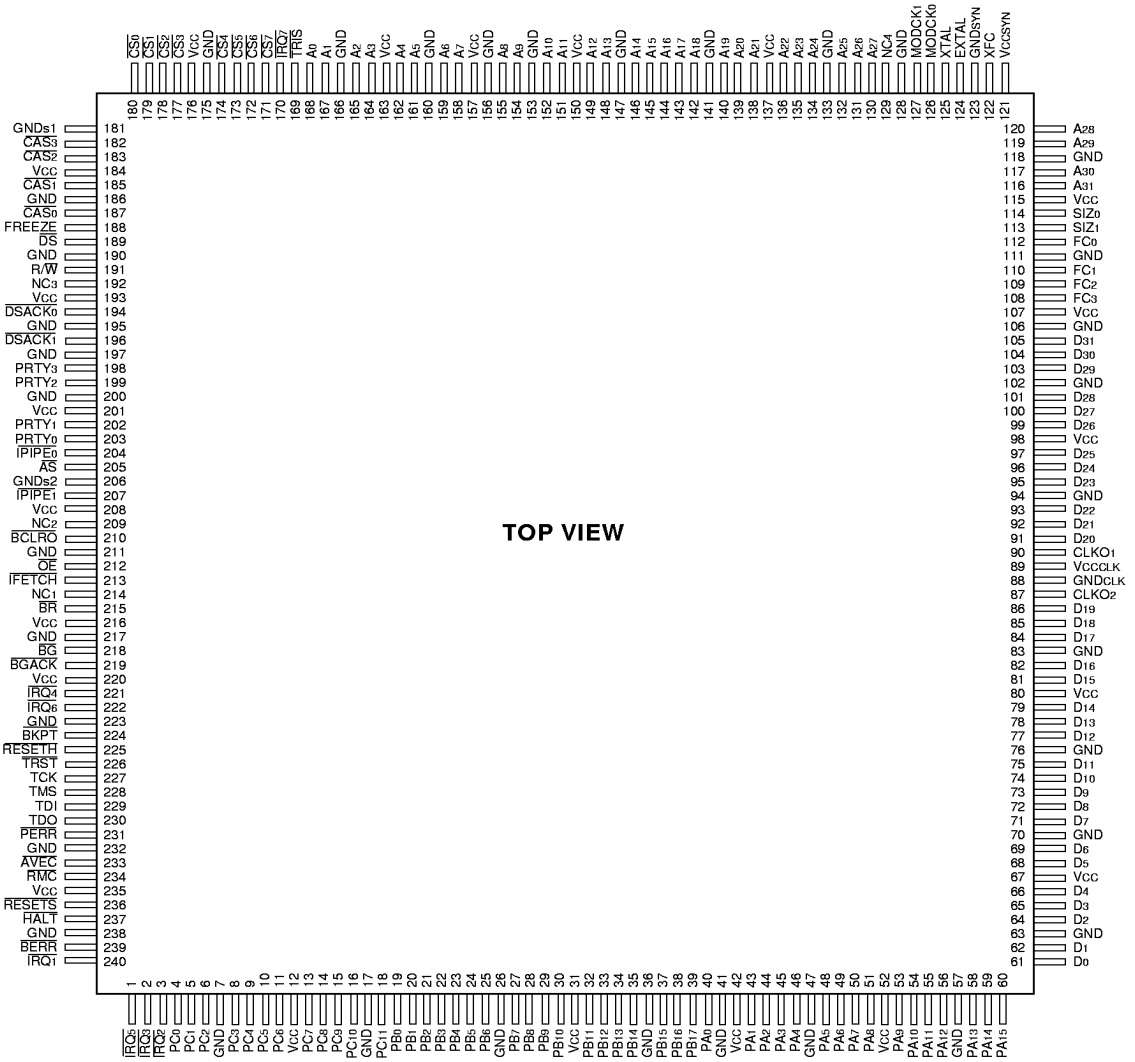


FIG. 3 PIN CONFIGURATION FOR WC32P360-25XM, PGA (P3)

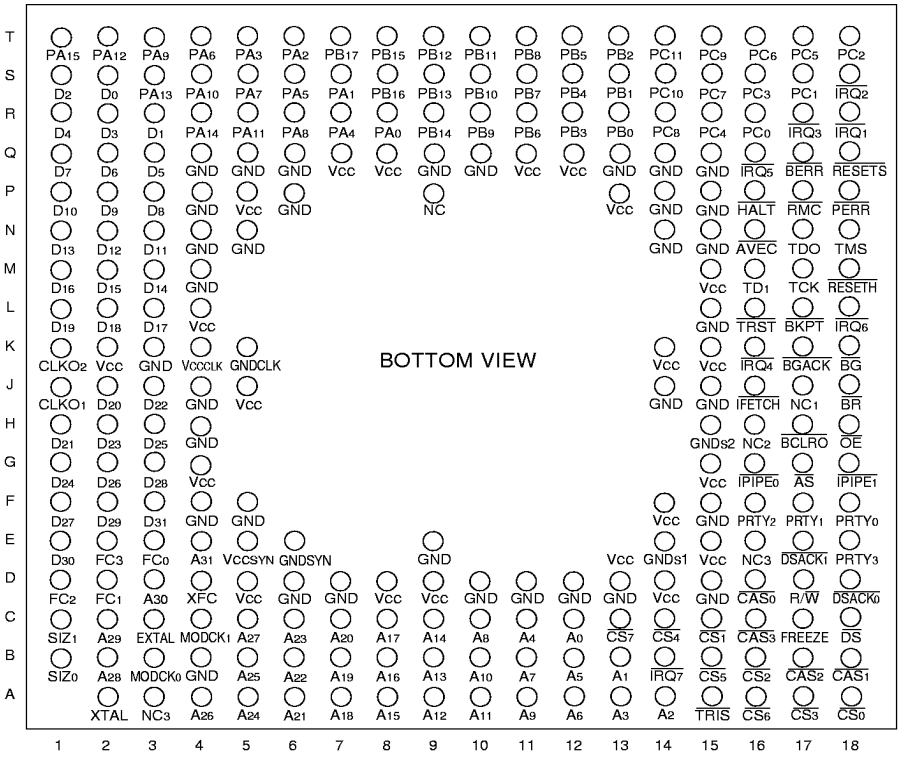
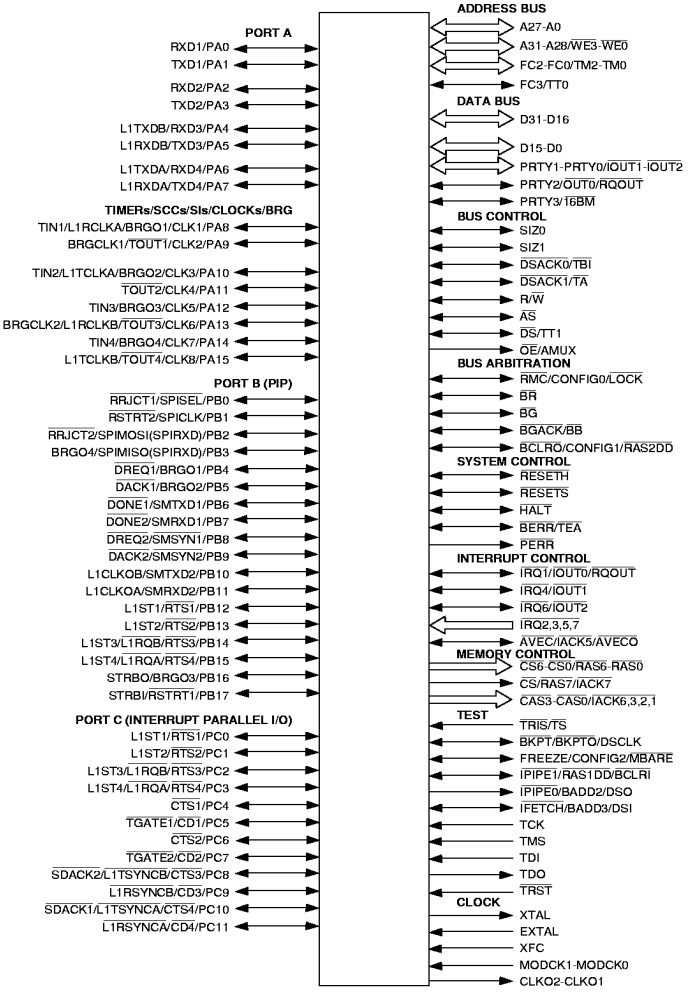


FIG. 4
FUNCTIONAL SIGNAL GROUPS



SIGNAL INDEX (NORMAL OPERATION)

Group	Signal Name	Mnemonic	Function
Address	Address Bus	A27-A0	Lower 27 bits of address bus. (I/O)
	Address Bus/Byte Write Enables	A31-A28/$\overline{WE0}$-$\overline{WE3}$	Upper four bits of address bus (I/O), or write enable signals (O) for accesses to external memory or peripherals.
	Function Codes	FC3-FC0	Identifies the processor state and the address space of the current bus cycle. (I/O)
Data	Data Bus 31-16	D31-D16	Upper 16-bit data bus used to transfer byte or word data. Used in 16-bit bus mode (I/O).
	Data Bus 15-0	D15-D0	Lower 16-bit data bus used to transfer 3-byte or long-word data (I/O). Not used in 16-bit bus mode.
Parity	Parity 2-0	PRTY2-0	Parity signals for byte writes/reads from/to external memory module (I/O).
	Parity 3/$\overline{16BM}$	PRTY3/$\overline{16BM}$	Parity signals for byte writes/reads from/to external memory module or defines 16-bit bus mode (I/O).
	Parity Error	$\overline{PERR}$	Indicates a parity error during a read cycle (O).
Memory Controller	Chip Select/Row Address Select 7/Interrupt Acknowledge 7	$\overline{CS}$/$\overline{RAS7}$/$\overline{IACK7}$	Enables peripherals or DRAMs at programmed addresses (O) or interrupt level 7 acknowledge line (O).
	Chip Select 6-0/Row Address Select 6-0	$\overline{CS6}$-$\overline{CS0}$/$\overline{RAS6}$-$\overline{RAS0}$	Enables peripherals or DRAMs at programmed addresses. (O)
	Column Address Select 3-0/Interrupt Acknowledge 1, 2, 3, 6	CAS3-CAS0/ $\overline{IACK6,3,2,1}$	DRAM column address select or interrupt level acknowledge lines. (O)
Bus Arbitration	Bus Request	$\overline{BR}$	Indicates that an external device requires bus mastership. (I)
	Bus Grant	$\overline{BG}$	Indicates that the current bus cycle is complete and the WC32P360 has relinquished the bus. (O)
	Bus Grant Acknowledge	$\overline{BGACK}$	Indicates that an external device has assumed bus mastership. (I)
	Read-Modify-Write Cycle/Initial Configuration 0	$\overline{RMC}$/CONFIG0	Identifies the bus cycle as part of an indivisible read-modify-write operation (I/O) or initial QUICC configuration select (I).
	Bus Clear Out/Initial	$\overline{BCLRO}$/CONFIG1/ $\overline{RAS2DD}$	Indicates that an internal device requires the external bus (Open-Drain O) or initial QUICC configuration select (I) or row address select 2 double drive output (O).
Bus Control	Data and Size Acknowledge	$\overline{DSACK1}$-$\overline{DSACK0}$	Provides asynchronous data transfer acknowledgment and dynamic bus sizing (Open-Drain I/O but driven high before three-stated).
	Address Strobe	$\overline{AS}$	Indicates that a valid address is on the address bus. (I/O)
	Data Strobe	$\overline{DS}$	During a read cycle, DS indicates that an external device should place valid data on the data bus. During a write cycle, DS indicates that valid data is on the data bus. (I/O)
	Size	SIZ1-SIZ0	Indicates the number of bytes remaining to be transferred fro this cycle. (I/O)
	Read/Write	R/$\overline{W}$	Indicates the direction of data transfer on the bus. (I/O)
	Output Enable/ Address Multiplex	$\overline{OE}$/AMUX	active during a read cycle, DS indicates that an external device should place valid data on the data bus (O) or provides a strobe for external address multiplexing in DRAM accesses if internal multiplexing is not used (O).
Interrupt Control	Interrupt Request Level 7-1	$\overline{IRQ7}$-$\overline{IRQ1}$	Provides external interrupt requests to the CPU32+ at priority levels 7-1. (I)
	Autovector/Interrupt Acknowledge 5	$\overline{AVEC}$/$\overline{IACK5}$	Autovector request during an interrupt acknowledge cycle (Open-Drain I/O) or interrupt level 5 acknowledge line (O).
System Control	soft Reset	$\overline{RESETS}$	Soft system reset. (Open-Drain I/O)
	Hard Reset	$\overline{RESETH}$	Hard system reset (Open-Drain I/O)
	Halt	$\overline{HALT}$	Suspends external bus activity. (Open-Drain I/O)
	Bus Error	$\overline{BERR}$	Indicates an erroneous bus operation is being attempted. (Open-Drain I/O)
Clock and Test	System Clock Out 1	CLKO1	Internal system clock output 1. (O)
	System Clock Out 2	CLKO2	Internal system clock output 2 – normally 2x CLKO1. (O)
	Crystal Oscillator	EXTAL, XTAL	Connections for an external crystal to the internal oscillator circuit. EXTAL (I), XTAL (O).

SIGNAL INDEX (NORMAL OPERATION) (cont'd.)

Group	Signal Name	Mnemonic	Function
Clock and Test	External Filter Capacitor	XFC	Connection pin for an external capacitor to filter the circuit of the PLL (I).
	Clock Mode Select 1-0	MODCK1-MODCK0	Selects the source of the internal system clock. (I) THESE PINS SHOULD NOT BE SET TO 00
	Instruction Fetch/ Development Serial Input	$\overline{\text{IFETCH}}$/DSI	Indicates when the CPU32+ is performing an instruction word prefetch (O) or input to the CPU32+ background debug mode (O).
	Instruction Pipe 0/ Development Serial Output	$\overline{\text{IPIPE0}}$/DSO	Used to track movement of words through the instruction pipeline (O) or output from the CPU32+ background debug mode (O).
	Instruction Pipe 1/ Row Address Select 1 Double-Drive	$\overline{\text{IPIPE1}}$/$\overline{\text{RAS1DD}}$	Used to track movement of words through the instruction pipeline (O) or a row address select 1 "double-drive" output (O).
	Breakpoint/Development Serial Clock	$\overline{\text{BKPT}}$/DSCLK	Signals a hardware breakpoint to the WC32P360 (Open-Drain I/O), or clock signal for CPU32+ background debug mode (O).
Clock and Test (cont'd.)	Freeze/Initial Configuration 2	FREEZE/CONFIG2	Indicates that the CPU32+ has acknowledged a breakpoint (O), or initial the controller configuration select (I).
	Three-State	$\overline{\text{TRIS}}$	Used to three-state all pins if the controller is configured as a master. Sampled during system reset (I).
	Test Clock	TCK	provides a clock Scan test logic. (I)
	Test Mode Select	TMS	Controls test mode operations. (I)
	Test Data In	TDI	Serial test instructions and test data signal. (I)
	Test Data Out	TDO	Serial test instructions and test data signal. (O)
	Test Reset	$\overline{\text{TRST}}$	Provides an asynchronous reset to the test controller. (I)
Power	Clock Synthesizer Power	V_{CCSYN}	Power supply to the PPL of the clock synthesizer.
	Clock Synthesizer Ground	GND_{SYN}	Ground supply to the PPL of the clock synthesizer.
	Clock Out Power	V_{CCCLK}	Power supply to clock out pins.
	Clock Out Ground	GND_{CLK}	Ground supply to clock out pins.
	Special Ground 1	GNDS1	Special ground for fast AC timing on certain system bus signals.
	Special Ground 2	GNDS2	Special ground for fast AC timing on certain system bus signals.
	System Power Supply	V_{CC}, GND	Power supply and return to the controller.
–	No Connect	NC4-NC1	Four no-connect pins.

NOTE: I denotes input, O denotes output, and I/O is input/output.

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage (1,2)	V_{CC}	-0.3 to +6.5	V
Input Voltage (1,2)	V_{IN}	-0.3 to +6.5	V
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

NOTES:
1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electric fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Rating
Thermal Resistance – Junction to Case 240-Pin QFP 241-Pin PGA	θ_{JC}	 2 7	°C/W
Thermal Resistance – Junction to Ambient 240-Pin QFP 241-Pin PGA	θ_{JA}	 22.4 22.8	°C/W

$T_J = T_A + (P_D \bullet \theta_{JA})$
$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$
where:
$P_{I/O}$ is the power dissipation on pins.

POWER CONSIDERATIONS

The average chip junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = P_{INT}+$P_{I/O}$

P_{INT} = I_{CC} x V_{CC}, Watts-Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins-User Determined

For most applications, $P_{I/O}<0.3*P_{INT}$ and can be neglected.

The following is an approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected):

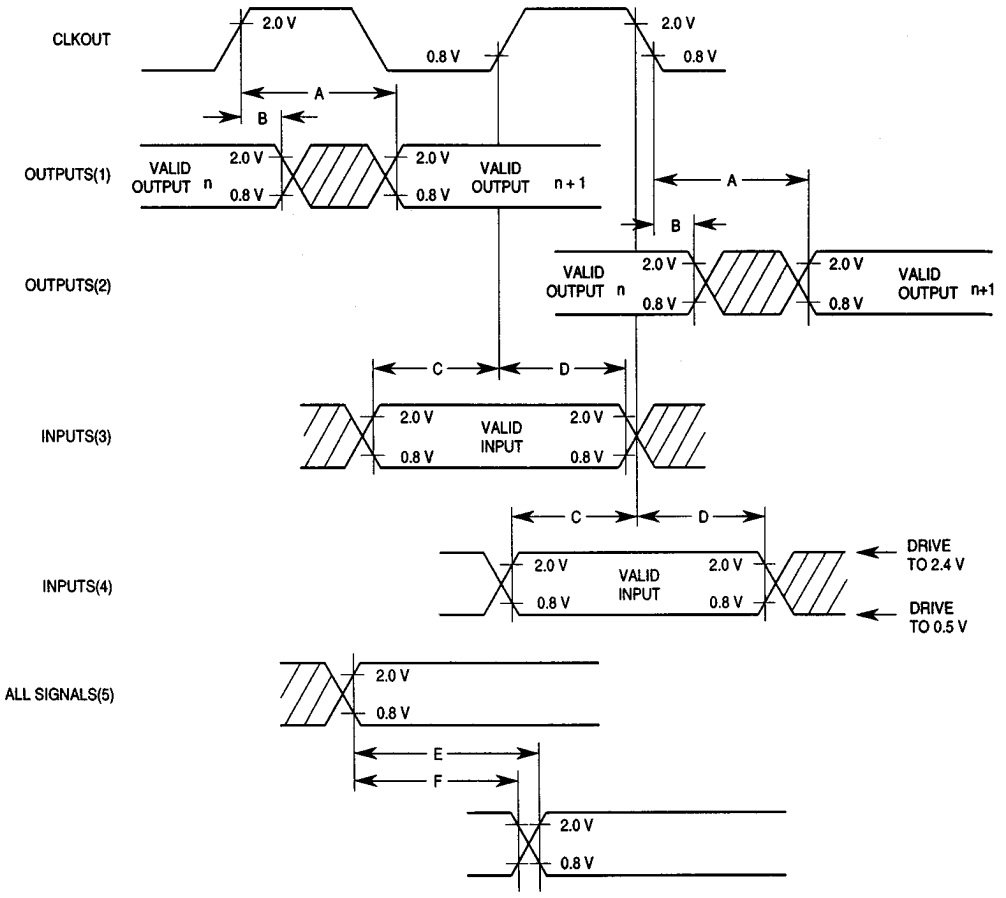
$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring PD (at thermal equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

FIG.5
DRIVE LEVELS AND TEST POINTS FOR AC SPECIFICATIONS



NOTE:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

DC ELECTRICAL SPECIFICATIONS

(V_{CC} = 0 V_{DC}, T_A = -55°C to +125°C)

Characteristics		Symbol	Min	Max	Unit
Input High Voltage (except EXTAL)		V_{IH}	2.0	Vcc	V
Input Low Voltage		V_{IL}	GND	0.8	V
EXTAL Input high Voltage		VIHC	0.8 x Vcc	Vcc + 0.3	V
Undershoot		–	–	-0.8	V
Input Leakage Current, V_{IN} = Vcc or GND	All Input Only Pins except for TMS, TDI and $\overline{TRST}$	I_{IN}	-2.5	2.5	µA
High-Z (Off State) Leakage Current, V_{IN} = 0.5/2.4V	All Noncrystal Outputs and I/O Pins	I_{OZ}	-20	20	µA
Signal Low Input Current, V_{IL} = 0.8V	TMS, TDI, $\overline{TRST}$	I_{IL}	-0.5	-0.5	mA
Signal High Input Current, V_{IH} = 2.0V	TMS, TDI, $\overline{TRST}$	I_{IH}	-0.5	-0.5	mA
Output High Voltage, I_{OH} = -0.8mA, Vcc = 4.75V	All Noncrystal Outputs except Open-Drain Pins	V_{OH}	2.4	–	V
Output Low Voltage		V_{OL}			V
I_{OL} = 2.0mA, CLKO1-2, FREEZE, $\overline{IPIPE0-1}$, $\overline{IFETCH}$, $\overline{BKPTO}$			–	0.5	
T_{OL} = 3.2mA, A31-A0, D31-D0, FC3-0, SIZ0-1, PA0,2,4,6,8-15, PB0-5, PB8-17, PC0-11, TDO, $\overline{PERR}$, PRTY0-3, $\overline{IOUT0-2}$, $\overline{AVECO}$, $\overline{AS}$, $\overline{CAS3-0}$, $\overline{BLCRO}$, $\overline{RAS0-7}$			–	0.5	
T_{OL} = 5.3mA, $\overline{DSACK0-1}$, R/$\overline{W}$, $\overline{DS}$, $\overline{OE}$, $\overline{RMC}$, $\overline{BG}$, $\overline{BGACK}$, $\overline{BERR}$			–	0.5	
T_{OL} = 7mATXD1-4			–	0.5	
I_{OL} = 8.9mAPB6, PB7, $\overline{HALT}$, $\overline{RESET}$, $\overline{BR}$ (Output)			–	0.5	
Input Capacitance	All I/O Pins	C_{IN}	–	20	pF
Load Capacitance	except CLKO1-2	C_L	–	100	pF
Power, 5V version		Vcc	4.75	5.25	V
Minimum Vcc Ramp up time on power on reset		^tRANP	4	–	ms

AC POWER DISSIPATIONS

Mode of Operation	Symbol	System Clock Frequency	BRGCLK Clock Frequency	SyncCLK Clock Frequency	Typ	Unit
Normal Mode	I_{DD}	25MHz	25MHz	25MHz	250	mA
Low Power Mode	I_{DDSB}	Divided by 2 12.5MHz	Divided by 16 1.56MHz	Divided by 2 12.5MHz	150	mA
Low Power Mode	I_{DDSB}	Divided by 4 6.25MHz	Divided by 16 1.56MHz	Divided by 4 6.25MHz	85	mA
Low Power Mode	I_{DDSB}	Divided by 16 1.56MHz	Divided by 16 1.56MHz	Divided by 4 6.25MHz	35	mA
Low Power Mode	I_{DDSB}	Divided by 256 97.6KHz	Divided by 16 1.56MHz	Divided by 4 6.25MHz	20	mA
Low Power Mode	I_{DDSB}	Divided by 256 97.6KHz	Divided by 64 390KHz	Divided by 64 390KHz	13	mA
Low Power stop V_{CO} Off (1)	I_{DDSP}				0.5	mA
PLL Supply Current						
PLL Disabled	I_{DDPD}				TBD	
PLL Enabled	I_{DDPE}				TBD	

NOTES:

1. EXTAL frequency is 32KHz
   All measurements were taken with only CLKO1 enabled, V_{CC} = 5.0V, V_{IL} = 0V and V_{IH} = V_{CC}

MAXIMUM POWER DISSIPATION

System Frequency	Vcc	Max P_D	Unit
25MHz	5.25V	1.80	W

AC ELECTRICAL SPECIFICATIONS CONTROL TIMING

(GND = 0 VDC, TA = -55°C to +125°C)

Characteristic	Symbol	Specification	25 MHz		Unit
			Min	Max	
System Frequency		f_{sys}	dc (1)	25.00	MHz
Crystal Frequency		f_{XTAL}	25	6000	KHz
On-Chip VCO System Frequency		f_{sys}	20	50	MHz
Sart-up Time with external clock (oscillator disabled) or after changing the multiplication factor MF.		t_{pll}		2500	CLKS
CLKO1-2 Stability		ΔCLK	TBD	TBD	%
CLKO1 Period	1	t_{cyc}	40	–	ns
XETAL Duty Cycle, MF	1A	t_{dcyc}	40	60	ns
External Clock Input Period	1C	t_{EXTcyc}	40	–	ns
CLKO1 Pulse Width (Measured at 1.5V)	2, 3	t_{CW1}	19	–	ns
CLKO2 Pulse Width (Measured at 1.5V)	2A, 3A	t_{CW2}	9.5	–	ns
CLKO1 Rise and Fall Times (Full Drive)	4, 5	t_{crf1}	–	2	ns
CLKO2 Rise and Fall Times (Full Drive)	4A, 5A	t_{crf2}	–	2	ns
EXTAL to CLKO1 Skew – PLL Enabled (MF<5)	5B	t_{EXTP1}		a	ns
EXTAL to CLKO2 Skew – PLL Enabled (MF<5)	5C	t_{EXTP2}		a	ns
CLKO1 to CLKO2 Skew	5D	t_{CSKW}		a	ns

NOTE 1: Note that the minimum VCO frequency and the PLL default values put some restrictions on the minimum system frequency.

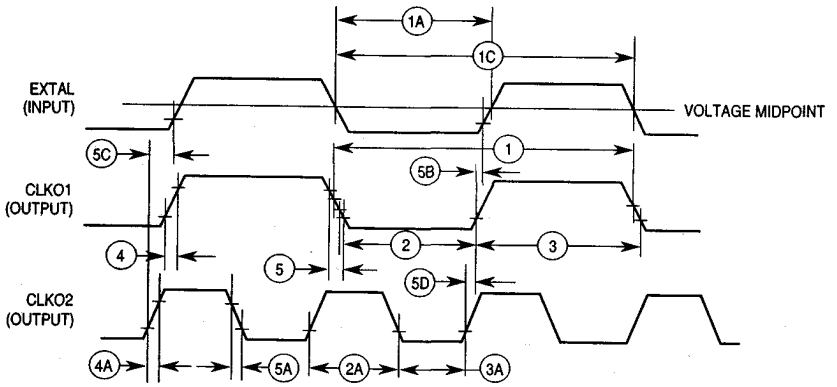
a: The following calculation should be used to determine the actual value for specifications 5B, 5C and 5D.

5B: +/- (0.9ns + 0.25 x (rise time)) (1.4ns @ rise = 2ns; 1.9ns @ rise = 4ns)

5C: +/- (2ns + 0.25 x (rise time)) (2.5ns @ rise = 2ns; 3ns @ rise = 4ns)

5D: +/- (3ns + 0.5 x (rise time)) (4ns @ rise = 2ns; 5ns @ rise = 4ns)

FIG.6
CLOCK TIMING



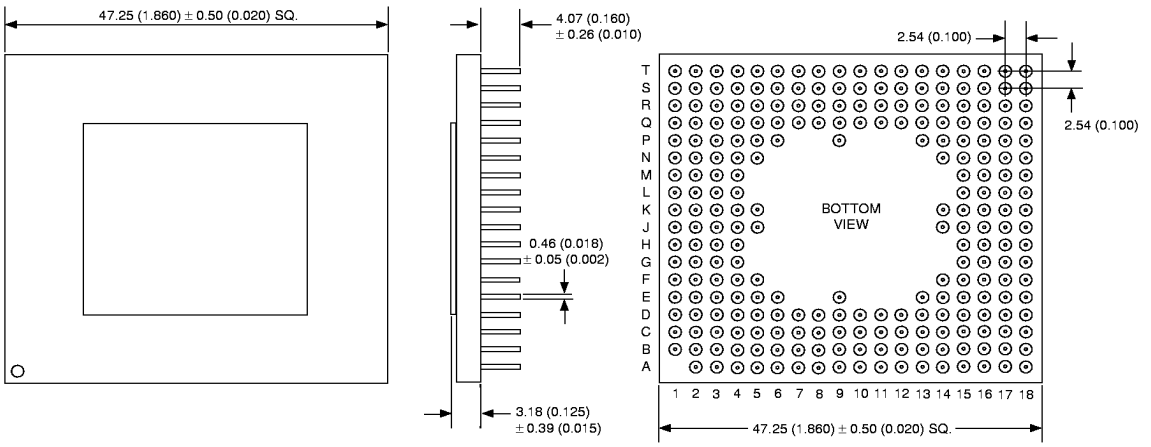
EXTERNAL CAPACITOR FOR PLL

Characteristic	Symbol	5.0V		Unit
		Max	Min	
PLL external capacitor (XFC to V_{CCSYN})	C_{XFC}			
MF<5 (recommended value MF x 400 pF)		MFX340	MFX480	pF
MF>4 (recommended value MF x 540 pF)		MFX380	MFX970	pF

EXAMPLES:

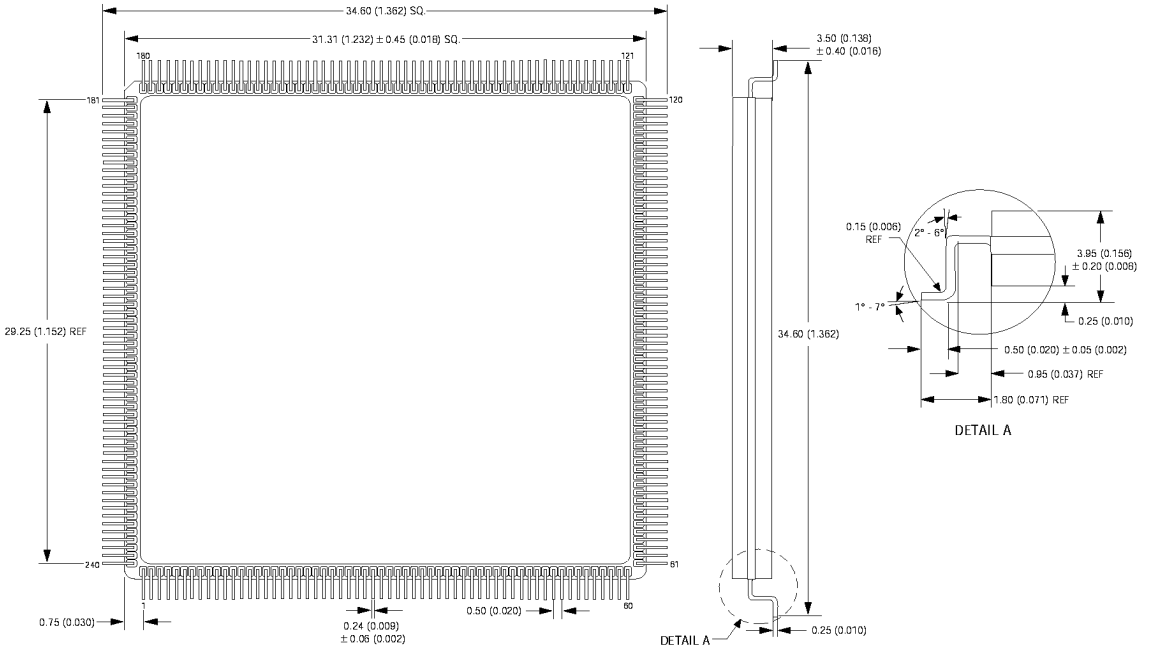
1. MODCK1pin = 0, MF = 1 ⇒ C_{XFC} = 400 pF
2. MODCK1 pin = 1, crystal is 32.768KHz (or 4.192MHz), initial MF = 401, initial frequency = 13.14MHz, later on MF is changed to 762 to support a frequency of 25MHz.
   Minimum C_{XFC} is: 762 x 380 = 289nF, maximum C_{XFC} is: 401 x 970 = 390nF. The recommended C_{XFC} for 25MHz is: 762 x 540 = 414nF.
   289nF < C_{XFC} < 390nF and closer to 414nF. The proper available value for C_{XFC} 390nF.
3. MODCK1 pin = 1, crystal is 32.768KHz (or 4.192MHz), initial MF = 401, initial frequency = 13.14MHz, later on MF is changed to 1017 to support a frequency of 33.34MHz.
   Minimum C_{XFC} is: 1017 x 380 = 386nF, maximum C_{XFC} is: 401 x 970 = 390nF ⇒ 386nF < C_{XFC} < 390nF.
   The proper value for C_{XFC} is 390nF.
4. In order to to get higher range, higher crystal frequency can be used (i.e. 50KHz), in this case:
   Minimum C_{XFC} is: 667 x 380 = 253nF, maximum C_{XFC} is: 401 x 970 = 390nF ⇒ 253nF < C_{XFC} < 390nF.

FIG. 7 241 PIN GRID ARRAY, PGA (P3)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

FIG. 8 240 PIN, CERAMIC QUAD FLAT PACK, CQFP (Q3)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION