TFT LCD Approval Specification

MODEL NO.:V315H1-PH2

Customer: _____

Approved by: _____

Note:

Approved By	TV Product Marketing & Management Div.
	Chao-Chun Chung

Reviewed By	QRA Dept.	Product Development Div.
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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 2.0	Nov.10, 2009	All	All	Approval Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V315H1-PH2 is a 31.5" TFT Liquid Crystal Display module. This module supports 1920* 1080 HDTV format and can display 1.07G colors (8-bit+Hi-FRC/color).

1.2 CHARACTERISTICS

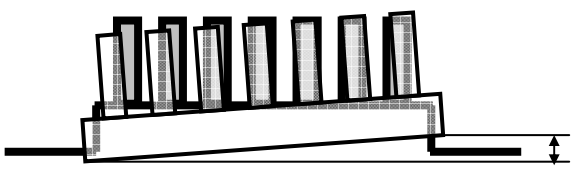
CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	31.51
Pixels [lines]	1920*1080
Active Area [mm]	698.4 (H) x 392.85 (V) (31.51" diagonal)
Sub -Pixel Pitch [mm]	0.12125 (H) x 0.36375 (V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	1200
Physical Size [mm]	716.1(W) x 410(H) x 1.79(D) Typ.
Display Mode	Transmissive mode / Normally black
Contrast Ratio	4000:1 Typ. (Typical value measured at CMO's module)
Glass thickness (Array/CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H),+88/-88(V) Typ. (Typical value measured at CMO's module)
Color Chromaticity	R=(0.638, 0.323) G=(0.288, 0.605) B=(0.146, 0.055) W=(0.280, 0.290) (Typical value measured at CMO's module)
Cell Transparency [%]	4.0%Typ.. (Typical value measured at CMO's module)
Polarizer (CF side)	Super Wide View **Glare & Hard coating (3H)** 709.7(W) x 405(H)..
Polarizer (TFT side)	Super Wide View, 709.7(W) x 405(H)..

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	1099	1199	1299	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ±0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

(2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT (BASED ON CMO MODULE V546H1-PH3)

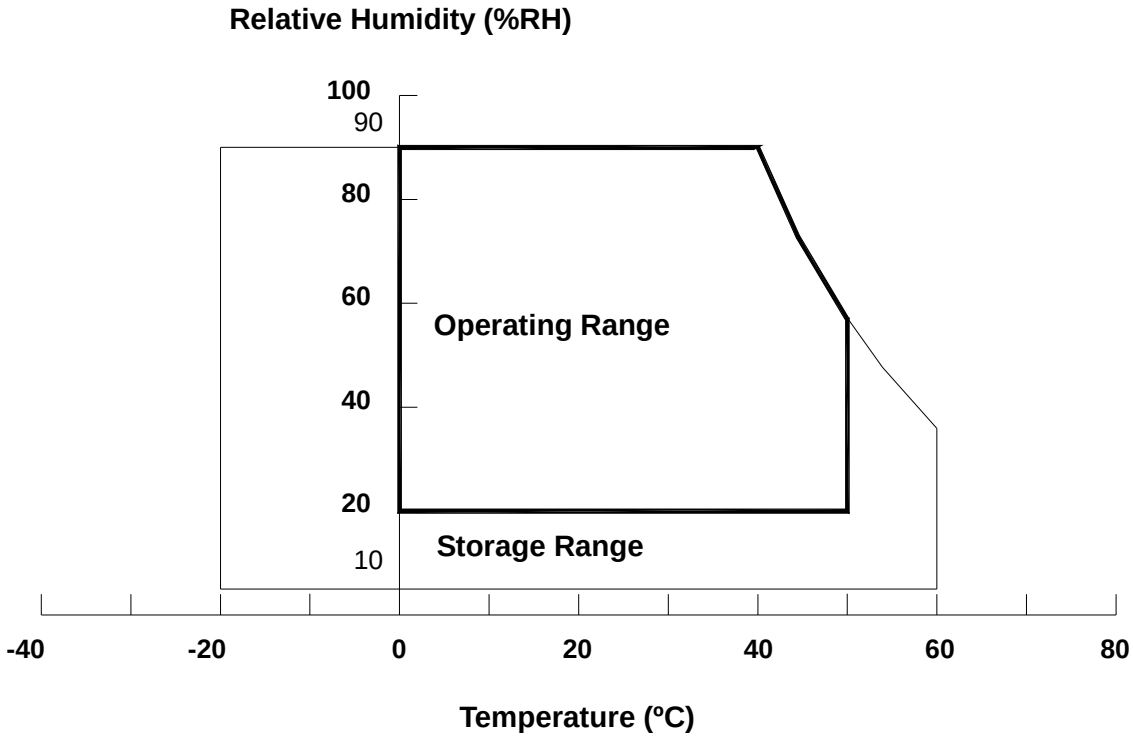
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1), (3)
Operating Ambient Temperature	T_{OP}	0	50	ºC	(1), (2), (3)
Altitude Operating	A_{OP}	0	5000	M	(3)
Altitude Storage	A_{ST}	0	12000	M	(3)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation..



Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) The rating of environment is base on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.

2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

Storage Condition : With shipping package.

Storage temperature range : 25±5 ℃

Storage humidity range : 50±10%RH

Shelf life : a month

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 ELECTRICAL ABSOLUTE RATINGS

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

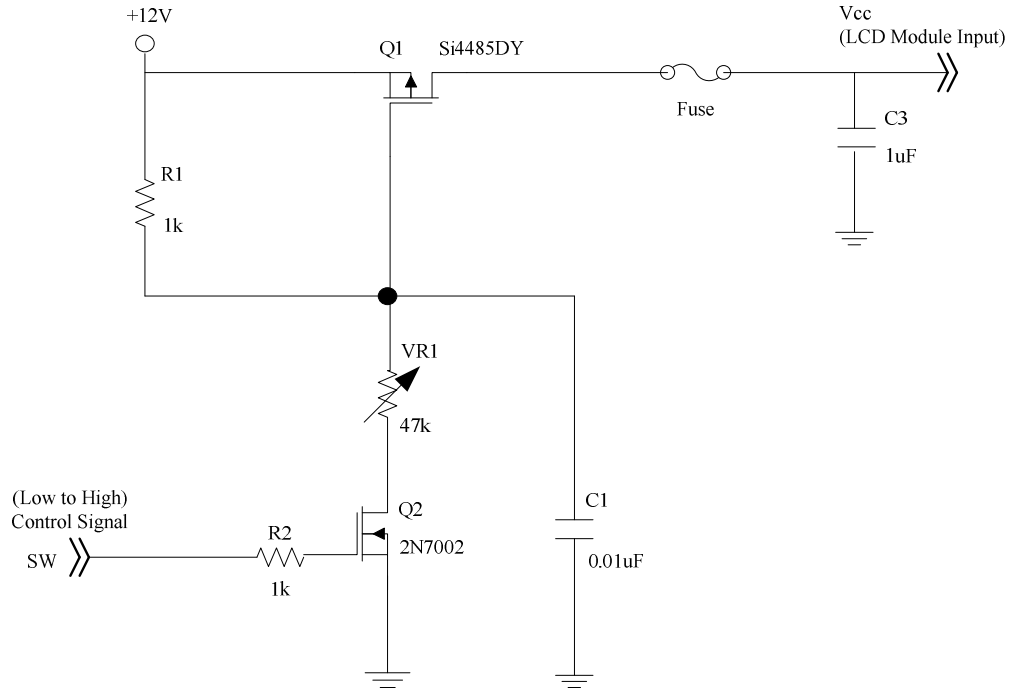
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

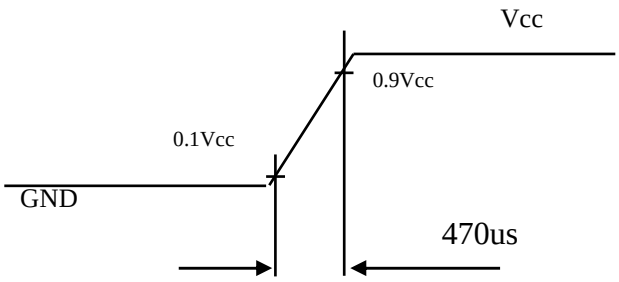
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	5	A	(2)
Power Supply Current	White Pattern	-	-	1	-	A	(3)
	Horizontal Stripe	-	-	1	1.3	A	
	Black Pattern	-	-	0.5	-	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.

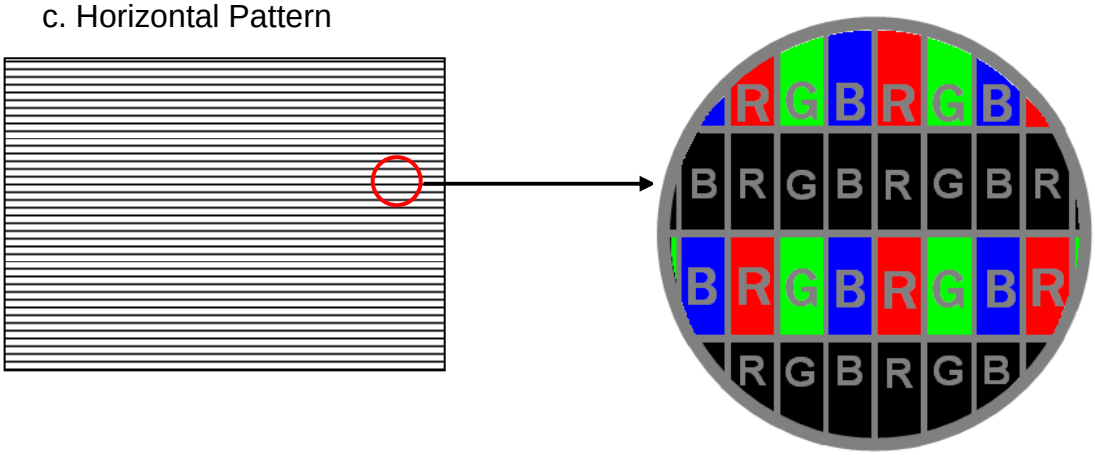
a. White Pattern

Active Area

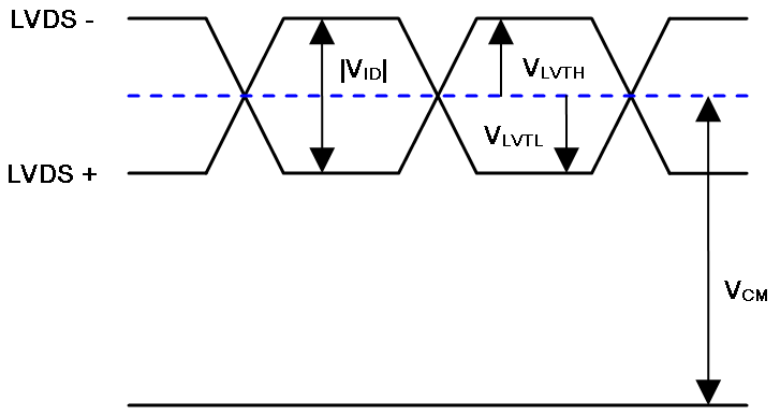
b. Black Pattern

Active Area

c. Horizontal Pattern

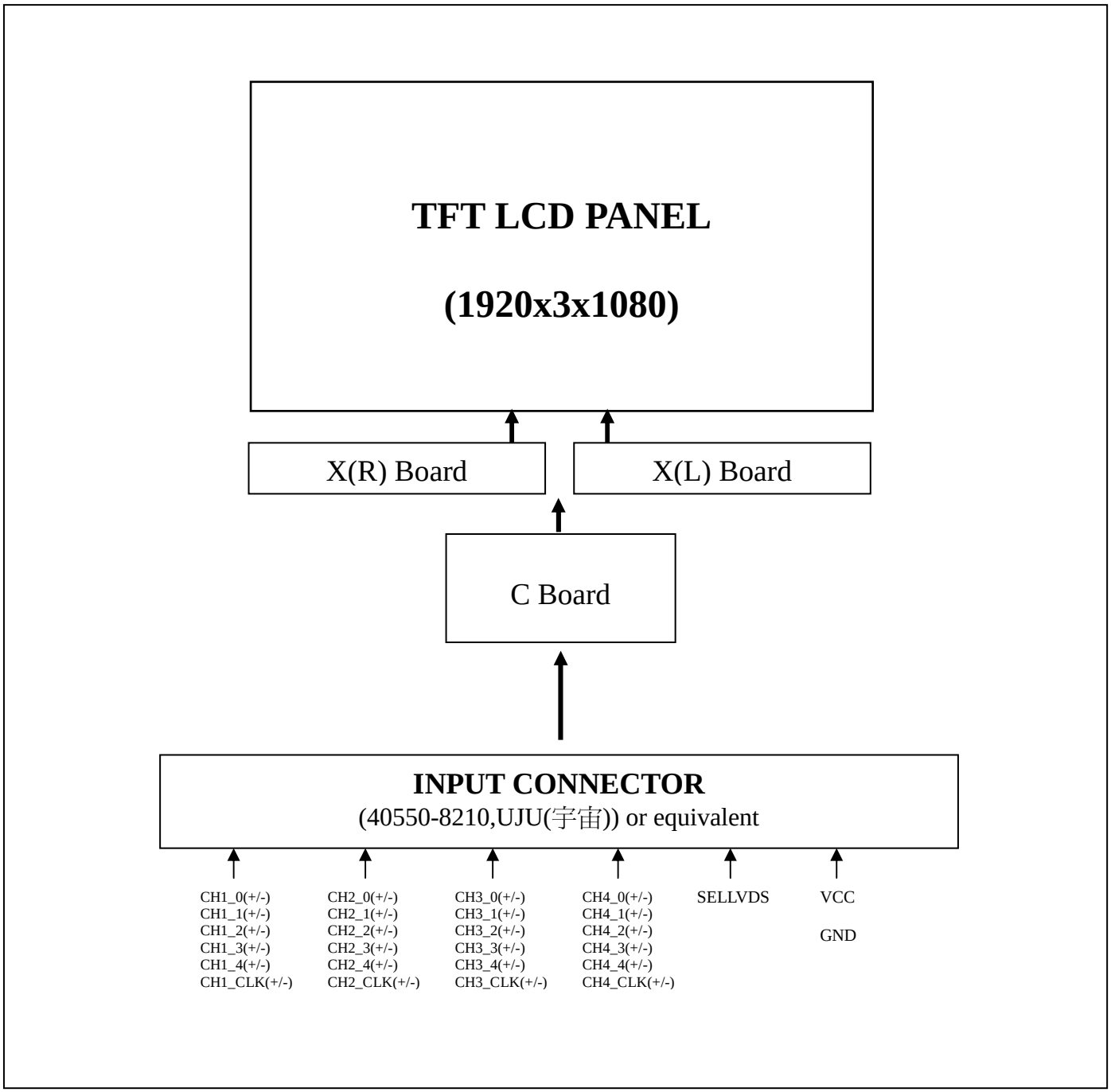


Note (4) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM

4.1 TFT LCD OPEN CELL



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF1 Connector Pin Assignment (40550-8210,UJU(宇宙) or equivalent)

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	N.C.	No Connection	(1)
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	
11	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
12	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
13	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
14	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
15	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH1CLK-	First pixel Negative LVDS differential clock input.	
18	CH1CLK+	First pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	
21	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
22	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
23	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	
26	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
27	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
28	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	

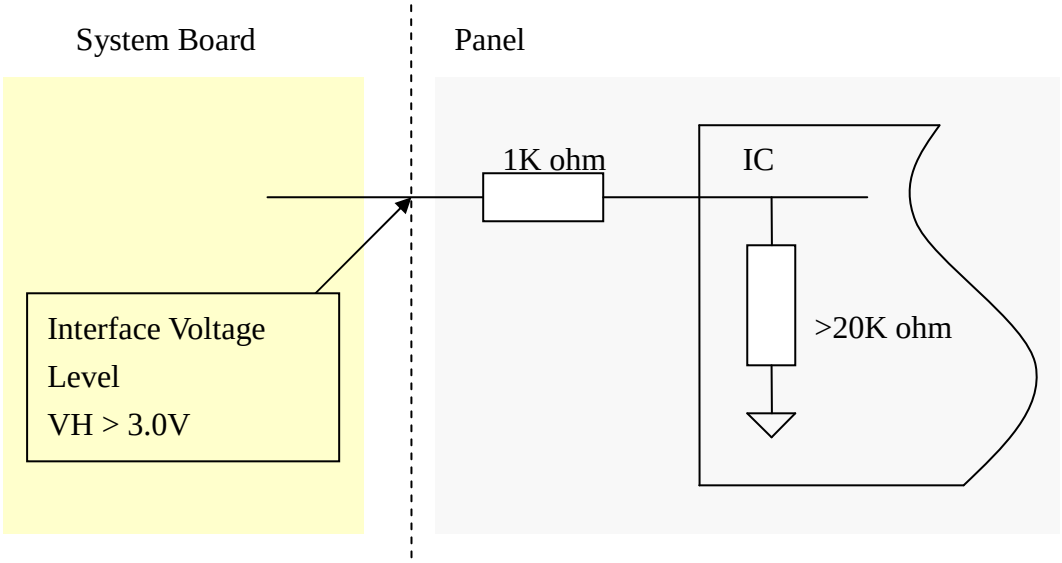
29	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
30	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
31	GND	Ground	
32	CH3CLK-	Third pixel Negative LVDS differential clock input.	
33	CH3CLK+	Third pixel Positive LVDS differential clock input.	
34	GND	Ground	
35	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	
36	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
37	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
38	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
39	GND	Ground	
40	SCL	I2C Bus	
41	N.C.	No Connection	(1)
42	N.C.	No Connection	(1)
43	WP	Write Protection for EEPROM	
44	SDA	I2C Bus	
45	LVDS_SEL	LVDS Data Format Selection	(2)
46	N.C.	No Connection	(1)
47	N.C.	No Connection	(1)
48	N.C.	No Connection	(1)
49	N.C.	No Connection	(1)
50	N.C.	No Connection	(1)
51	N.C.	No Connection	(1)
52	GND	Ground	
53	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
54	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	
55	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
56	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	
57	GND	Ground	
58	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
59	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	
60	GND	Ground	

61	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
62	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	
63	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
64	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
65	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
66	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	
67	GND	Ground	
68	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
69	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
70	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
71	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	
72	GND	Ground	
73	CH2CLK+	Second pixel Positive LVDS differential clock input.	
74	CH2CLK-	Second pixel Negative LVDS differential clock input.	
75	GND	Ground	
76	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
77	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
78	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
79	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
80	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
81	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	
82	GND	Ground	

Note (1) Reserved for internal use. Please leave it open.

Note (2) High=connect to +3.3V or Open : VESA Format ； Low= connect to GND : JEIDA Format.

Note (3) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement as below.



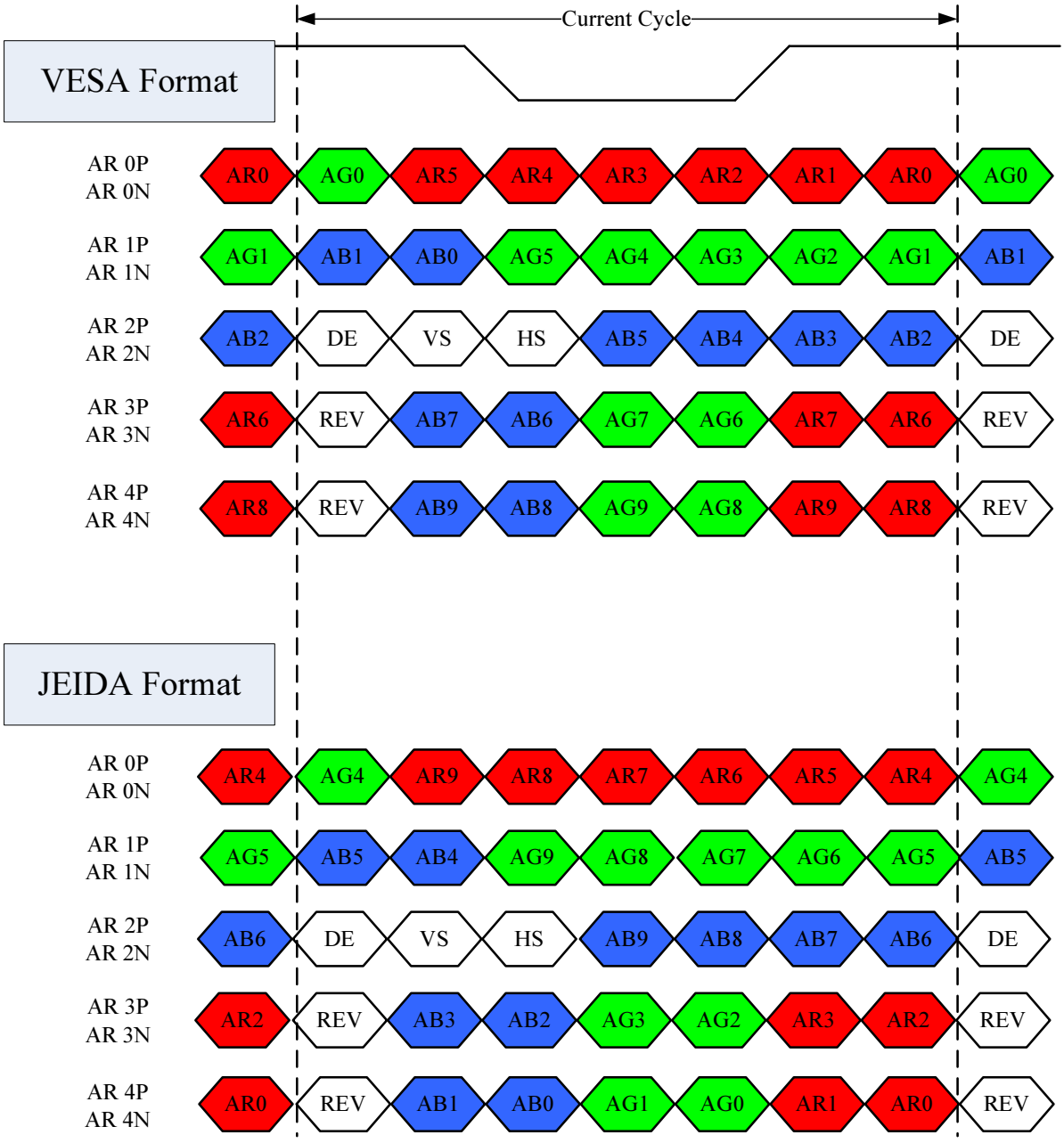
Note (4) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, ……1913, 1917
2nd Port	Second Pixel	2, 6, 10, ….1914, 1918
3rd Port	Third Pixel	3, 7, 11, ….1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ….1916, 1920

5.2 LVDS INTERFACE

VESA Format : SELLVDS = H or Open

JEIDA Format : SELLVDS = L



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSV : Reserved

5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
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	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(5)
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	97	100	103	Hz	(6)
		F_{r6}	117	120	123	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	—
	Blank	Tvb	35	45	55	Th	—
Horizontal Active Display Term	Total	Th	540	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	—
	Blank	Thb	60	70	95	Tc	—

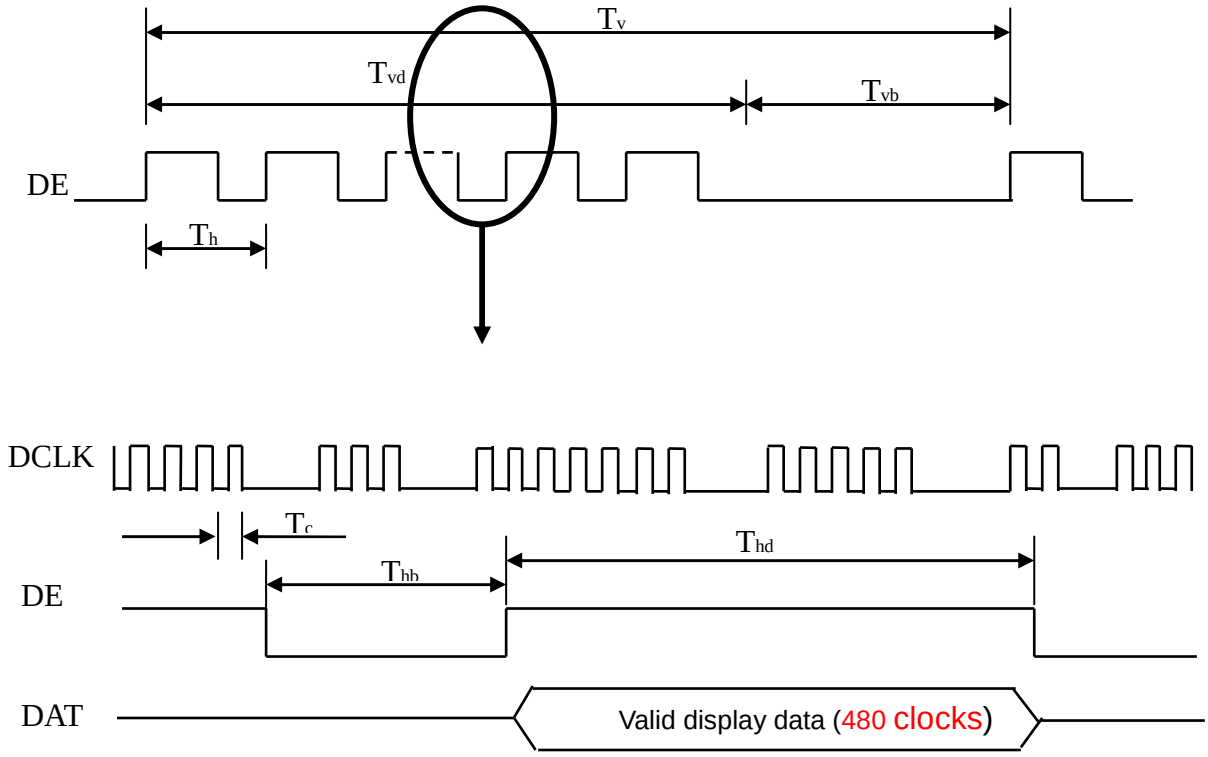
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

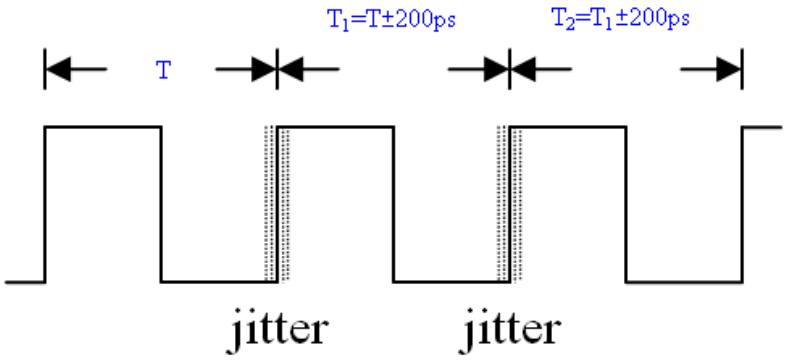
$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

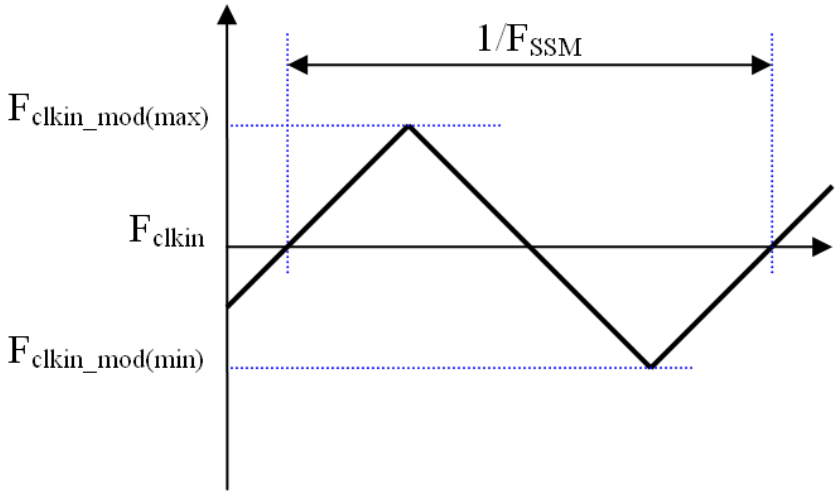
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

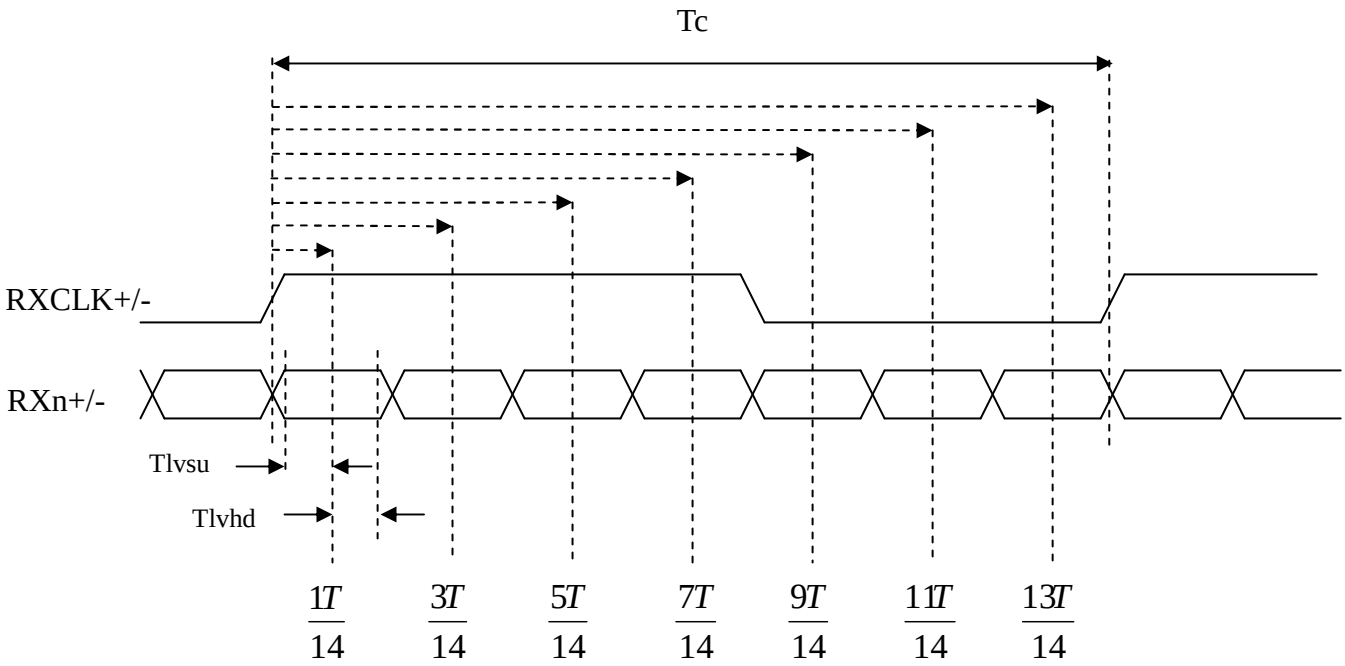


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM

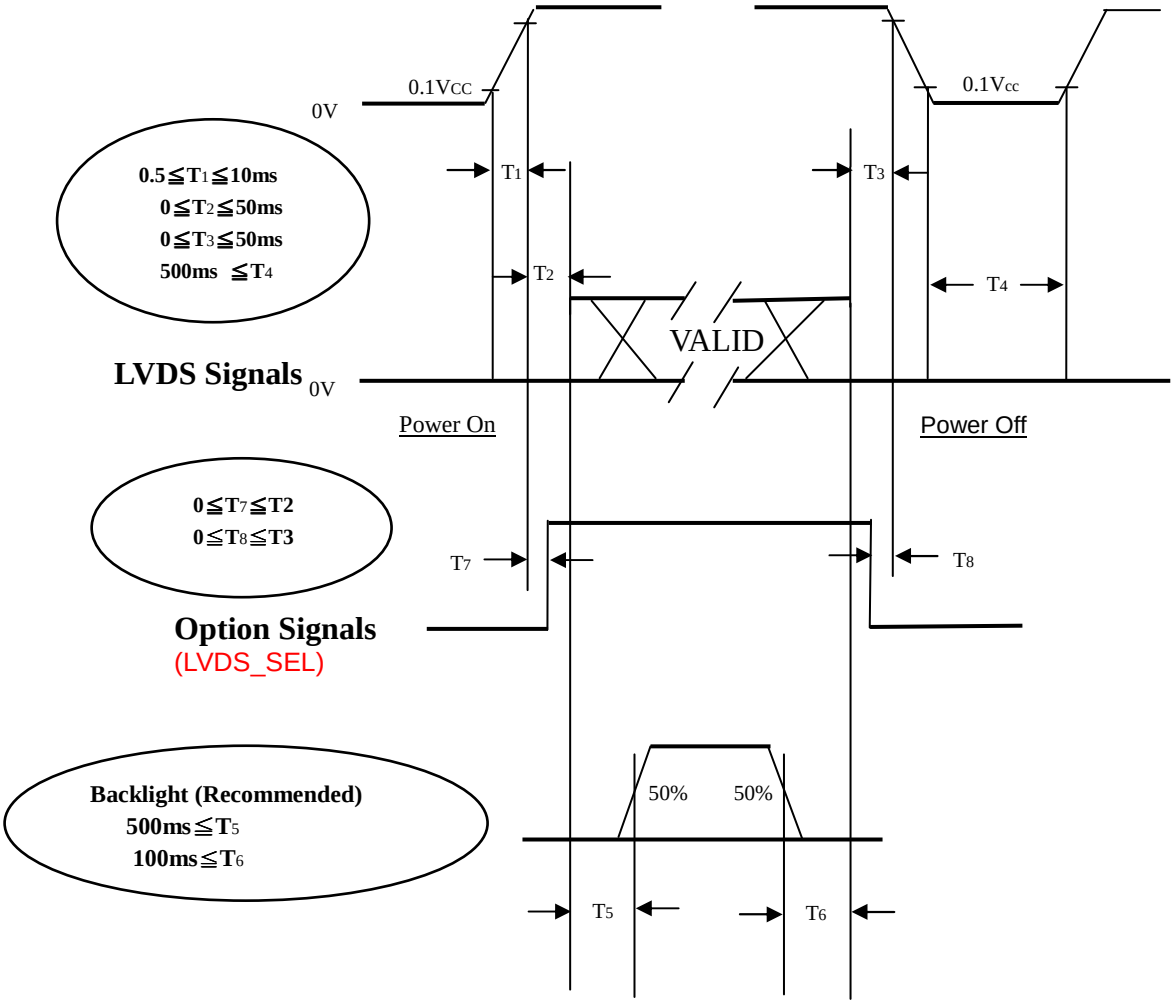


Note (6) : (ODSEL) = H/L or open for 100/120Hz frame rate. Please refer to 5.1 for detail information

6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	12.5±0.5	mA
Inverter Driving Frequency	F_L	58±3	KHz

7.2 OPTICAL SPECIFICATIONS

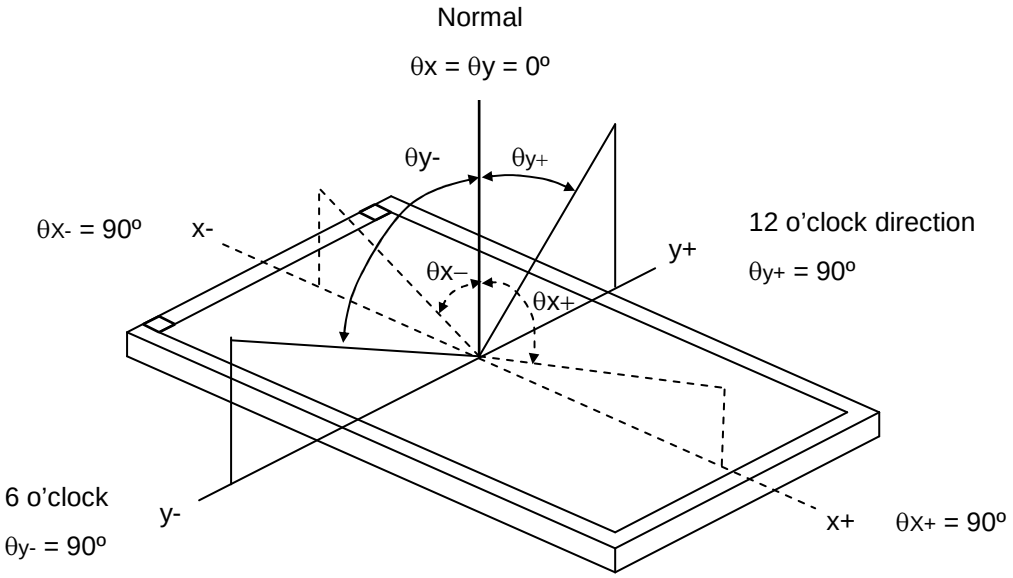
The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rx	θ_x=0°, θ_Y =0° Viewing angle at normal direction With CMO module	Typ.-0.03	(0.638)	Typ+0.03	-	(1),(5)
		Ry			(0.323)		-	
	Green	Gx			(0.288)		-	
		Gy			(0.605)		-	
	Blue	Bx			(0.146)		-	
		By			(0.055)		-	
	White	Wx			(0.280)		-	
		Wy			(0.290)		-	
Center Transmittance		T%	θ_x=0°, θ_Y =0° With CMO Module	-	4.0		%	(1), (7)
Contrast Ratio		CR		3000	4000		-	(1), (3)
Response Time		Gray to gray average	θ_x=0°, θ_Y =0° With CMO Module@120Hz	-	4.5	9	ms	(4)
White Variation		δW	θ_x=0°, θ_Y =0° With CMO Module			1.3	-	(1), (6)
Crosstalk		CT				4	%	(1), (8)
Viewing Angle	Horizontal	θ_x+	CR≥20 With CMO Module	80	88	-	Deg.	(1), (2)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

Note (1) Light source is CMO's V315H1-L01 BLU and driving voltages are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by EZ-Contrast 160R (Eldim)



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

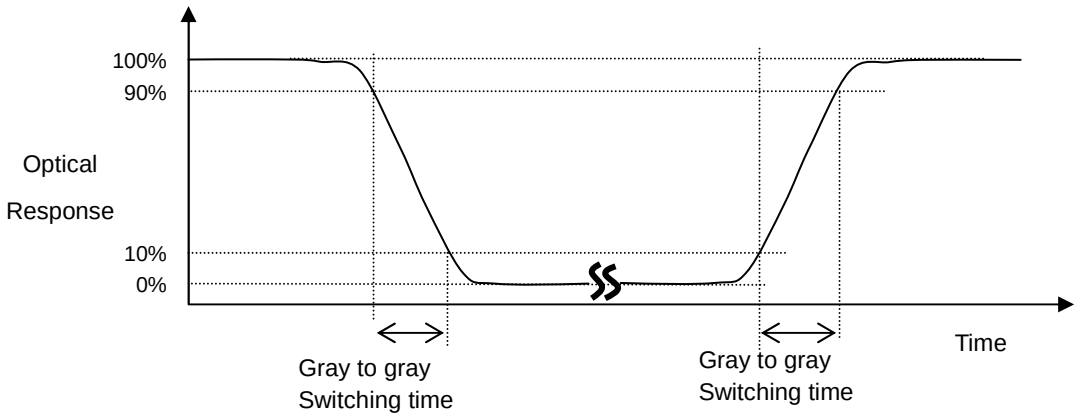
Contrast Ratio (CR) = L1023 / L0

L1023: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5) ,where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (4) Definition of Gray-to-Gray Switching Time:

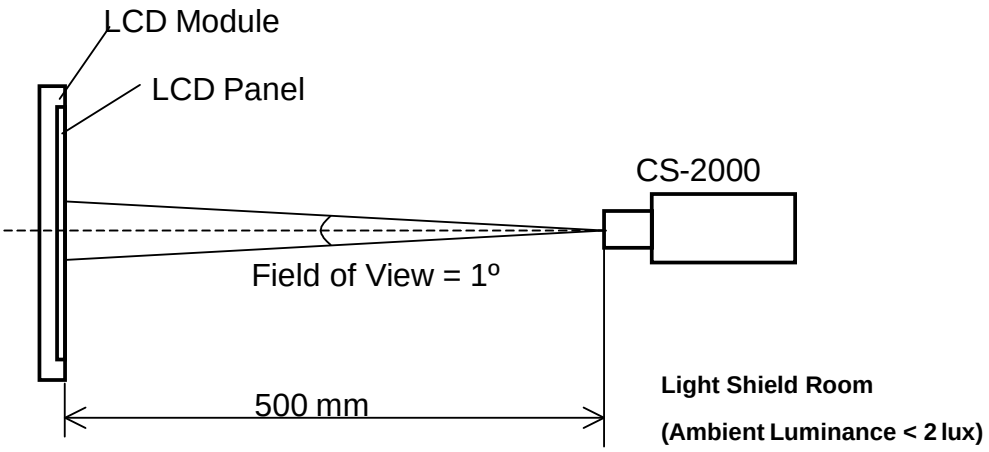


The driving signal means the signal of gray 0, 127, 255, 383,511, 639,767, 895, and 1023

Gray to gray average time means the average switching time of gray 0, 127, 255, 383,511, 639,767, 895, and 1023 to each other.

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 60 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 60 minutes in a windless room.

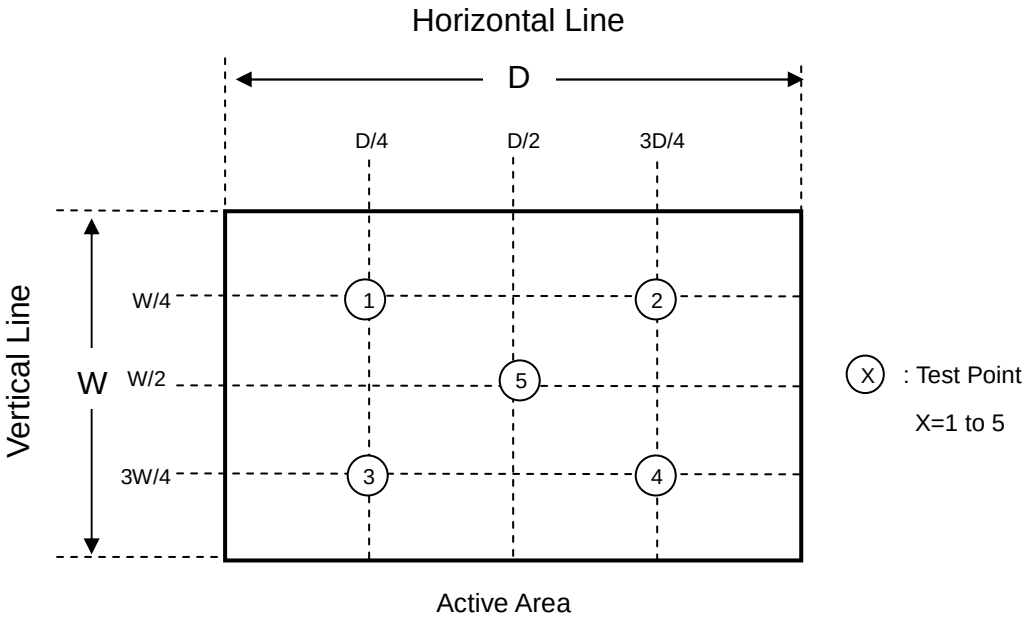


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

where L (X) is corresponding to the luminance of the point X at the figure below.



Note (7) Definition of Transmittance(T%):

Module with signal input gray 1023, BLU film structure is DP and Diffuser

$$\text{Transmittance} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}} * 100\%$$

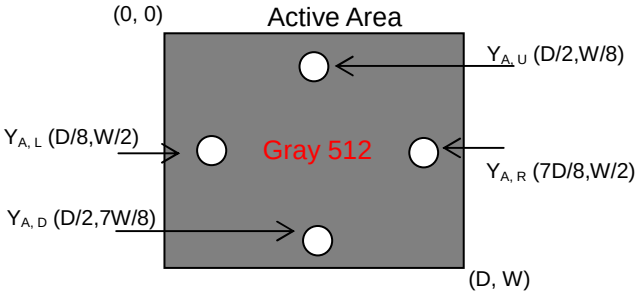
Note (8) Definition of Cross Talk (CT):

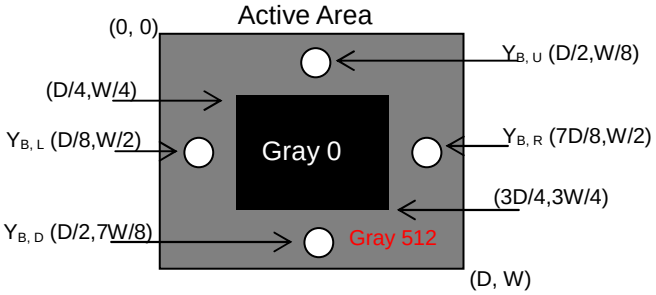
$CT = | Y_B – Y_A | / Y_A \times 100\ (\%)$

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



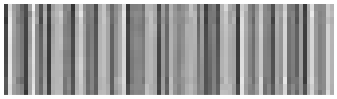


8. DEFINITION OF LABELS

8.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMO internal control.

V315H1-PH2



XXXXXXXXXXXXX

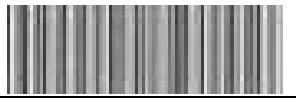
8.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation

P.O. NO._____

Parts ID._____

Carton ID._____ Quantities 21



XXXXXXXXXXXXX

Made in Taiwan

(a) Model Name: V315H1– PH2

(b) Carton ID: CMO internal control

(c) Quantities:21

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 21 LCD TV Panels / 1 Box

(2) Box dimensions : 970 (L) X 640 (W) X 319 (H)

(3) Weight : approximately 38Kg (21 panels per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

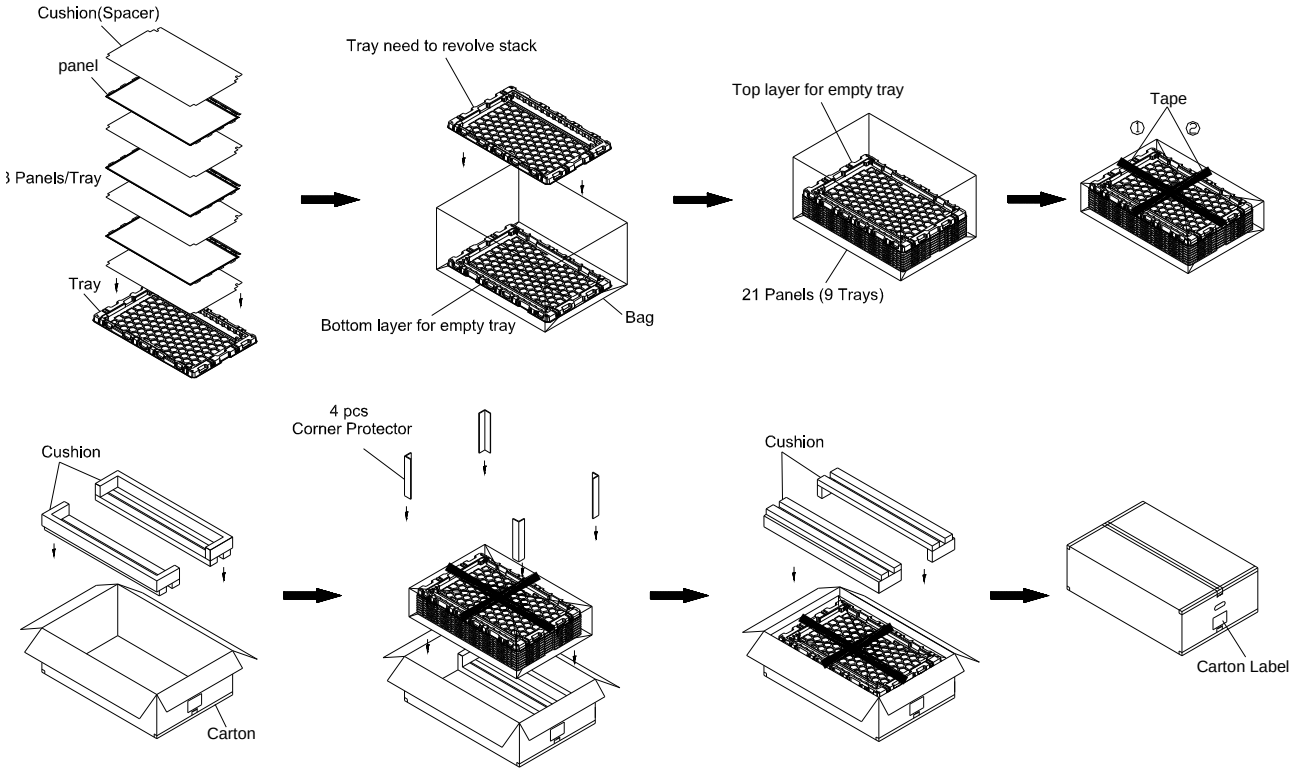
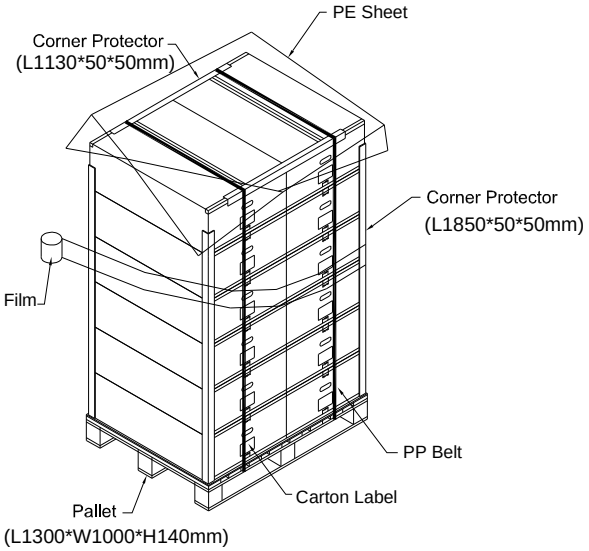


Figure.9-1 packing method

Sea & Land Transportation
Gross : 471kg



Air Transportation
Gross : 319kg

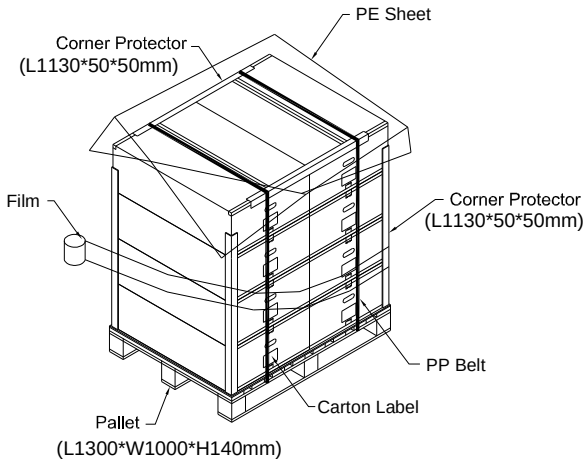


Figure.9-2 packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the product during assembly.

(2) To assemble backlight or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel will be damaged.

(4) Always follow the correct power sequence when the product is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(7) It is dangerous that moisture come into or contacted the product, because moisture may damage the product when it is operating.

(8) High temperature or humidity may reduce the performance of module. Please store this product within the specified storage conditions.

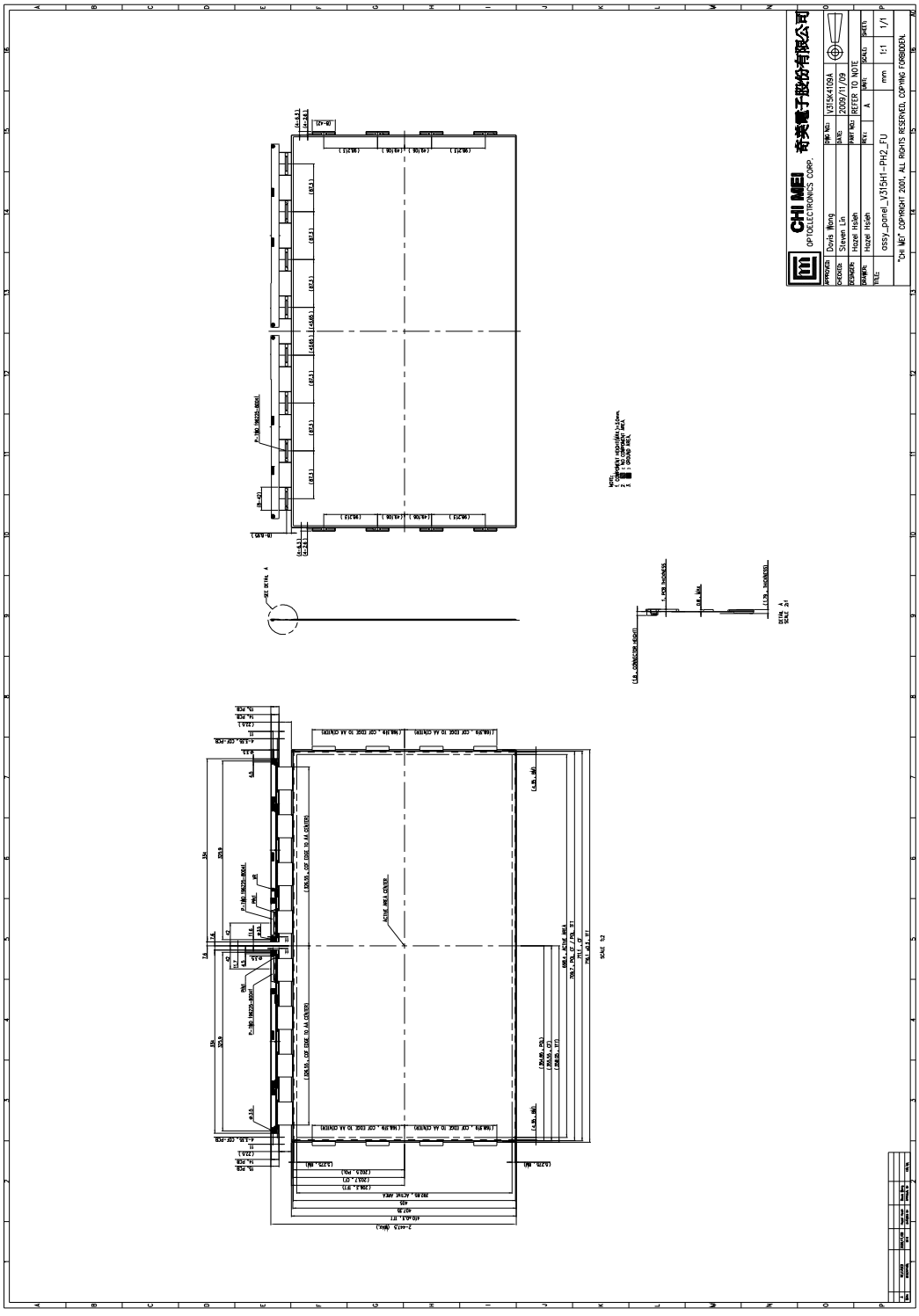
(9) When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly.

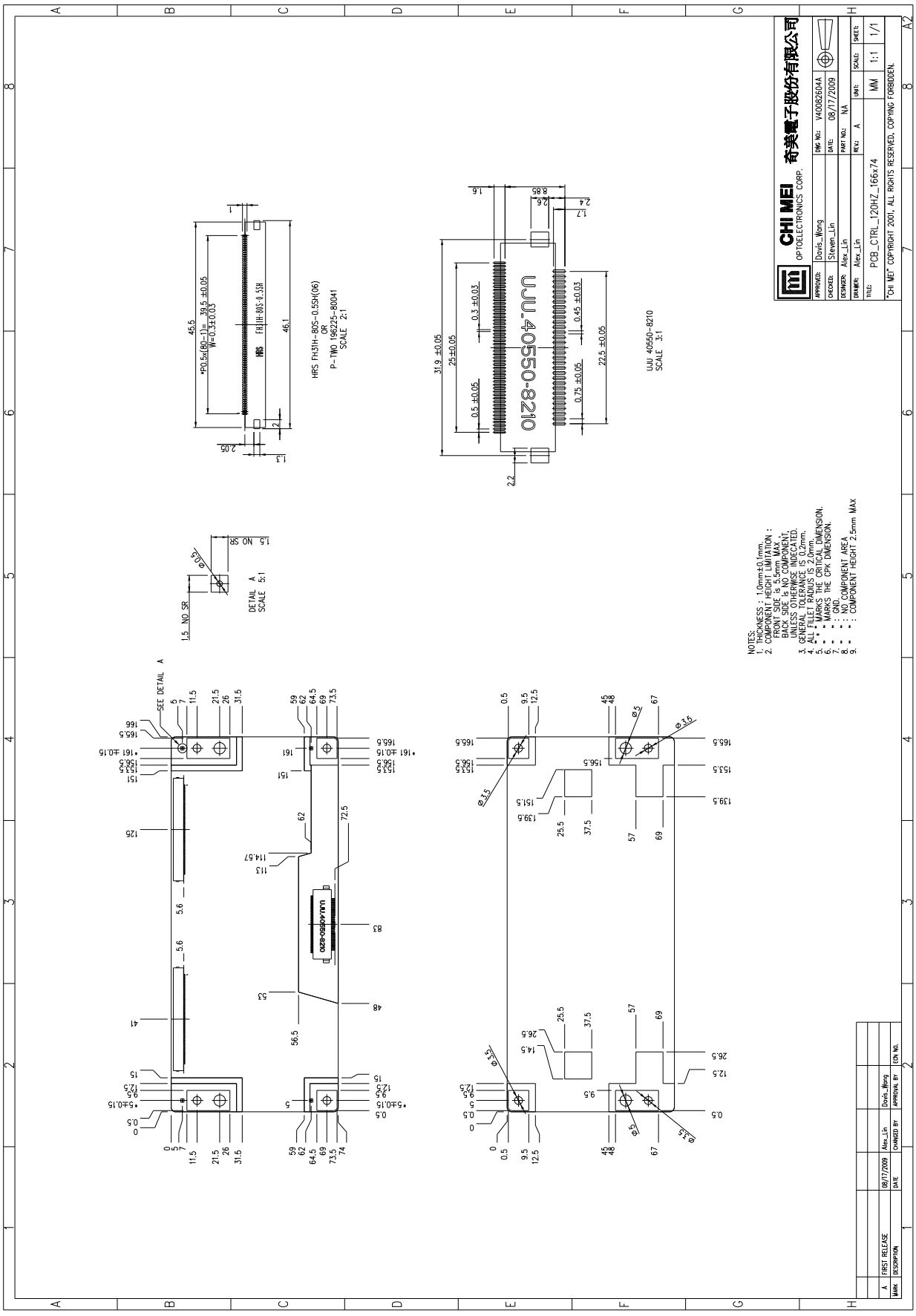
10.2 SAFETY PRECAUTIONS

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the product's end of life, it is not harmful in case of normal operation and storage.

11. Mechanical Drawing

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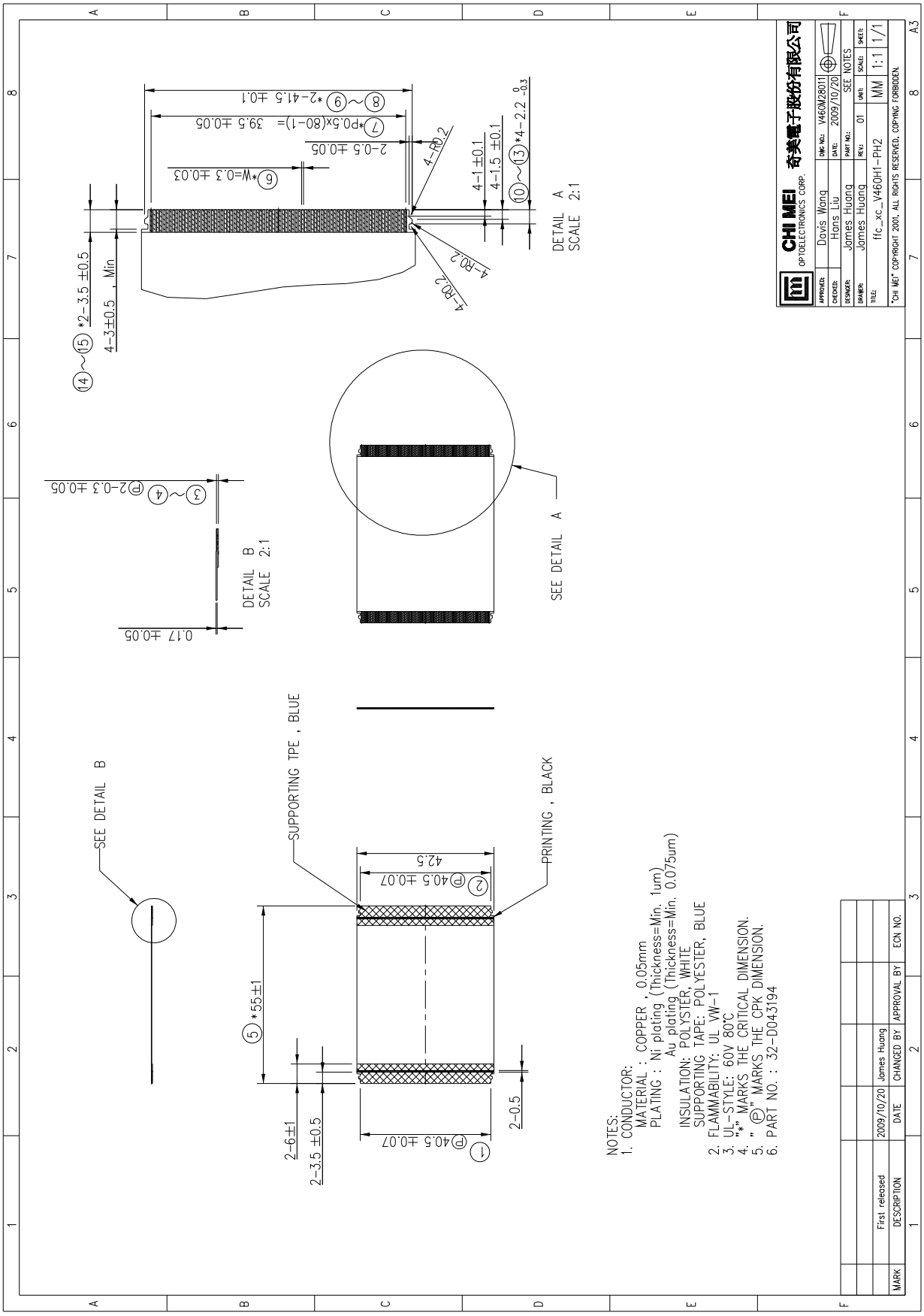
奇美電子股份有限公司
PCB_CTRL_120HZ_166x74
"CHI MEI" COPYRIGHT 2001, ALL RIGHTS RESERVED, COPYING FORBIDDEN.
HRS FH31H-80S-0.5SH(06)
P-TWO 196225-80041
SCALE 2:1
UJU 40550-8210
SCALE 3:1
DETAIL A
SCALE 5:1
NOTES:
1. THICKNESS : 1.0mm±0.1mm
2. COMPONENT HEIGHT LIMITATION :
FRONT SIDE is 5mm MAX.,
BACK SIDE is NO COMPONENT,
UNLESS OTHERWISE INDECATED.
3. GENERAL TOLERANCE IS ±0.2mm.
4. ALL FILLET RADIUS IS 2.0mm.
5. ▪ ▪ ▪ MARKS THE CRITICAL DIMENSION.
6. ▪ ▪ ▪ MARKS THE CPK DIMENSION.
7. ▪ ▪ ▪ : GND.
8. ▪ ▪ ▪ : NO COMPONENT AREA
9. ▪ ▪ ▪ : COMPONENT HEIGHT 2.5mm MAX


DETAIL A
SCALE 2:1
DETAIL B
SCALE 2:1
SEE DETAIL A
SEE DETAIL B
SUPPORTING TPE , BLUE
PRINTING , BLACK
NOTES:
1. CONDUCTOR:
MATERIAL : COPPER , 0.05mm
PLATING : Ni plating (Thickness=Min. 1um)
Au plating (Thickness=Min. 0.075um)
INSULATION: POLYSTER, WHITE
SUPPORTING TAPE: POLYESTER, BLUE
2. FLAMMABILITY: UL VW-1
3. UL-STYLE: 60V 80°C
4. "*" MARKS THE CRITICAL DIMENSION.
5. " Ⓟ " MARKS THE CPK DIMENSION.
6. PART NO. : 32-D043194
CHI MEI OPTOELECTRONICS CORP.
奇美電子股份有限公司
APPROVED: Davis Wang
CHECKED: Hans Liu
DESIGNED: James Huang
DRAWN: James Huang
TITLE: ffc_xc_V460H1-PH2
DWG NO.: V460M28011
DATE: 2009/10/20
PART NO.: SEE NOTES
REV: 01
UNIT: MM
SCALED: 1:1
SHEET: 1/1
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First released 2009/10/20 James Huang