NEC
NEC Electronics Inc.

μPD75036 Family (μPD75028/036/P036) 4-Bit, General-Purpose Microcontrollers With A/D Converter

March 1994

Description

The μPD75036 family of high-performance 4-bit single-chip CMOS microcontrollers includes the following devices:

μPD75028 μPD75036 μPD75P036

The 75036 family features an A/D converter and 48 I/O lines. The instruction set operates on 1-, 4-, and 8-bit data

Timing is generated by two oscillators. The main oscillator normally drives the CPU and all peripherals. The 32.768-kHz subsystem oscillator provides time keeping when the main oscillator is turned off. Since CMOS power dissipation is proportional to clock rate, the 75036 provides a software selectable instruction cycle time from 0.95 μs to 122 μs. The STOP and HALT modes turn off parts of the microcontroller for additional power savings. The data retention mode retains RAM contents down to 2.0 V.

Features

- Eight-channel, 8-bit A/D converter
- Subsystem oscillator allows watch timer to operate in power-down modes
- 8-bit synchronized serial interface
  - Full-duplex, three-wire mode
  - Half-duplex, two-wire mode
  - NEC serial bus interface (SBI) mode
- Timers: four channels
  - Watch (clock) timer: 0.5-sec. interrupt request
  - 8-bit timer/event counter
  - 8-bit interval timer
  - 16-bit multifunction timer that can be used as an 8-bit timer, 8-bit PWM output, 16-bit free-running timer, or 16-bit counter for an integrating A/D converter
- 48 I/O lines
  - 12 input-only lines
  - 24 bidirectional I/O lines
  - Twelve 10-V n-channel, open-drain I/O lines that can directly drive LEDs
  - 27 software selectable I/O pullup resistors
  - 4 software selectable I/O pulldown resistors
  - 12 mask selectable resistors (ROM versions only)
- Bit-sequential buffer
  - 16-bit, bit addressable memory
- Standard 75X instruction set
  - 107 instructions
  - Bit manipulation
  - 4- and 8-bit transfer instructions
- Minimum instruction execution times
  - 0.95, 1.91, and 15.3 μs using 4.19-MHz main system clock
  - 122 μs selectable using 32.768-kHz subsystem clock
- Eight 4-bit registers
  - Usable as four 8-bit registers
- Memory-mapped on-chip peripherals
  - Special function registers
- Vectored interrupt controller
  - 12 external and 5 internal interrupt sources
  - 12 edge-detection inputs
  - 6 vectored interrupts
- Power saving and battery backup
  - Variable CPU clock rate; 3.2 mA typical at 5 V 4.19 MHz
  - HALT mode stops CPU; 0.5 mA typical current drain
  - STOP mode stops oscillator; 0.5 μA typical power drain
- CMOS operation
  - ROM versions; V_{DD} from 2.7 to 6.0 V
  - 75P036 (low voltage OTP); V_{DD} from 2.7 to 6.0 V

Internal High-Capacity ROM and RAM

	75028	75036	75P036
ROM	8064 bytes	16,256 bytes	—
PROM	—	—	16,256 bytes
RAM	512 nibbles	1024 nibbles	1024 nibbles

50200

Ordering Information

Part Number (See notes)	Package (Dwg)	ROM
μPD75028CW-xxx	64-pin plastic shrink DIP (P64C-70-750A, C)	Mask
GC-xxx-AB8	64-pin plastic QFP (P64GC-80-AB8-3)	
μPD75036CW-xxx	64-pin plastic shrink DIP (P64C-70-750A, C)	Mask
GC-xxx-AB8	64-pin plastic QFP (P646C-80-AB8-3)	
μPD75P036CW	64-pin plastic shrink DIP (P64C-70-750A, C)	OTP
GC-AB8	64-pin plastic QFP (P64GC-80-AB8-3)	

Notes:

(1) Engineering samples are supplied in either a 64-pin ceramic shrink dip (CW) or a 64-pin ceramic QFP (GC) package.

(2) xxx indicates ROM code suffix.

(3) All parts are standard quality grade.

Pin Configurations

64-Pin Shrink DIP

μPD75028, 75036, 75P036

SB1/SI/P0$_3$	1	64	V_{SS}
SB0/SO/P0$_2$	2	63	P3$_0$(MD0) †
$\overline{SCK}$/P0$_1$	3	62	P3$_1$(MD1) †
INT4/P0$_0$	4	61	P3$_2$(MD2) †
BUZ/P2$_3$	5	60	P3$_3$(MD3) †
PCL/P2$_2$	6	59	P4$_0$
PPO/P2$_1$	7	58	P4$_1$
PTO$_0$/P2$_0$	8	57	P4$_2$
$\overline{MAT}$/P10$_3$	9	56	P4$_3$
$\overline{MAZ}$/P10$_2$	10	55	P5$_0$
$\overline{MAI}$/P10$_1$	11	54	P5$_1$
$\overline{MAR}$/P10$_0$	12	53	P5$_2$
$\overline{RESET}$	13	52	P5$_3$
X1	14	51	P6$_0$/KR0
X2	15	50	P6$_1$/KR1
* IC (V_{PP})	16	49	P6$_2$/KR2
XT1	17	48	P6$_3$/KR3
XT2	18	47	P7$_0$/KR4
V_{DD}	19	46	P7$_1$/KR5
AV_{DD}	20	45	P7$_2$/KR6
AV_{REF+}	21	44	P7$_3$/KR7
AV_{REF-}	22	43	P8$_0$
AN7	23	42	P8$_1$
AN6	24	41	P8$_2$
AN5	25	40	P8$_3$
AN4	26	39	P9$_0$
AN3/P11$_3$	27	38	P9$_1$
AN2/P11$_2$	28	37	P9$_2$
AN1/P11$_1$	29	36	P9$_3$
AN0/P11$_0$	30	35	P1$_0$/INT0
AV_{SS}	31	34	P1$_1$/INT1
TI0/P1$_3$	32	33	P1$_2$/INT2

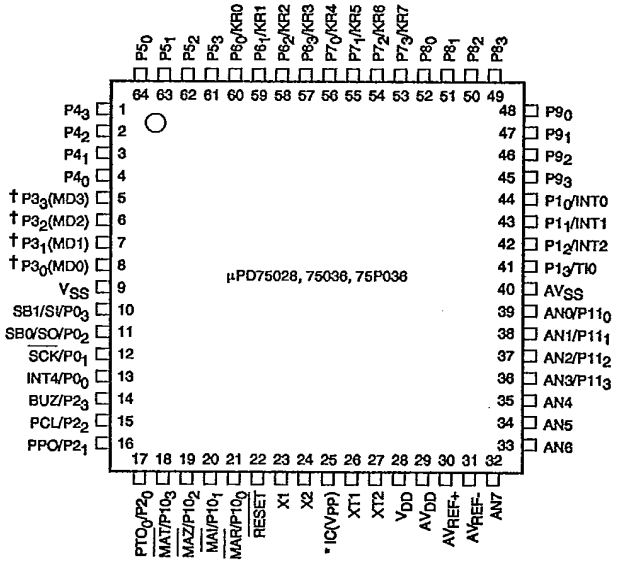
* IC Should be connected to V_{DD}. Used as V_{PP} programming pin in μPD75P036.

† MD0-MD3 are used as the programming mode selection pins on the μPD75P036 during OTP programming and verification.

83RD-8622A (12/94)

Pin Configurations (cont)

64-Pin QFP



* IC Should be connected to V_{DD}. Used as V_{PP} programming pin in μPD75P036.

† MD0-MD3 are used as the programming mode selection pins on the μPD75P036 during OTP programming and verification.

83RD-66238 (2/94)

Pin Identification

Symbol	Function
AN4-AN7	Inputs for A/D converter
AV_{DD}	A/D converter positive power supply
AV_{SS}	A/D converter ground
AV_{REF+} AV_{REF-}	A/D converter reference voltages
IC (V_{PP})	Internally connected (V_{PP} for μPD75P036)
$P0_0$/INT4	Port 0 input; interrupt 4
$P0_1$/$\overline{SCK}$	Port 0 input; serial clock
$P0_2$/SO/SB0	Port 0 input; serial out; serial bus interface 0
$P0_3$/SI/SB1	Port 0 input; serial in; serial bus interface 1
$P1_0$/INT0	Port 1 input; interrupt 0
$P1_1$/INT1	Port 1 input; interrupt 1
$P1_2$/INT2	Port 1 input; interrupt 2
$P1_3$/TI0	Port 1 input; timer 0 input
$P2_0$/PTO_0	Port 2 I/O; timer/event counter output
$P2_1$/PPO	Port 2 I/O; multifunction timer output
$P2_2$/PCL	Port 2 I/O; programmable clock output
$P2_3$/BUZ	Port 2 I/O; buzzer output
$P3_0$-$P3_3$	Port 3 I/O; μPD75P036 mode selection
$P4_0$-$P4_3$	Port 4 I/O
$P5_0$-$P5_3$	Port 5 I/O
$P6_0$/KR0	Port 6 I/O; key scan input 0
$P6_1$/KR1	Port 6 I/O; key scan input 1
$P6_2$/KR2	Port 6 I/O; key scan input 2
$P6_3$/KR3	Port 6 I/O; key scan input 3
$P7_0$/KR4	Port 7 I/O; key scan input 4
$P7_1$/KR5	Port 7 I/O; key scan input 5
$P7_2$/KR6	Port 7 I/O; key scan input 6
$P7_3$/KR7	Port 7 I/O; key scan input 7
$P8_0$-$P8_3$	Port 8 I/O
$P9_0$-$P9_3$	Port 9 I/O
$P10_0$/$\overline{MAR}$	Port 10 I/O; multifunction timer A/D converter reverse integration output
$P10_1$/$\overline{MAI}$	Port 10 I/O; multifunction timer A/D converter integration output
$P10_2$/$\overline{MAZ}$	Port 10 I/O; multifunction timer A/D converter autozero output
$P10_3$/$\overline{MAT}$	Port 10 I/O; multifunction timer A/D converter termination input
$P11_0$/AN0	Port 11 input; A/D converter input 0
$P11_1$/AN1	Port 11 input; A/D converter input 1
$P11_2$/AN2	Port 11 input; A/D converter input 2
$P11_3$/AN3	Port 11 input; A/D converter input 3
$\overline{RESET}$	Reset input
X1, X2	Main clock inputs
XT1, XT2	Subsystem clock inputs
V_{DD}	Positive power supply
V_{SS}	Ground

PIN FUNCTIONS

$P0_0$/INT4, $P0_1$/$\overline{SCK}$, $P0_2$/SO/SB0, $P0_3$/SI/SB1. These pins can be used as 4-bit input port 0. Or, $P0_0$ can also be used for vectored interrupt 4, which interrupts on either the leading edge or the trailing edge of the signal. $P0_1$-$P0_3$ may also be used for the serial interface in the SBI or two- or three-wire mode. SI is the serial input, SO is the serial output, and $\overline{SCK}$ is the serial clock. Reset causes these pins to default to the port 0 input mode.

$P1_0$/INT0, $P1_1$/INT1, $P1_2$/INT2, $P1_3$/TI0. These pins can be used as 4-bit input port 1. Or, $P1_0$ and $P1_1$ can also be used for edge-triggered interrupts INT0 and INT1. $P1_2$ can be used for INT2, which is also an edge-triggered input, but one that generates an interrupt request and does not cause an interrupt. $P1_3$ can be used as an input clock to the timer/event counter to count external events. Reset causes these pins to default to the port 1 input mode.

$P2_0$/PTO_0, $P2_1$/PPO, $P2_2$/PCL, $P2_3$/BUZ. These pins can be used as 4-bit I/O port 2. When used as an output the data is latched. When used as an input port, the port outputs are three-state. $P2_0$ can also be used as the output of the timer/event counter flip-flop (TOUT); $P2_1$ can also be used as the output of the multifunction timer/event counter MFT flip-flop; $P2_2$ can be used as the output (PCL) for the clock generator; and $P2_3$ can be used to output square waves for a buzzer. Reset causes these pins to default to the port 2 input mode.

$P3_0$-$P3_3$. These pins are used for I/O port 3. Each bit in this port can be independently programmed to be either an input or an output. This port has latched outputs, and can directly drive LEDs. A reset signal causes this port to default to the input mode.

$P4_0$-$P4_3$, $P5_0$-$P5_3$. Ports 4 and 5 are identical 4-bit I/O ports that can be combined to function as a single 8-bit port. Latched outputs will directly drive LEDs. Outputs are n-channel, open-drain that can withstand up to 10 volts; pullup resistor mask options are available for

these ports in the μPD75028 and μPD75036 only. A reset signal causes these ports to default to the input mode.

$P6_0$/KR0, $P6_1$/KR1, $P6_2$/KR2, $P6_3$/KR3, $P7_0$/KR4, $P7_1$/KR5, $P7_2$/KR6, $P7_3$/KR7. Ports 6 and 7 are 4-bit I/O ports with latched outputs that can be combined to function as one 8-bit port. Each pin of port 6 can be independently programmed to be either an input or an output, while port 7 can be programmed to be either all inputs or all outputs. Alternately, these pins may be used to detect the falling edge of inputs KR0-KR3 (port 6) and KR4-KR7 (port 7). A reset signal causes these ports to default to the input mode.

$P8_0$-$P8_3$, $P9_0$-$P9_3$. Ports 8 and 9 are identical 4-bit I/O ports. Outputs are latched. A reset signal causes these ports to default to the input mode.

$P10_0$/$\overline{MAR}$, $P10_1$/$\overline{MAI}$, $P10_2$/$\overline{MAZ}$, $P10_3$/$\overline{MAT}$. These pins are used for I/O port 10. Outputs are n-channel, open-drain that can withstand up to 10 volts. The outputs are latched and can directly drive an LED. Pullup resistor mask option is available for this port for the μPD75028 and μPD75036 only. $P10_0$-$P10_2$ can also be used as the $\overline{MAR}$, $\overline{MAI}$, and $\overline{MAZ}$ outputs from the multifunction timer/event counter's A/D control logic. $P10_3$ can be used as the input $\overline{MAT}$ to the multifunction timer/event counter's A/D control logic. A reset signal causes this port to default to the input mode.

$P11_0$/AN0, $P11_1$/AN1, $P11_2$/AN2, $P11_3$/AN3. These pins are used for input port 11, or can alternately be used as A/D converter inputs AN0-AN3. A reset signal causes this port to default to the input mode.

AN4-AN7. A/D converter inputs.

AV_{DD}. A/D converter positive power supply.

AV_{SS}. A/D converter analog ground.

AV_{REF+}, AV_{REF-}. A/D converter positive and negative reference voltages.

IC/V_{PP}. This pin should be connected to V_{DD} when using the μPD75028 or μPD75036. For the μPD75P036, this pin is used as the programming voltage input during the EPROM write/verify cycles. When the device is not being programmed, this pin should be tied to V_{DD}.

X1, X2. These pins are the main system clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

XT1, XT2. These pins are the subsystem clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

$\overline{RESET}$. Active-low reset input.

V_{DD}. System positive power supply.

V_{SS}. System ground.

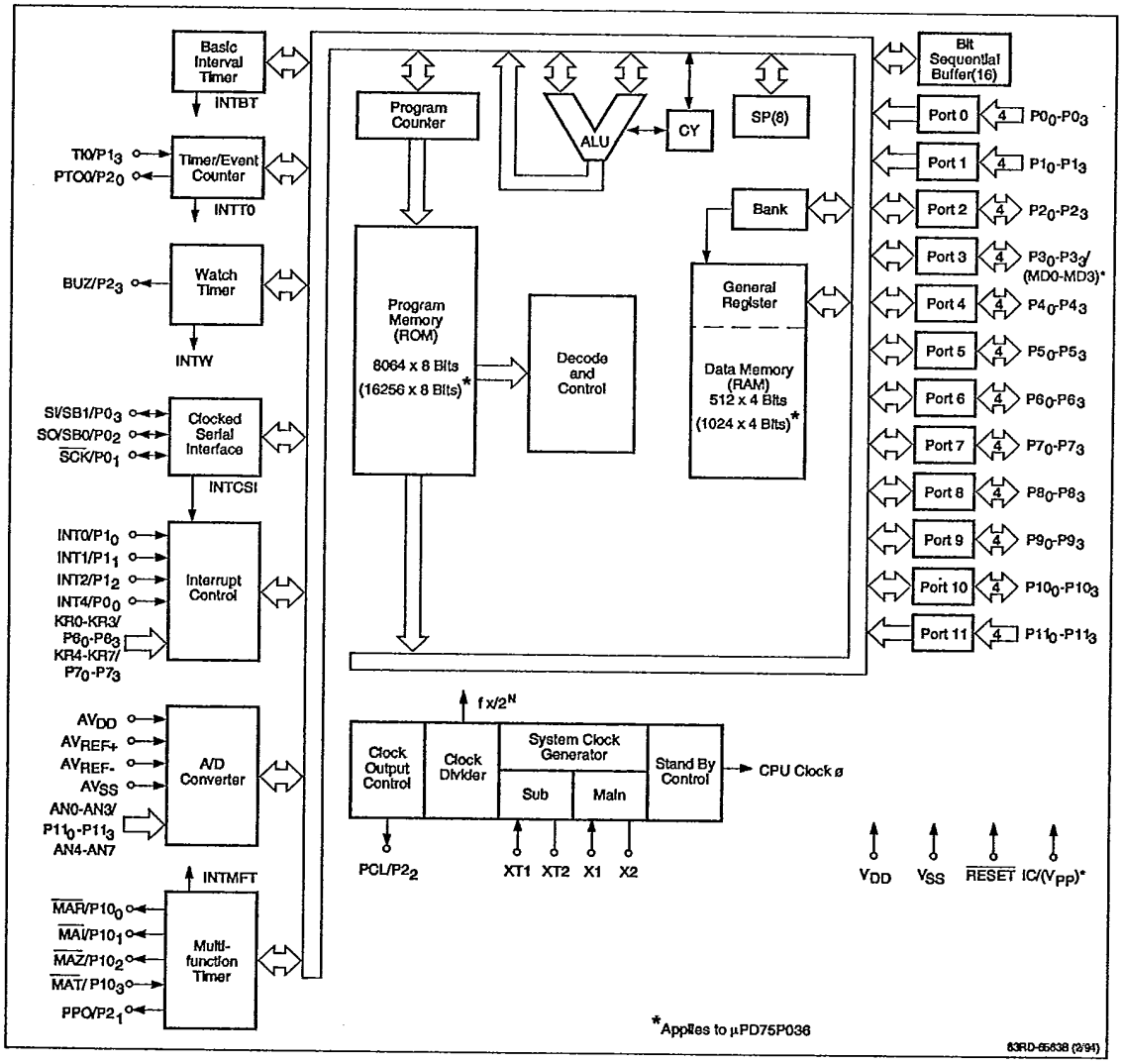
μPD75036 Family Differences

The μPD75028, μPD75036, and μPD75P036 differ only in their program memory, data memory, mask options, and AC/DC specifications. The μPD75P036 contains a one-time programmable (OTP) program memory, and the μPD75028 and μPD75036 contain a mask ROM program memory. Table 1 shows the differences among these parts except for AC/DC specification differences.

Table 1. Differences Among μPD75036 Family Devices

Item	μPD75028	μPD75036	μPD75P036
Program memory	Mask ROM	Mask ROM	One-time EPROM
	8064 x 8 bits	16,256 x 8 bits	16,256 x 8 bits
	0000H - 1F7FH	0000H-3F7FH	0000H - 3F7FH
Data memory (RAM)	512 x 4	1024 x 4	1024 x 4
Ports 4, 5 and 10 pullup resistor	Mask option	Mask option	Not offered
Subsystem clock internal feedback resistor	Mask option	Mask option	Not offered

Block Diagram; μPD75028/P036



CPU AND MEMORY ARCHITECTURE

The 75X architecture has two separate address spaces, one for program memory (ROM) and another for data memory (RAM).

Program Memory (ROM)

The ROM is addressed by the 13- or 14-bit program counter. The size of the program counter and the amount of ROM present depend on which family member is being used. The ROM contains program object code, interrupt vector table, GETI instruction reference table, and table data. Table data can be obtained using the table reference instruction, MOVT.

Figure 1 shows the addressing range that can be made using a branch instruction or subroutine call instruction. In addition, the BR PCDE and BR PCXA instructions can be used for a branch where only the low 8 bits of the PC are changed. The program memory addresses are:

75028	0000H to 1F7FH
75P036/P036	0000H to 3F7FH

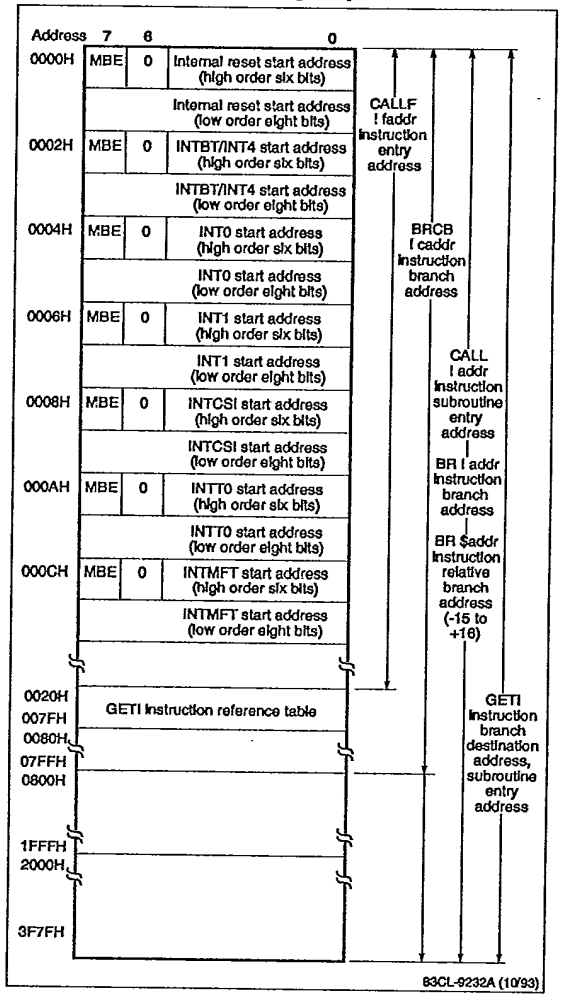
All locations in ROM except 0000H and 0001H can be used as program memory. However, if interrupts or GETI instructions are used, the locations corresponding to those functions cannot be used. Addresses are normally reserved as follows.

0000H to 0001H — This address area is used as the vector address for $\overline{\text{RESET}}$; it also contains the MBE bit.

0002H to 000DH — This area is used for interrupt vector addresses. Each vector address contains an MBE bit value.

0020H to 007FH — This is the table area for GETI instructions. The GETI instruction can access one 2-byte or two 1-byte instructions using 1 byte of program memory. This is useful in compacting code.

Figure 1. Program Memory Map



Program Counter (PC)

This is a 13/14-bit binary counter containing the address of the current program memory location. The 75028 has a 13-bit PC and the 75036/P036 have a 14-bit PC.

When an instruction is executed, the PC is automatically incremented by the number of bytes of the current instruction. When a branch instruction (BR, BRCB) is executed, the contents of the immediate data or register pair indicating the new address are loaded into some or all the bits of the PC. When a subroutine call instruction (CALL, CALLF) is executed or an interrupt is generated, the PC is incremented to point to the next instruction and the contents of the PC are saved on the stack.

During an interrupt, the contents of the PC and the program status word (PSW) are also automatically saved on the stack. The address to be jumped to by the CALL or interrupt is then loaded into the PC.

When a return instruction (RET, RETS, or RETI) is executed, the contents of the stack are restored to the PC.

Data Memory (RAM)

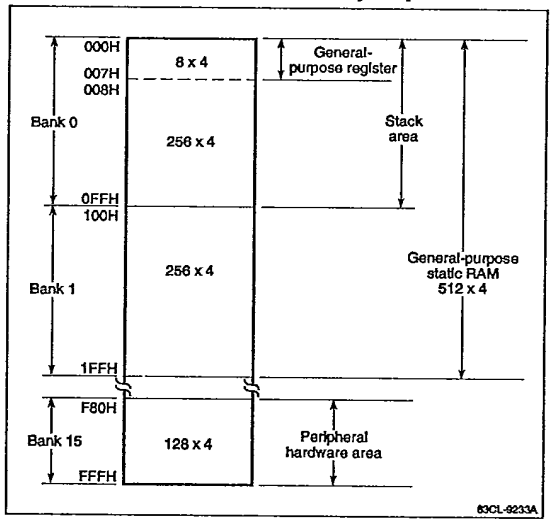
The 75028 data memory contains three memory banks (0, 1, and 15) and the 75036/P036 contain five memory banks (0, 1, 2, 3, and 15). The RAM memory map is shown in figure 2 for the 75028 and figure 3 for the 75036/P036. The memory consists of general-purpose static RAM and peripheral control registers. The memory banks are accessed using MBE (memory bank enable) and by programming the BS (bank select) register. If MBE = 0, the lower 128 nibbles of memory bank 0 and the upper 128 nibbles of memory bank 15 are accessed. If MBE = 1, the upper 4 bits in the BS register will specify the memory bank.

The values are 0H for memory bank 0, 1H for memory bank 1, 2H for memory bank 2, 3H for memory bank 3, and FH for memory bank 15. Memory banks 0, 1, 2, and 3 contain 256 nibbles. Although the memory is organized in nibbles, the 75X architecture allows the data to be manipulated in bytes, nibbles, and individual bits.

The data memory is used for storing processed data, as general-purpose registers, and as a stack for subroutine or interrupt service. Because of its static nature, the RAM will retain its data when CPU operation is stopped and the chip is in the standby mode, provided V_{DD} is at least 2 volts.

There are eight 4-bit general-purpose registers (figure 4) in bank 0 starting at location 00H. These registers may also be used as four 8-bit registers. The on-chip peripheral control registers and ports reside in the upper 128 nibbles of bank 15. Bank 15 addresses not assigned to a register are not available as random memory except for the 16-bit sequential buffer. Also, the lower 128 nibbles of bank 15 do not contain RAM.

Figure 2. μPD75028 Data Memory Map



Addressing Modes

The μPD75036 family can address data memory and ports as individual bits, nibbles, or bytes. These addressing modes are as follows.

- 1-bit direct data memory
- 4-bit immediate
- 4-bit register indirect (@ rpa)
- 4-bit direct data memory
- 8-bit immediate
- 8-bit register indirect (@ HL)
- 8-bit direct data memory

Tables 2 and 3 show the data memory addressing modes. Figures 5 and 6 show the data memory organization and addressing modes for the μPD75028 and μPD75036/P036, respectively.

Figure 3. μPD75036/P036 Data Memory Map

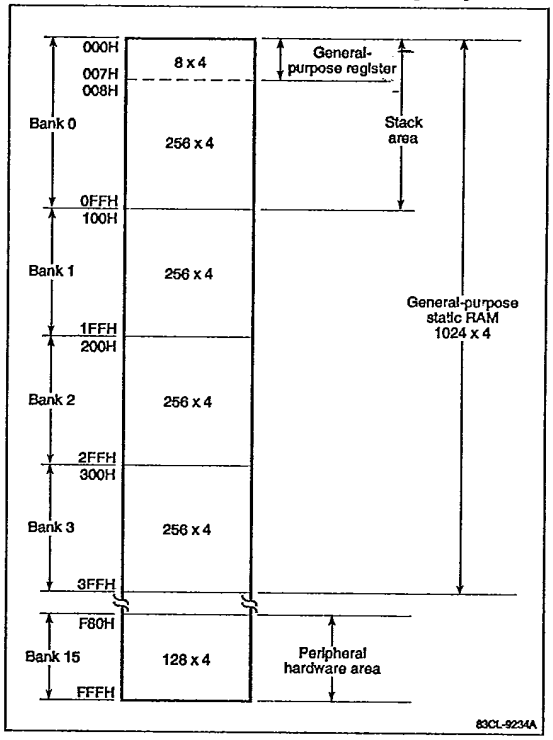


Figure 4. General-Purpose Register Configurations

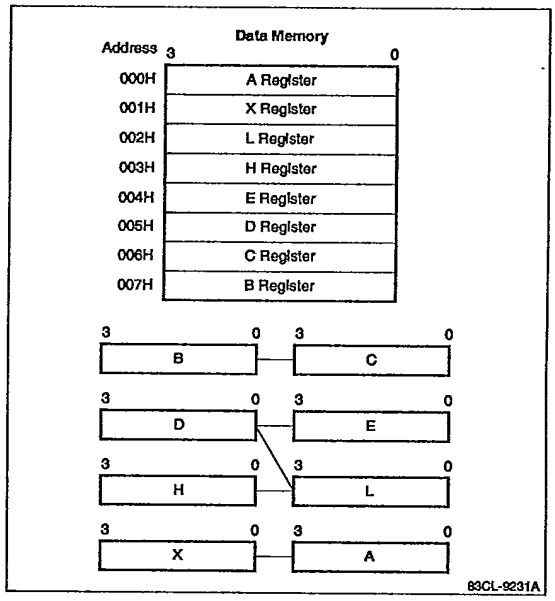


Table 2. Data Memory Addressing Modes

Addressing Mode	Format	Address

1-bit direct addressing	mem.bit	The memory bank is,
		if MBE = 0:
		MB = 0 for addr 00H-7FH
		MB = 15 for addr 80H-FFH
		if MBE = 1:
		MB = (MBE)•(MBS Reg)
		The memory location and bit within the memory bank is mem.bit.

4-bit direct addressing	mem	The memory bank is,
		if MBE = 0:
		MB = 0 for addr 00H-7FH
		MB = 15 for addr 80H-FFH
		if MBE = 1:
		MB = (MBE)•(MBS Reg)
		The memory location within the memory bank is mem.

8-bit direct addressing	mem	The memory bank is,
		if MBE = 0:
		MB = 0 for addr 00H-7FH
		MB = 15 for addr 80H-FFH
		if MBE = 1:
		MB = (MBE)•(MBS Reg)
		The memory location within the memory bank is mem.

4-bit register indirect addressing	@HL	If MBE = 0, MB = 0 If MBE = 1: MB = (MBE)•(MBS Reg) The memory location within the memory bank is contained in register HL.
	@DE	The memory bank is always bank 0 independent of MBE & MBS. The memory location within the memory bank is contained in register DE.
	@DL	The memory bank is always bank 0. independent of MBE & MBS. The memory location within the memory bank is contained in register DL.
8-bit register indirect addressing	@HL	If MBE = 0, MB = 0 If MBE = 1: MB = (MBE)•(MBS Reg) The memory location within the memory bank is contained in register HL. HL must contain an even address.

Table 2. Data Memory Addressing Modes (cont)

Addressing Mode	Format	Address
Bit manipulation addressing	fmem.bit	The memory bank is bank 15 independent of MBE & MBS. The memory location in bank 15 is fmem where: fmem = B0H-BFH for interrupts fmem = F0H-FFH for I/O ports The bit is specified in fmem.bit.
	pmem.@L	The memory location is always FC0H to FFFH independent of MBE and MBS. The upper 10 bits of the location are in the high-order 10 bits of pmem and the 2 lower address bits are in the upper 2 bits of register L. The bit to be manipulated is specified by the 2 LSBs of register L.
	@H + mem. bit	The memory bank is: MB = (MBE)•(MBS Reg) The memory location within the memory bank is: 4 upper bits are in register H 4 lower bits are mem The bit is specified in mem.bit.
Stack addressing		The stack is always in bank 0 and the address is indicated by stack pointer SP.

MBE Memory bank enable bit
MB Memory bank
MBS Memory bank select register
mem Memory location
mem.bit Memory location and a bit at that location

Table 3. On-Chip Peripherals Addressing Modes

Manipulation	Addressing Mode	Hardware
Bit	MBE = 0 or MBE = 1, and MBS = 15; direct addressing with bank address specified in mem.bit.	All hardware where bit manipulation can be performed.
	Direct addressing regardless of the setting of MBE and MBS. Bank address specified in fmem.bit.	ISTO, MBE; IExxx, IRQxxx, PORTn.x
	Indirect addressing regardless of the setting of MBE and MBS. Bank address specified in pmmem.@L.	BSBn.x; PORTn.x
4-bit	MBE = 0 or MBE = 1, and MBS = 15; direct addressing with bank address specified in mem.	All hardware where 4-bit manipulation can be performed
	MBE = 1 and MBS = 15; register indirect addressing with bank address specified in HL.	
8-bit	MBE = 0 or MBE = 1, and MBS = 15; direct addressing with bank address specified in mem; mem must be an even address.	All hardware where 8-bit manipulation can be performed
	MBE = 1 and MBS = 15; register indirect addressing with bank address specified in HL; L register must contain an even number.	

Figure 5. Data Memory Organization and Addressing Modes of μPD75028

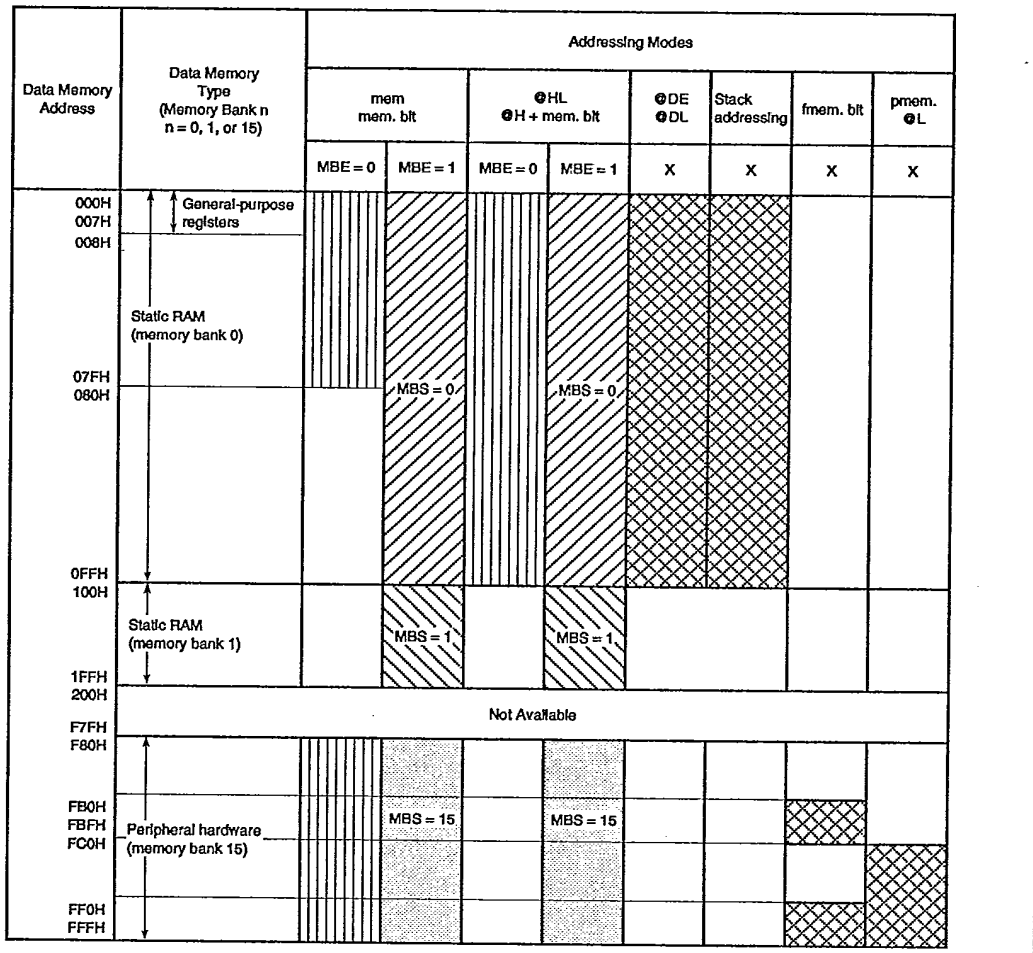
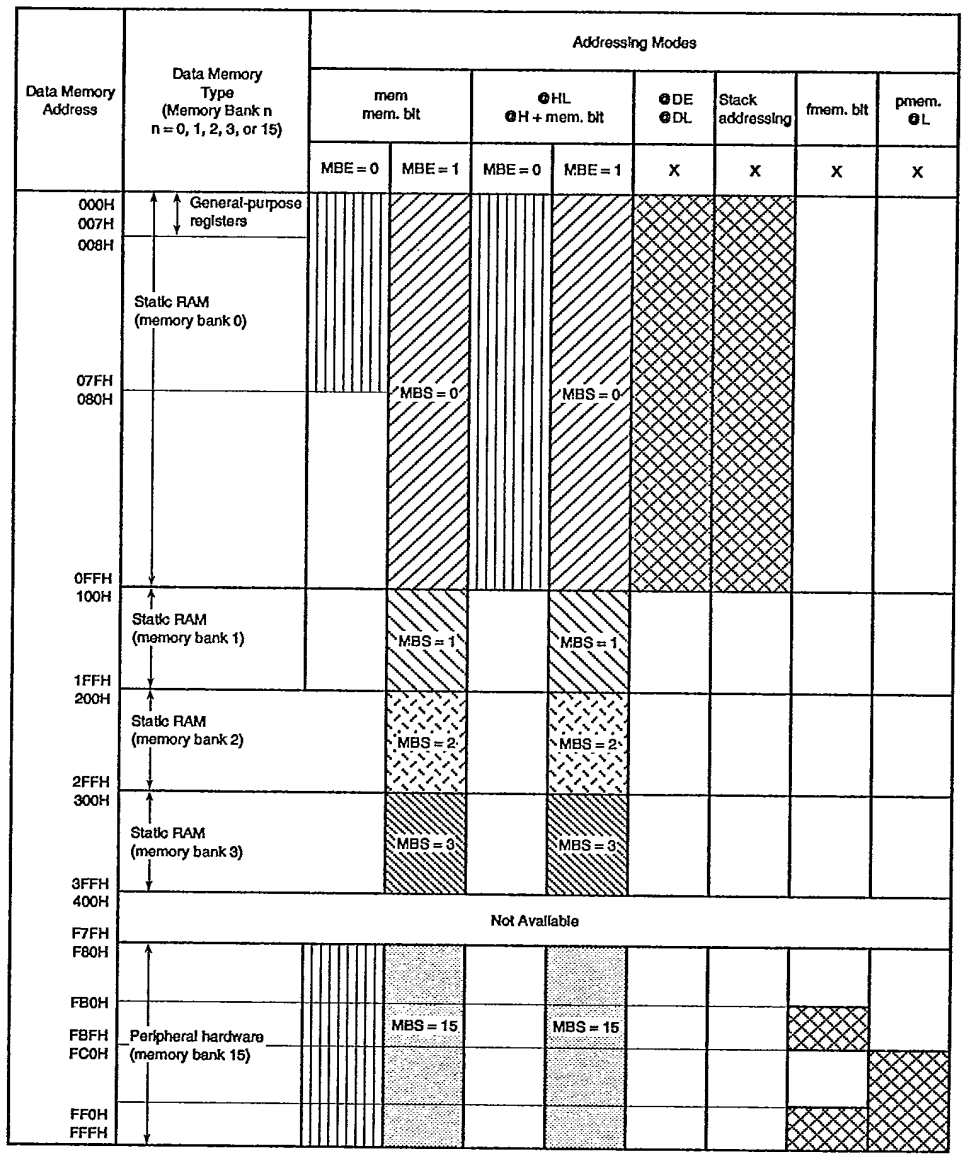


Figure 6. Data Memory Organization and Addressing Modes of μPD75036/P036



X MBE has no effect
MBE Memory bank enable bit
MBS Memory bank select register

83CL-9236B (10/93)

FUNCTIONAL DESCRIPTION

Input/Output Ports

The μPD75036 family provides twelve 4-bit ports; nine are input/output and three are input only. Table 4 lists the function and operation of the I/O ports. Figure 7 shows the internal circuits, which are classified into 14 types.

Table 4. Operation of the Digital I/O Ports

Port	Input/Output	Operation	Additional Pin Applications
P0, P1, P11	4-bit input	Can be read or tested regardless of the operation mode of the following pins: SO/SB0, SI/SB1, $\overline{SCK}$, INT0, INT1, INT2, INT4, TI0, AN0, AN1, AN2, AN3.	SO/SB0, SI/SB1, $\overline{SCK}$, INT0, INT1, INT2, INT4, TI0, AN0, AN1, AN2, AN3.
P3	4-bit I/O	Can be set up in input or output mode in 1-bit units.	
P6	4-bit I/O		KR0 to KR3
P2	4-bit I/O	Can be set up in input/output mode in 4-bit units. Ports 6 and 7 can be paired for data input/output in 8-bit units.	PTO0, PCL, and BUZ
P7	4-bit I/O		KR4 to KR7
P8	4-bit I/O		
P9	4-bit I/O		
P4, P5, P10	4-bit I/O (n-channel, open-drain, 10 volts)	Can be set up in input or output mode in 4-bit units. Ports 4 and 5 can be paired for data input/output in 8-bit units. An LED can be driven directly.	Internal pullup resistor specified in 1-bit units by the mask option. $\overline{MAR}$, $\overline{MAI}$, $\overline{MAZ}$, $\overline{MAT}$.

Figure 7. Input/Output Circuits (Sheet 1 of 2)

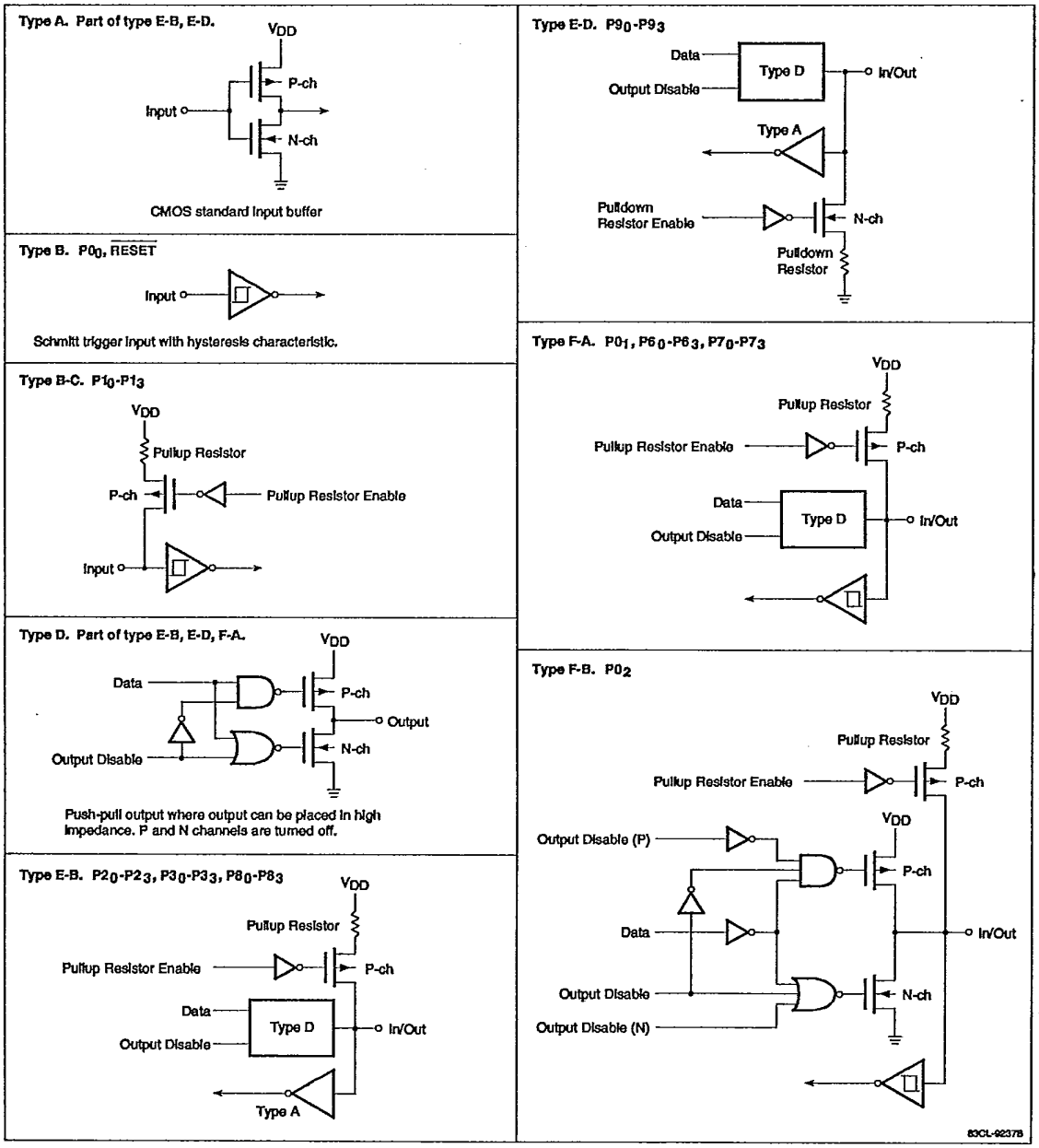
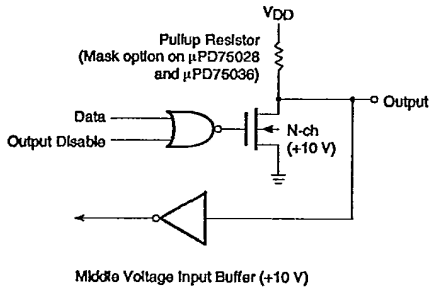
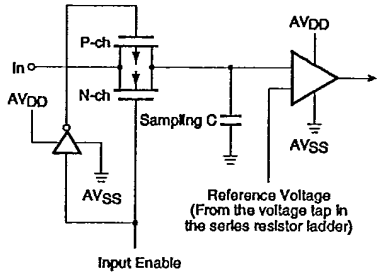


Figure 7. Input/Output Circuits (Sheet 2 of 2)

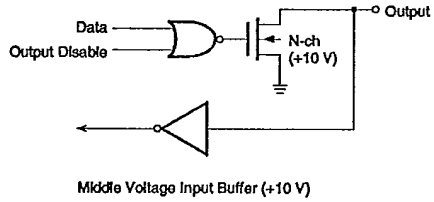
Type M. $P4_0$-$P4_3$, $P5_0$-$P5_3$, $P10_0$-$P10_3$



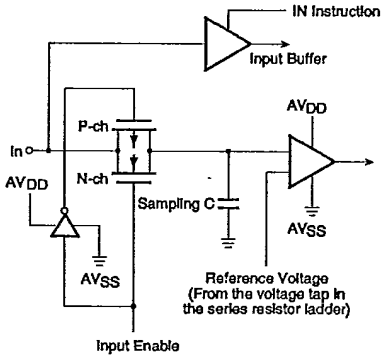
Type Y. AN4-AN7



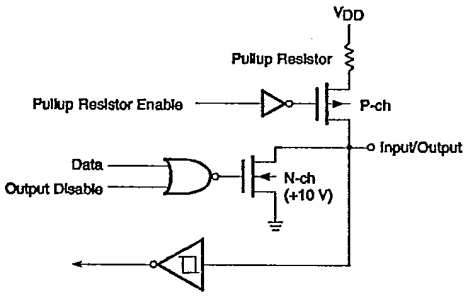
Type M-A. $P4_0$-$P4_3$, $P5_0$-$P5_3$, $P10_0$-$P10_3$, μPD75P036



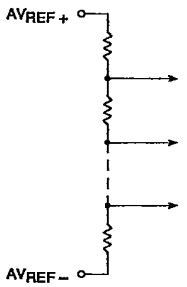
Type Y-A. $P11_0$-$P11_3$



Type M-C. $P0_3$



Type Z-A. AV_{REF}



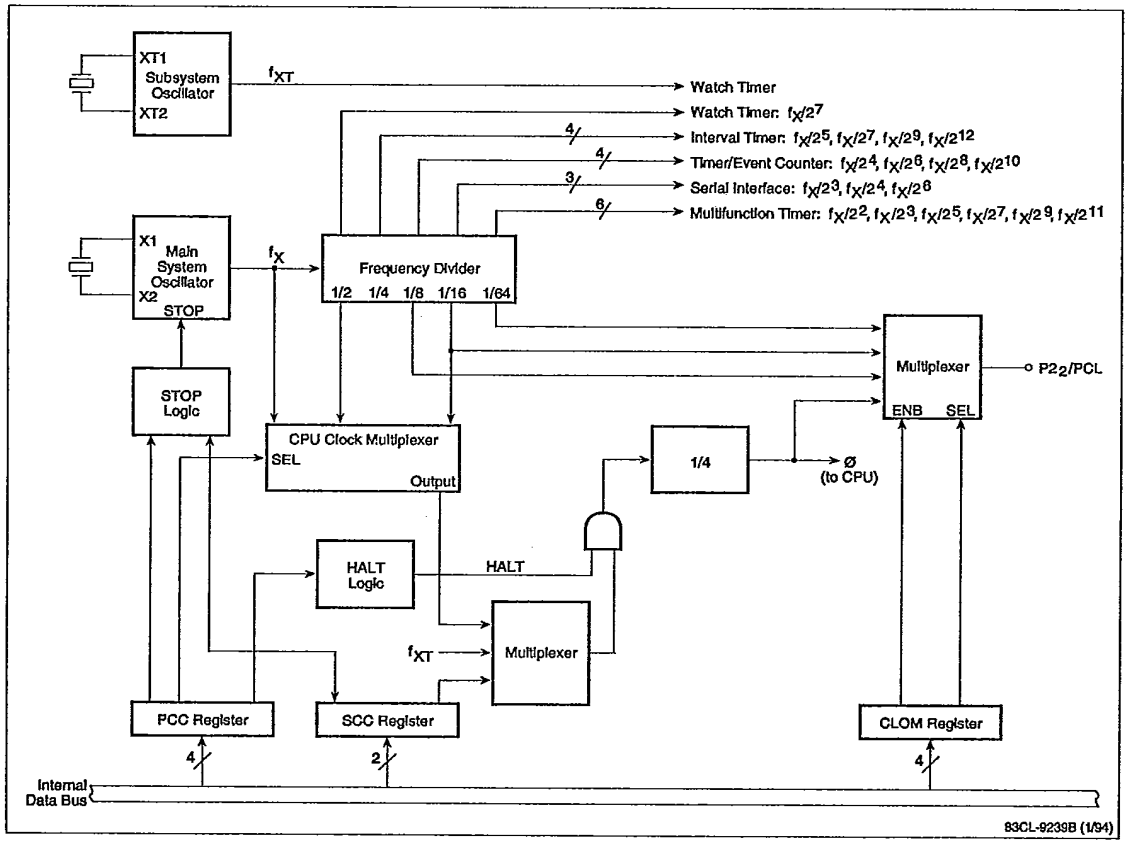
83CL-9238B (2/94)

Clock Generator

The clock generator uses a crystal as a time base to generate its clocks. Figure 8 shows the generator, which consists of main and subsystem oscillators, frequency dividers, multiplexers, and three control registers (PCC, SCC, and CLOM). Registers PCC and SCC are programmed to supply frequencies derived from the crystal to the CPU at one of four speeds. Register CLOM controls the clock output to output pin PCL. Registers PCC and SCC control the HALT and STOP logic.

The μPD75036 family contains a subsystem clock with an oscillator driven by an external crystal. The clock operates from 32 to 35 kHz. It can be used as a clock source for the watch timer and the CPU.

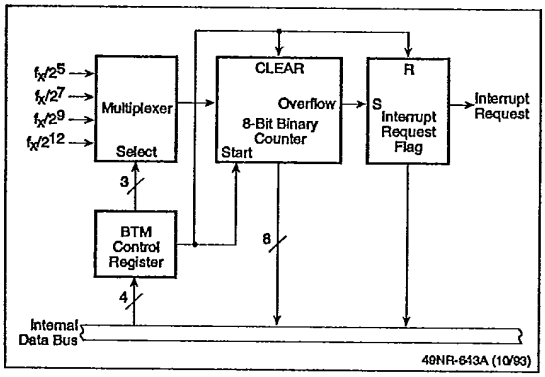
Figure 8. Clock Generator



Basic Interval Timer

The basic interval timer (figure 9), which provides continuous real-time interrupts, consists of a multiplexer, an 8-bit free-running counter, and a 4-bit BTM control register. Every time the counter overflows from FFH to 00H, it generates an interrupt and continues to count. In addition to clearing the counter and its interrupt request, the BTM register is used to select one of four clock inputs. The counter can generate 250-ms interrupts with a 4.19-MHz crystal. It provides the oscillator stabilization time when the chip leaves the STOP mode.

Figure 9. Basic Interval Timer



Timer/Event Counter

The timer/event counter (figure 10) consists of a binary 8-bit up-counter, 8-bit modulo register, 8-bit comparator, clock multiplexer, mode control register TM0, and a TOUT flip-flop. Control logic allows the TOUT flip-flop signal to be output to port 2, bit 2.

The counter operates when an 8-bit value is loaded into the modulo register. A count register clock is selected in the clock multiplexer by control register TM0. The 8-bit up-counter is incremented every time it receives a counter pulse (CP).

When the count value equals the modulo register count, the 8-bit comparator outputs a signal. This toggles the TOUT flip-flop and resets the count register to 00H. The count register continues to count up unless it is stopped. Every time the comparator has a match, the TOUT flip-flop changes state and interrupt request IRQT0 is generated. Signal TOUT can also be used as a clock for the serial interface.

Watch Timer

The watch timer (figure 11) is normally used as a time source for keeping track of the time of day. With a 4.19-MHz crystal, it will generate interrupt requests (not interrupts) at 0.5-second intervals. The timer consists of an input clock multiplexer, frequency divider, output multiplexer, control logic, and control register WM.

When a subsystem clock is present, the timer can operate in the STOP mode. Using the buzzer multiplexer, the timer can output a 2-, 4-, or 32-kHz buzzer signal.

Multifunction Timer

The multifuction timer (MFT) is a 16-bit timer that can be configured to operate in one of four modes:

- Interval timer
- Pulse-width modulation (PWM) timer
- Free-running timer
- A/D converter

The MFT consists of a clock multiplexer, two 8-bit count registers (MFTH and MFTL), MFT flip-flop (MFT F/F), multifunction timer mode (MFTM) control register, and multifunction timer control (MFTC) register; these components are used in all four modes. Also contained is a tap multiplexer, comparator, edge selector, and A/D conversion control logic; these components are used in some of the four configurations, but not all.

The configuration and use of the MFT components depend upon the MFT operating mode, which is set by programming the MFTM register. The three lower register bits (0-2) select one of the six counter clock sources. MFTM bit 3 selects a rising or falling edge of input MAT in the A/D converter mode. The four MSBs of MFTM (7-4) select one of the four modes, and whether the counter will be 6, 7, 8, 13, 14, 15, or 16 bits. The MFTC register is not shown in any of the figures; it is used for timer output control, count register initialization, and count operation control.

Interval Timer Mode. This configuration is used to output a square wave from the MFT flip-flop. The MFT is configured as shown in figure 12 by programming MFTM bits 7-4 to 0000B and the timer is always 8 bits. One 8-bit counter is used as an 8-bit count register, and it is clocked by the clock multiplexer output (CP). The second 8-bit counter is used as an 8-bit modulo register. The frequency of the square wave is a function of the frequency of the clock source (selected by MFTM bits 0-2) and the number in the modulo register. The two

register outputs are connected to an 8-bit comparator whose output is connected to the MFT flip-flop.

An 8-bit value is written to the 8-bit modulo register and MFTM is programmed to select a clock source to the 8-bit count register. The count register counts up and when count value matches the value in the modulo register, the comparator generates interrupt request IRQMFT, clears the 8-bit count register, and toggles the MFT flip-flop. The count register continues to count, starting from 00H, and the sequence repeats as described above. The period of the square wave is twice the time it takes to count from zero to the value in the modulo register.

PWM Mode. This configuration is used to output a PWM waveform from the MFT flip-flop (PPO/$P2_1$). The PWM can be 6, 7, or 8 bits. The MFT is configured as shown in figure 13 by programming MFTM bits 7-4 to 0001B or 001XB. One 8-bit counter is used as an 8-bit count register and it is clocked by the clock multiplexer output (CP). The second 8-bit counter is used as an 8-bit modulo register. The frequency of the PWM waveform is a function of the clock source frequency (selected by MFTM bits 0-2) and whether the counter is 6, 7, or 8 bits long.

The width of the output pulse is a function of the clock source frequency and the number in the modulo register. The two register outputs are connected to an 8-bit comparator, which is connected to the MFT flip-flop. The tap multiplexer's output is selected by programming the MFTM register; the output will be bit 6, bit 7, or bit 8 of the count register.

An 8-bit value is written to the 8-bit modulo register and MFTM is programmed to select the clock source to the 8-bit count register. The count register is a free-running counter; its maximum count is FFH if counter bit 8 is used, 7FH if bit 7 is used, or 3FH if bit 6 is used. When the counter reaches its maximum value, it will set the MFT F/F, reload the modulo register, generate interrupt request IRQMFT, overflow to count 00H, and continue counting. The count register counts up, and when its value matches the value in the modulo register, the comparator resets the MFT F/F, thereby controlling the output pulse width.

Free-Running Timer Mode. In this configuration, the MFT is used to output a free-running square wave from the MFT F/F (PPO/$P2_1$). The timer can be 13, 14, 15, or 16 bits. The MFT is configured as shown in figure 14 by programming MFTM bits 7-6 to 10B. Registers MFTH and MFTL are concatenated to form one 16-bit counter with four taps.

The frequency of the square wave from the MFT F/F is a function of the clock source and counter tap selected. The clock source is selected by MFTM bits 0-2 and counter tap 13, 14, 15, or 16 is selected by MFTM bits 5-4. The counter counts up and when it reaches its maximum value, it overflows to 0000H. Each time the counter overflows, it toggles the MFT F/F. The maximum value for tap 13 is 1FFFH; tap 14, 3FFFH; tap 15, 7FFFH; and tap 16, FFFFH.

Figure 10. Timer/Event Counter

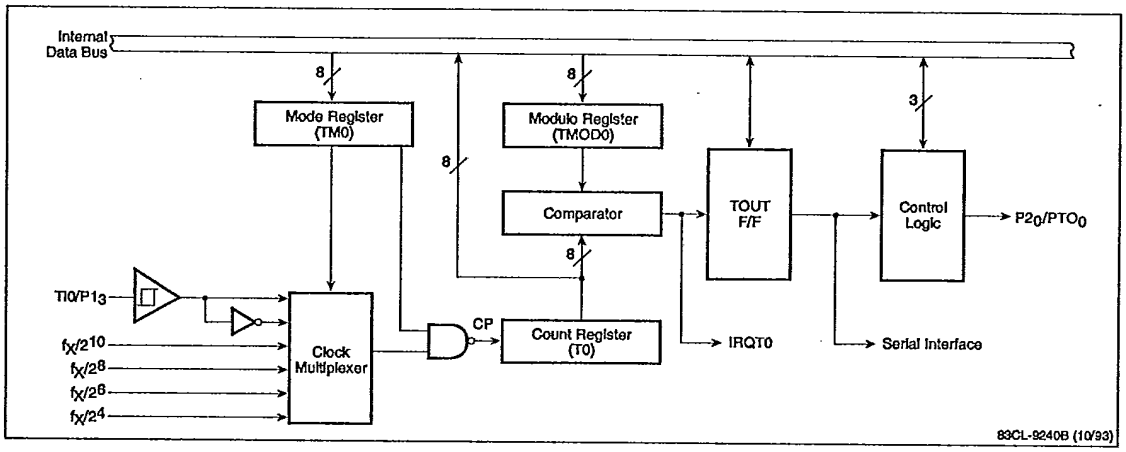


Figure 11. Watch Timer

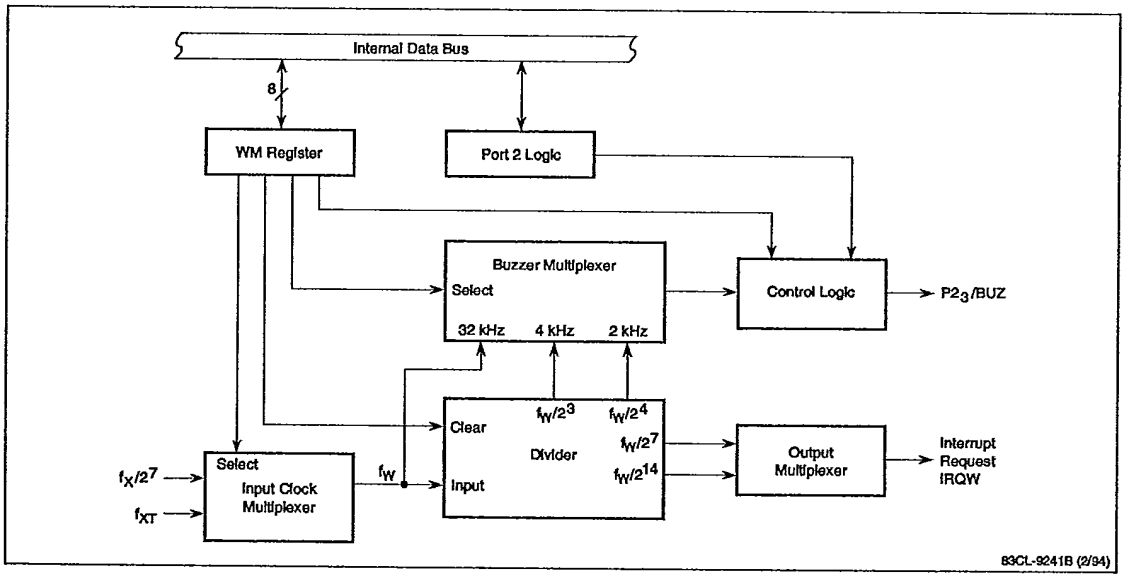


Figure 12. Multifunction Timer in Interval Timer Mode

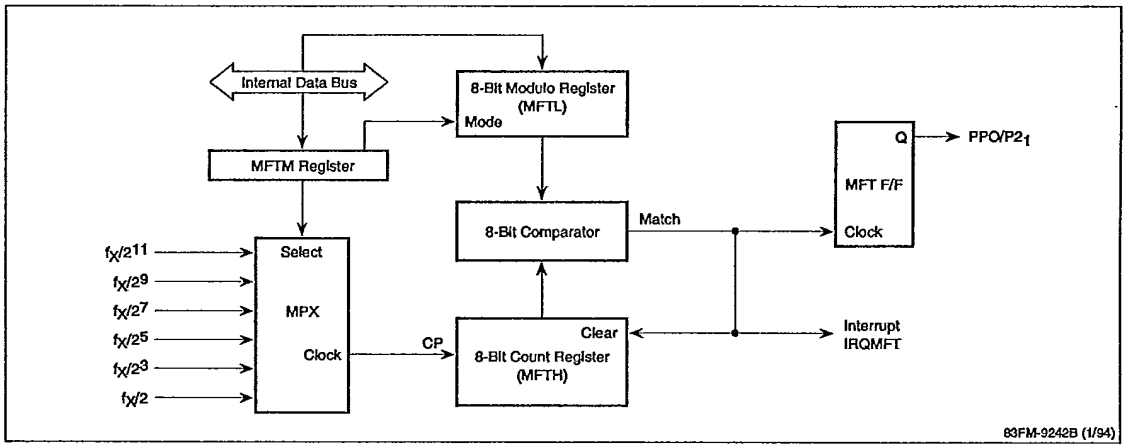


Figure 13. Multifunction Timer in PWM Mode

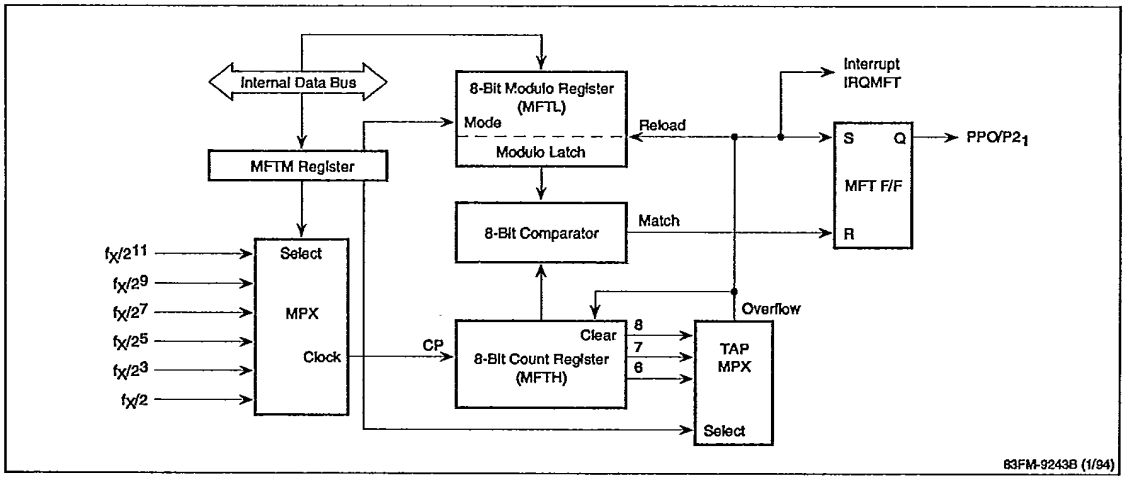


Figure 14. Multifunction Timer in Free-Running Timer Mode

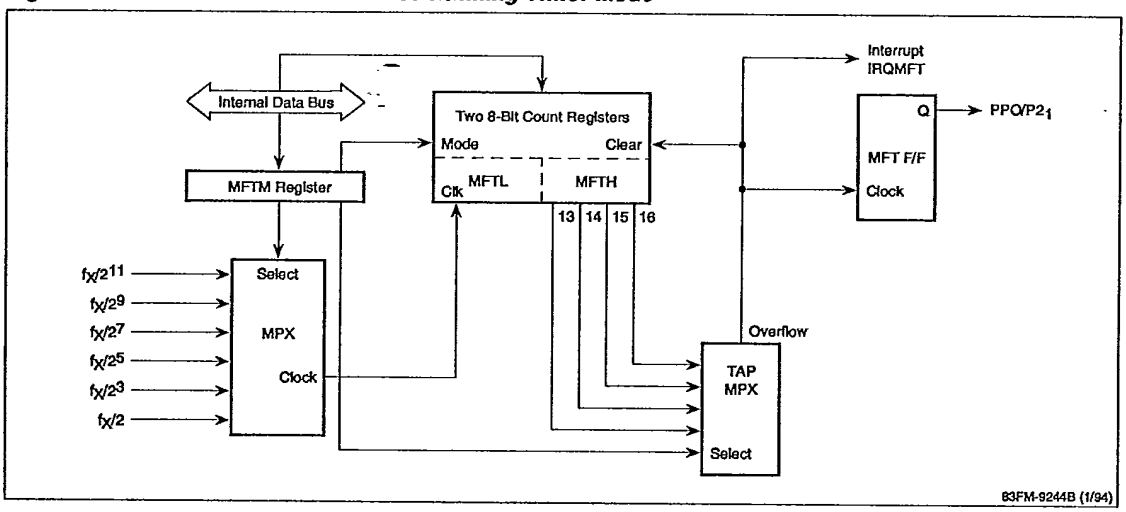
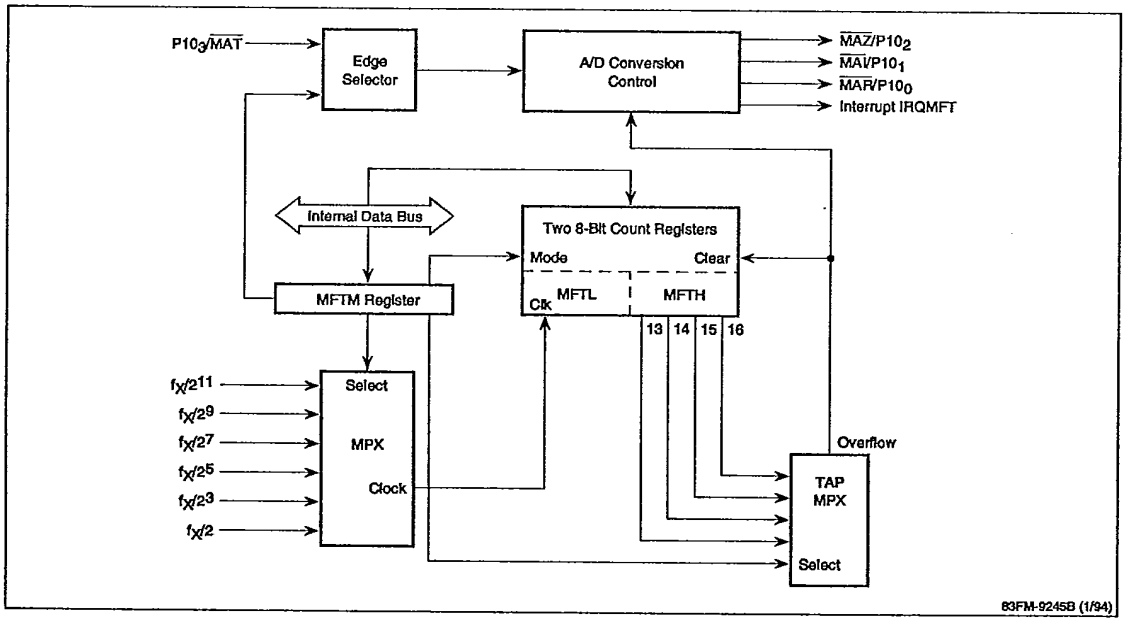


Figure 15. Multifunction Timer in A/D Converter Mode



A/D Converter Mode. When the MFT is used with analog circuitry, a dual-slope A/D converter can be implemented. The converter can be 13, 14, 15, or 16 bits. A dual-slope A/D converter consists of digital and analog circuitry. The MFT can be configured to perform the digital portion of the A/D by programming bits MFTM bits 7-6 to 11B (see figure 15). The analog circuitry must be provided off-chip as shown in figure 16.

In the A/D converter mode, registers MFTH and MFTL are concatenated to form one 16-bit counter with four taps (13, 14, 15, or 16 bits). The accuracy of the dual-slope A/D converter is a function of the selected counter tap (MFTM bits 5-4); the A/D conversion time is a function of the selected clock source (MFTM bits 0-2). Assuming a 4.19-MHz crystal, the A/D conversion times are:

13-bit	11.7 ms
14-bit	23.4 ms
15-bit	46.9 ms
16-bit	93.8 ms

The digital circuitry consists of a clock multiplexer, 16-bit counter, tap multiplexer, input edge selector, and A/D conversion control circuitry. The conversion control contains outputs $\overline{MAZ}$ (autozero phase), $\overline{MAI}$ (signal integrate phase), $\overline{MAR}$ (reference integrate phase), interrupt IRQMFT, and input $\overline{MAT}$ (auto A/D termination).

Figure 17 shows the timing for one A/D conversion cycle. It consists of autozero, signal integrate, and reference integrate phases. The timing of the phases is generated by the A/D control conversion logic and outputted on the $\overline{MAZ}$, $\overline{MAI}$, and $\overline{MAR}$ signals, respectively. The end of the A/D conversion occurs when comparator A3 (figure 16) goes from 1 to 0 at the $\overline{MAT}$ input. This stops the conversion cycle and generates interrupt IRQMFT. At this time, the A/D conversion result may be read from the 16-bit register.

Serial Interface

The 8-bit serial interface allows the μPD75036 family to communicate with other NEC or NEC-like serial interfaces. The serial interface consists of an 8-bit shift register (SIO), serial output latch (SO), 8-bit address comparator, slave address register (SVA), control registers (CSIM and SBIC), busy/acknowledge circuitry, and bus release/detect circuitry. See figure 18. The interface also contains a serial clock counter, clock multiplexer, and serial clock control logic. The serial interface contains a three-wire interface, which consists of the following:

- Serial data in (SI/SB1)
- Serial data out (SO/SB0)
- Serial shift clock ($\overline{SCK}$)

The three serial interface operation modes are:

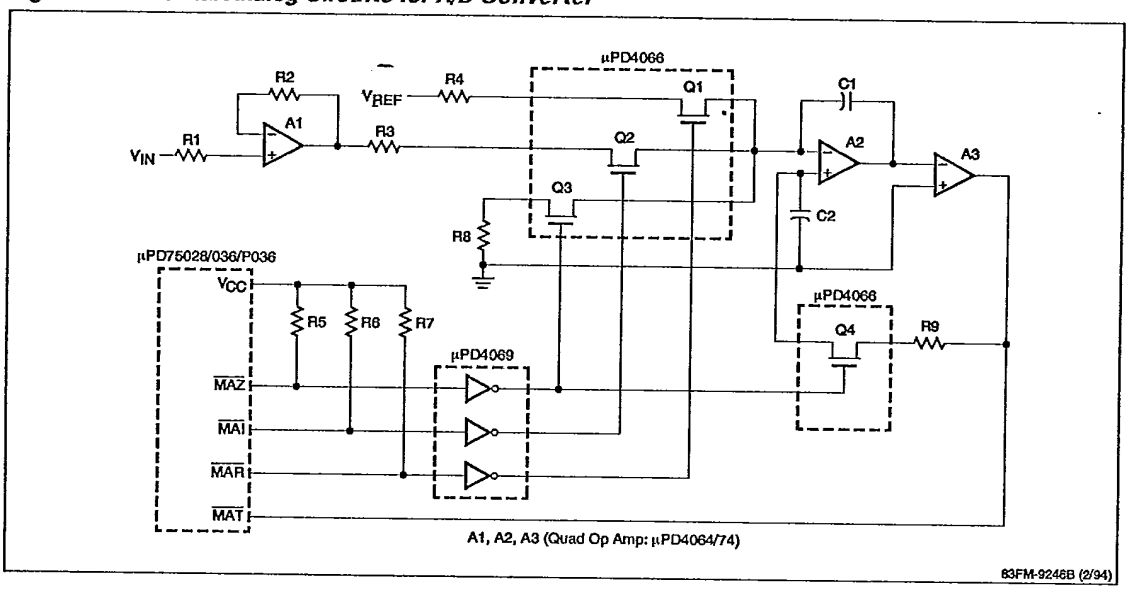
- Two-wire serial
- Three-wire serial
- Two-wire SBI

The two- or three-wire serial modes are the simplest: the 8-bit shift register is loaded with a byte of data and eight clock pulses are generated. The pulses shift data out of the SO line and in from the SI line, thereby communicating in full duplex. When a byte of data is sent, a burst of eight clock pulses is generated and 8 bits of data are sent. The data may be sent with the LSB or MSB first. The interface can also be set to receive data only, consequently SO will be in the high-impedance state. One of four internal clocks or an external clock clocks the data.

The SBI mode uses a two-wire interface with devices in a master/slave configuration. See figure 19. There is only one master device at a time; all others are slaves. The master sends addresses, commands, and data over the bus. The slaves are able to detect in hardware if their addresses were sent, a command was sent, or a portion of data was sent.

There can be up to 256 slave addresses, 256 commands, and 256 data types. All commands are user definable. Commands can be sent to change slaves into masters; previous masters become slaves. Firmware performs this type of operation and thus the user decides whether the bus is simple or complex.

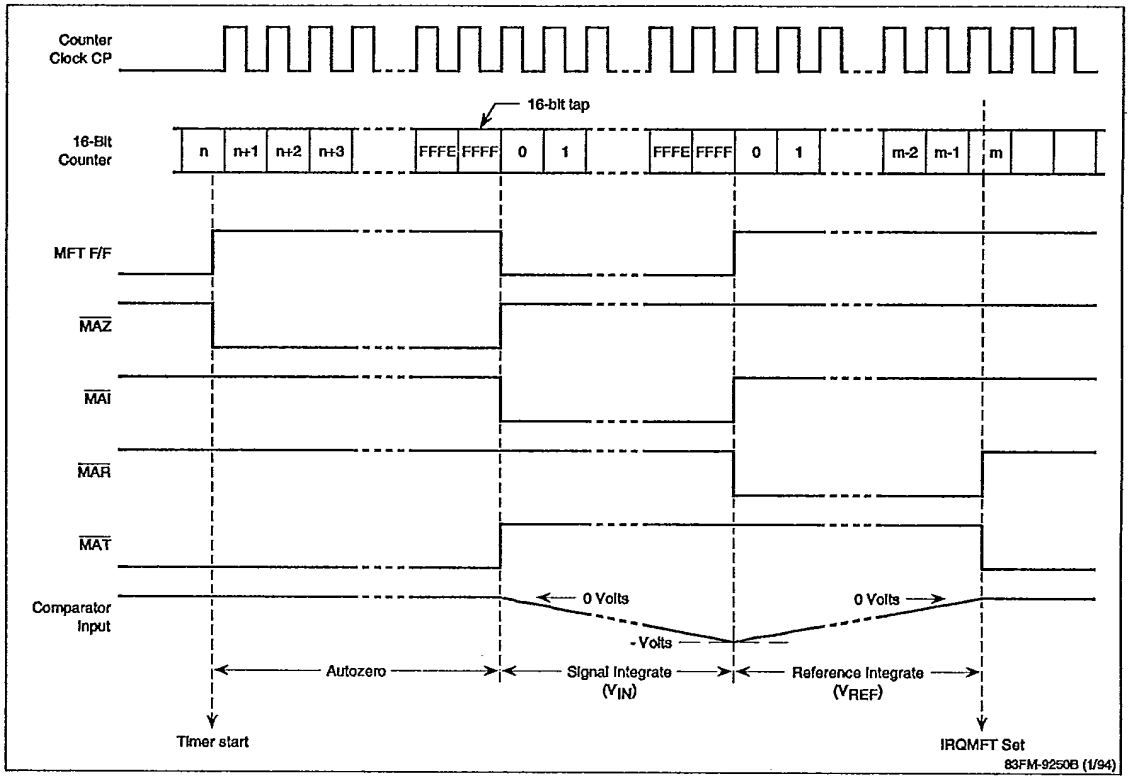
Figure 16. External Analog Circuits for A/D Converter



A/D Converter

The 8-bit analog-to-digital (A/D) converter is equipped with eight inputs and uses a successive approximation routine (SAR) for the conversion. See figure 20. An A/D conversion occurs when one of eight inputs is selected by the ADM register. The conversion starts by setting bit 3 of the ADM register. The selected input is sampled using the sample and hold circuit and the multiplexer. Then, using the SAR with the comparator, resistor ladder, and SA register, the input value is converted and stored in the SA register. When bit 2 of the ADM register is set, conversion is complete and the converted value can be read from the SA register.

Figure 17. A/D Converter Timing Diagram



Bit Sequential Buffer

The 16-bit sequential buffer is the only general-purpose RAM in the upper half of data memory bank 15. All other locations in this bank contain either on-chip peripheral control registers or unused addresses. The bit sequential buffer can be bit, nibble, or byte manipulated. Its bits are addressed by register L and can be sequentially scanned by incrementing or decrementing L.

A typical application for this buffer is data storage for the next serial output or input. Another application is as a port output data storage area.

Interrupts

The three external and four internal interrupts are all vectored interrupts and are shown in figure 21. Table 5 is a summary of the interrupts. Input INT2 detects rising-edge inputs and generates an interrupt request flag, which is testable. Inputs KR0 through KR7 detect a falling edge and generate the same interrupt request flag as INT2. Inputs INT2 and KR0-KR7 do not cause an interrupt, but can be used to release the standby mode. Interrupt requests and all interrupts except INT0 release the standby mode.

Figure 18. Serial Interface Block Diagram

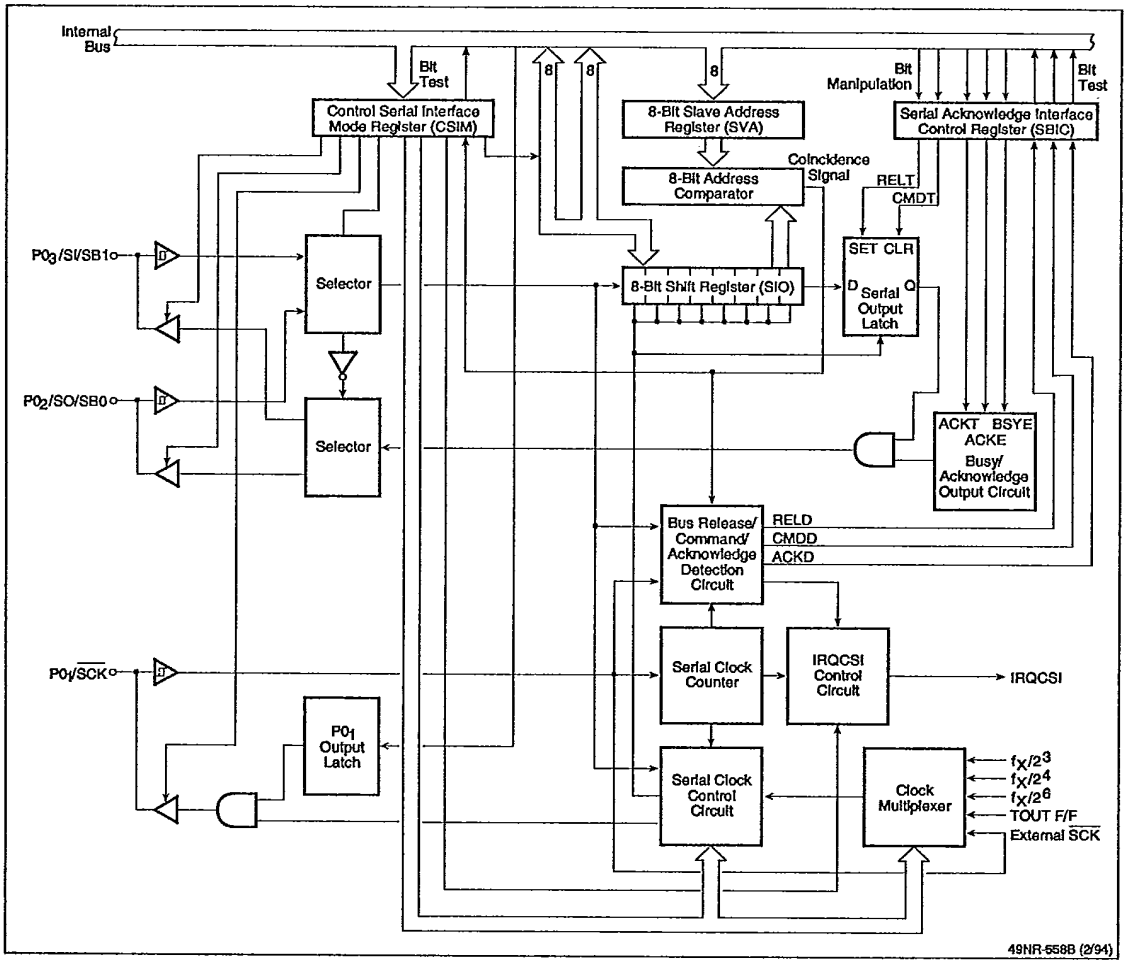


Figure 19. SBI Mode Master/Slave Configuration

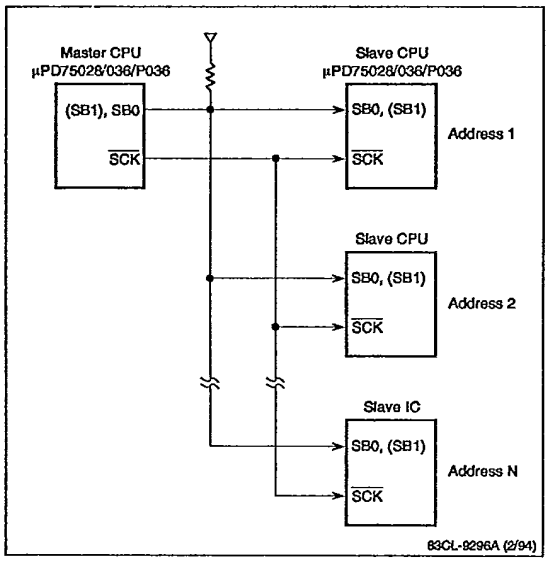


Figure 20. A/D Converter Block Diagram

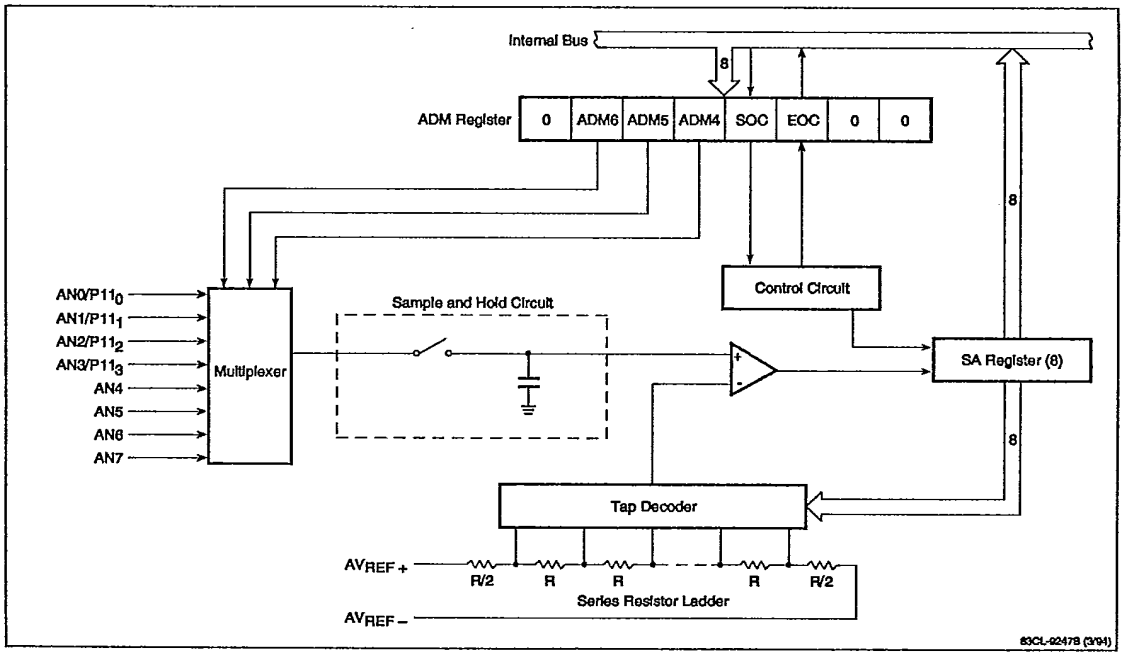


Figure 21. Interrupt Controller Block Diagram

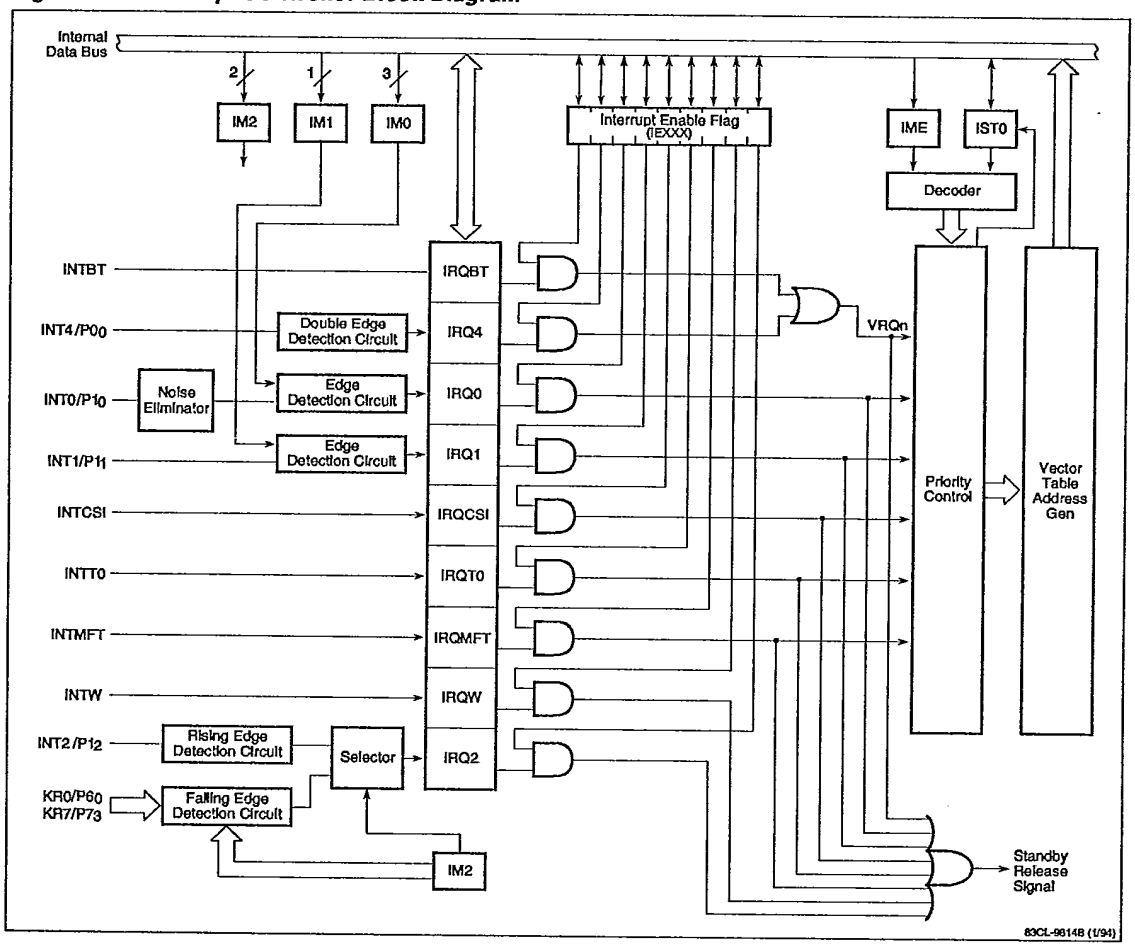


Table 5. Interrupt Sources

Interrupt Source	Internal/External	Interrupt Priority †	Vectored Interrupt Request (Table Address)
INTBT (Time reference interval signal from the basic interval timer)	Internal	1	VRQ1(0002H)
INT4 (Rising and falling edge detection)	External		
INT0 (Rising/falling edge detection)	External	2	VRQ2(0004H)
INT1 (Rising/falling edge detection)	External	3	VRQ3(0006H)

Table 5. Interrupt Sources (cont)

Interrupt Source	Internal/External	Interrupt Priority †	Vectored Interrupt Request (Table Address)
INTCSI (Serial data transfer end signal)	Internal	4	VRQ4(0008H)
INTT0 (Signal generated when programmable timer/event counter count register and modulo register coincide)	Internal	5	VRQ5(000AH)
INTMFT (Multifunction timer interrupt. Interrupt condition depends upon timer mode)	Internal	6	VRQ6(000CH)
INT2 (Rising edge input detection to INT2 pin or falling edge input detection to KR_0-KR_7)	External	Testable input signals (Tests whether IRQ2 or IRQW are set)	
INTW (Watch timer signal)	Internal		

† The interrupt priority determines the order when two or more simultaneous interrupts occur.

Standby Modes

The standby mode is summarized in table 6 and consists of three submodes.

HALT Mode. The HALT mode is entered by executing the HALT instruction. In this mode, the clock to the CPU is shut off (thus stopping the CPU), while all other parts of the chip, with the exception of INT0, remain fully functional.

STOP Mode. The STOP mode is entered by executing the STOP instruction. In this mode, the chip's main system oscillator is shut off, thereby stopping all portions of the chip except those that function off the subsystem clock. If the subsystem clock is used, it always remains on.

The HALT and STOP modes are released by a $\overline{\text{RESET}}$ or by any interrupt request except INT0.

Data Retention Mode. This mode may be entered after entering the STOP mode. Here, supply voltage V_{DD} may be lowered to 2 volts to further reduce power consumption. The contents of the RAM and registers are retained. This mode is released by first raising V_{DD} to the proper operating range, then releasing the STOP mode.

Reset

The state of the device after reset is summarized in table 7.

Table 6. Operation of the Standby Modes

Item	STOP Mode (STOP instruction when using main clock or SCC register when using subsystem clock)	HALT Mode (HALT instruction when using main or subsystem clock)
Clock oscillator	Only the main system clock oscillator is stopped.	Only CPU clock ϕ is stopped. Main and subsystem oscillators continue to operate.
Basic interval timer	Operation stops	Operation continues (IRQBT is set at reference time intervals).
Serial interface	Operates only when external $\overline{\text{SCK}}$ input is selected for serial clock.	Operational
Timer/event counter	Operates only when TIO pin input is selected for clock count.	Operational
Watch timer	Operation stops when using main system clock for timer. Operation continues when using subsystem clock for timer.	Operational
A/D converter	Operation stops	Operational

Table 6. Operation of the Standby Modes (cont)

Item	STOP Mode (STOP instruction when using main clock or SCC register when using subsystem clock)	HALT Mode (HALT instruction when using main or subsystem clock)
Multifunction timer	Operation stops	Operational
External interrupts	INT1, INT2, and INT4 operate. INT0 cannot operate.	All operational except INT0
CPU	Operation only from subsystem clock	Operation stops
Standby release signal	Enabled interrupt request signal (except INT0) or $\overline{\text{RESET}}$ input.	Enabled interrupt request signal (except INT0) or $\overline{\text{RESET}}$ input.

Table 7. State of the Device After Reset

Hardware		$\overline{\text{RESET}}$ Input During Standby Mode	$\overline{\text{RESET}}$ Input During Operation
Program counter (PC)	μPD75028/036	The low-order 5 bits of program memory address 0000H are loaded into PC12-PC8. The contents of address 0001H are loaded into PC7-PC0.	
	μPD75036/P036	The low-order 6 bits of program memory address 0000H are loaded into PC13-PC8. The contents of address 0001H are loaded into PC7-PC0.	
PSW	Carry flag (CY)	Held	Undefined
	Skip flags (SK0-SK2)	0	0
	Interrupt status flag (IST0)	0	0
	Memory bank enable flag (MBE)	Bit 7 of program memory address 0000H is loaded into MBE.	
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Held (Data memory address 0F8H-0FDH is undefined)	Undefined
General-purpose registers (X, A, H, L, D, E, B, C)		Held	Undefined
Memory bank selection register (MBS)		0	0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter	Counter (T0)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Watch timer	Mode register (WM)	0	0
Serial interface	Shift register (SIO)	Held	Undefined
	Operation mode register (CSIM)	0	0
	SBI control register (SBIC)	0	0
	Slave address register (SVA)	Held	Undefined

Table 7. State of the Device After Reset (cont)

Hardware		RESET Input During Standby Mode	RESET Input During Operation
Clock generator and clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
Interrupt function	Interrupt request flags (IRQxxx)	Reset to 0	Reset to 0
	Interrupt enable flags (IExxx)	0	0
	Interrupt master enable flag (IME)	0	0
	INT0, INT1, and INT2 and mode registers (IM0, IM1, and IM2)	0, 0, 0	0, 0, 0
Digital ports	Output buffers	Off	Off
	Output latches	Cleared to 0	Cleared to 0
	Input/output mode registers (PGMA, B, C)	0	0
	Pullup resistor specification register (POGA, POGB)	0	0
	Pulldown resistor register (PDGB)	0	0
Bit sequential buffer		Held	Undefined
Multifunction timer	Counter (MFTL)	FFH	FFH
	Counter (MFTH)	0	0
	Mode register (MFTM)	0	0
	Control register (MFTC)	0	0
A/D converter	Mode register (ADM)	04H	04H
	SA register (SA)	Unchanged	Undefined
Pins	$P0_0$-$P0_3$, $P1_0$-$P1_3$, $P2_0$-$P2_3$, $P3_0$-$P3_3$, $P6_0$-$P6_3$, $P7_0$-$P7_3$, $P8_0$-$P8_3$, $P9_0$-$P9_3$, $P11_0$-$P11_3$	Input	Input
	$P4_0$-$P4_3$, $P5_0$-$P5_3$, $P10_0$-$P10_3$	With internal pullup resistors: High level Open drain: High impedance	With internal pullup resistors: High level Open drain: High impedance

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = +25°C

Supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_{I1} (except ports 4, 5, 10)	−0.3 to V_{DD} + 0.3 V
Input voltage, V_{I2} (ports 4, 5, 10)	
With pullup resistor (75028/036 only)	−0.3 to V_{DD} + 0.3 V
Open drain	−0.3 to +11 V
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
High-level output current, I_{OH}	
Per pin	−10 mA
Total, all output pins	−30 mA
Low-level output current, I_{OL} †	
Per pin: ports 0, 3, 4, 5	30 mA peak, 15 mA rms
Per pin: except ports 0, 3, 4, 5	20 mA peak, 5 mA rms
Total: ports 0, 3 to 9, 11	170 mA peak, 120 mA rms (for 75028/P036)
Total: ports 3 to 9, 11	170 mA peak, 120 mA rms (μPD75036 only)
Total: ports 0, 2, 10	30 mA peak, 20 mA rms

Absolute Maximum Ratings (cont)

Operating temperature, T_{OPT}	−40 to +70°C (for 75028/P036 only)
Operating temperature, T_{OPT}	−40 to +85°C (for 75036 only)
Storage temperature, T_{STG}	−65 to +150°C

† Rms value = peak value x (duty cycle) $^{1/2}$

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC characteristics.

Capacitance

T_A = +25°C; V_{DD} = 0 V

Parameter	Symbol	Max	Unit	Conditions
Input capacitance	C_{IN}	15	pF	f = 1 MHz; unmeasured pins must be at 0 V
Output capacitance	C_{OUT}	15	pF	
Input/output capacitance	$C_{I/O}$	15	pF	

Main System Clock Oscillator

T_A = −40 to +70°C 75028/P036; T_A = −40 to +85°C 75036; V_{DD} = 2.7 to 6.0 V; refer to figures 22 and 23.

Type	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Ceramic resonator (figure 23A)	Frequency (Note 1)	f_X	2.0		5.0	MHz	μPD75028/P036
			1.0	4.19	5.0	MHz	μPD75036
	Oscillator stabilization time (Note 2)				4.0 (Note 3)	ms	After V_{DD} reaches the minimum value of the oscillator operating voltage range.
Crystal resonator (figure 23A)	Frequency (Note 1)	f_X	2.0	4.19	5.0	MHz	μPD75028/P036
			1.0	4.19	5.0	MHz	μPD75036
	Oscillator stabilization time (Note 2)				10 (Note 3)	ms	V_{DD} = 4.5 to V_{DD} max
					30 (Note 3)	ms	V_{DD} = 2.7 to 6.0 V
External clock (figure 23B)	X1 input frequency (Note 1)	f_X	2.0		5.0	MHz	μPD75028/P036
			1.0	4.19	5.0	MHz	μPD75036
	X1 input high/low level width	t_{XH}, t_{XL}	100		250	ns	μPD75028/P036
			100		500	ns	μPD75036

Notes:

(1) Oscillator and X1 input frequencies are shown only to present the oscillator characteristics. Refer to the AC Characteristics table for instruction execution time.

(2) Time required for oscillator to stabilize after V_{DD} min is reached or time after release of STOP mode.

(3) Values shown are for NEC approved resonators. Values for resonators not tested by NEC should be obtained from resonator manufacturer's spec sheets.

Subsystem Clock Oscillator

T_A = −40 to +70°C 75028/P036; T_A = −40 to +85°C 75036; V_{DD} = 2.7 to 6.0 V; refer to figures 22 and 24.

Type	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Crystal resonator (figure 24A)	Frequency	f_{XT}	32	32.768	35	kHz	
	Oscillator stabilization time (Note 1)			1.0	2	s	V_{DD} = 4.5 to V_{DD} max
					10	s	V_{DD} = 2.7 to 6.0 V
External clock (figure 24B)	XT1 input frequency	f_{XT}	32		100	kHz	
	XT1 input high/low level width	t_{XTH}, t_{XTL}	5		15	μs	

Note:

(1) Values shown are for NEC approved crystals. Values for crystals not tested by NEC should be obtained from crystal manufacturer's specification sheets.

Figure 22. Clock Oscillator Timing Measurements

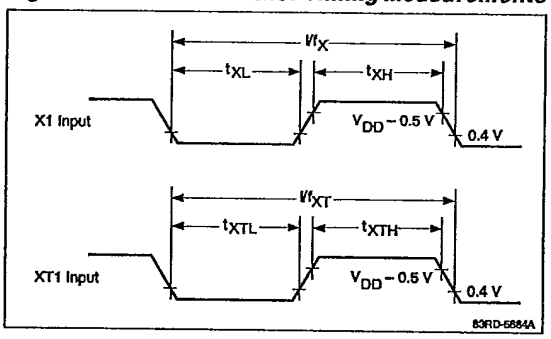


Figure 23. Main System Clock Configurations

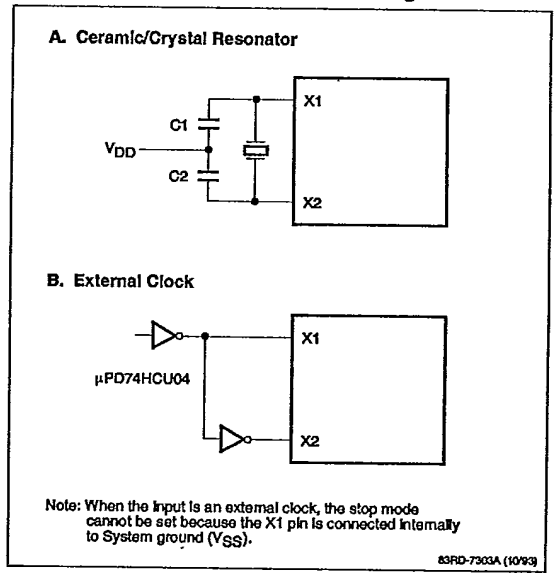
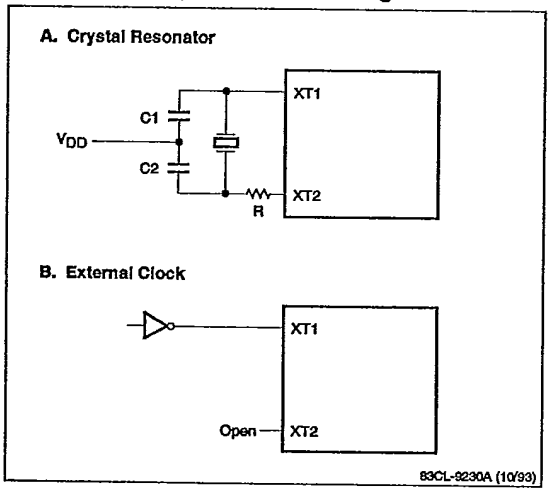


Figure 24. Subsystem Clock Configurations



DC Characteristics

T_A = −40 to +70°C 75028/P036; T_A = −40 to +85°C 75036; V_{DD} = 2.7 to 6.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Ports 2, 3, 8, 9, 11
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	Ports 0, 1, 6, 7, and $\overline{\text{RESET}}$ pin
	V_{IH3}	0.7 V_{DD}		V_{DD}	V	Ports 4, 5, 10 with internal pullup resistor (75028/036 only)
		0.7 V_{DD}		10	V	Ports 4, 5, 10 with open drain
	V_{IH4}	V_{DD} − 0.5		V_{DD}	V	X1, X2, XT1, XT2
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	Ports 2 to 5 and 8 to 11
	V_{IL2}	0		0.2 V_{DD}	V	Ports 0, 1, 6, 7, and $\overline{\text{RESET}}$ pin
	V_{IL3}	0		0.4	V	X1, X2, XT1, XT2
High-level output voltage	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 4.5 to 6.0 V; I_{OH} = −1 mA
		V_{DD} − 0.5			V	I_{OH} = −100 μA.
Low-level output voltage	V_{OL}		0.4	2.0	V	Ports 3, 4, 5; V_{DD} = 4.5 to 6.0 V; I_{OL} = 15 mA, 75028/P036
			0.5	2.0	V	Ports 3, 4, 5; V_{DD} = 4.5 to 6.0 V; I_{OL} = 15 mA μPD75036
				0.4	V	V_{DD} = 4.5 to 6.0 V; I_{OL} = 1.6 mA
				0.5	V	I_{OL} = 400 μA
				0.2 V_{DD}	V	SB0, SB1; open drain with pullup resistor ≥ 1 kΩ
High-level input leakage current	I_{LIH1}			3	μA	V_{IN} = V_{DD}; except X1, X2, XT1, XT2
	I_{LIH2}			20	μA	V_{IN} = V_{DD}; X1, X2, XT1, XT2
	I_{LIH3}			20	μA	V_O = 9 V for 75028/P036 V_O = 10 V for 75036
Low-level input leakage current	I_{LIL1}			−3	μA	V_{IN} = 0 V; except X1, X2, XT1, XT2
	I_{LIL2}			−20	μA	V_{IN} = 0 V; X1, X2, XT1, XT2
High-level output leakage current	I_{LOH1}			3	μA	V_{OUT} = V_{DD}; except ports 4, 5, 10
	I_{LOH2}			20	μA	V_{OUT} = 9 V; ports 4, 5, 10 with open drain
Low-level output leakage current	I_{LOL}			−3	μA	V_{OUT} = 0 V
Internal pullup resistor	R_{U1}	15	40	80	kΩ	Ports 0, 1, 2, 3, 6, 7, 8 (except $P0_0$); V_{IN} = 0 V; V_{DD} = 5.0 V ±10%
		30		300	kΩ	Ports 0, 1, 2, 3, 6, 7, 8 (except $P0_0$); V_{IN} = 0 V; V_{DD} = 3.0 V ±10%
	R_{U2} (75028/036 only)	15	40	70	kΩ	Ports 4, 5, 10; V_{OUT} = V_{DD} − 2.0 V; V_{DD} = 5.0 V ±10%
		10		60	kΩ	Ports 4, 5, 10; V_{OUT} = V_{DD} − 2.0 V; V_{DD} = 3.0 V ±10%.
Internal pulldown resistor	R_D	10	40	70	kΩ	Port 9; V_{IN} = V_{DD}; V_{DD} = 5.0 V ±10%
		10		60	kΩ	Port 9; V_{IN} = V_{DD}; V_{DD} = 3.0 V ±10%

DC Characteristics (cont)

Parameter	Symbol		Min	Typ	Max	Unit	Conditions
Supply current (Note 1)	I_{DD1} (Note 2)	*		2.5	8	mA	4.19-MHz crystal oscillator (C1, C2 = 22 pF); V_{DD} = 5 V ±10%; Note 3
		†		3.2	10	mA	
		‡		4.5	14	mA	
		*		0.35	1.2	mA	4.19-MHz crystal oscillator (C1, C2 = 22 pF); V_{DD} = 3 V ±10%; Note 4
		†		0.25	0.75	mA	
		‡		0.9	3	mA	
	I_{DD2} (Note 2)	*		500	1500	μA	4.19-MHz crystal oscillator (C1, C2 = 22 pF); HALT mode; V_{DD} = 5 V ±10%
		‡		700	2100	μA	
		*		150	450	μA	4.19-MHz crystal oscillator (C1, C2 = 22 pF); HALT mode; V_{DD} = 3 V ±10%
		‡		300	900	μA	
	I_{DD3} (Note 5)	*		30	90	μA	32.768-kHz crystal oscillator; V_{DD} = 3 V ±10%; Note 6
		†		15	45	μA	
		‡		100	300		
	I_{DD4} (Note 5)	*		5	15	μA	32.768-kHz crystal oscillator; V_{DD} = 3 V ±10%; HALT mode; Note 7
		‡		20	60	μA	
	I_{DD5}			0.5	20	μA	XT1 = 0 V; STOP mode; V_{DD} = 5 V±10%
				0.1	10	μA	XT1 = 0 V; STOP mode; V_{DD} = 3 V ±10%
				0.1	5	μA	XT1 = 0 V; STOP mode; V_{DD} = 3 V ±10%; T_A = 25°C
	I_{DD6} (Note 8)			5	15		32.768-kHz crystal oscillator; STOP mode; V_{DD} = 3 V ±10%

* 75028/036; † 75036 ‡ 75P036

Notes:

(1) Does not include internal pullup resistor current.

(2) Includes subsystem clock current.

(3) When operated in the high-speed mode with the processor clock control register (PCC) set to 0011.

(4) When operated in the low-speed mode with PCC set to 0000.

(5) SCC register used to select subsystem clock and stop main system clock; system clock control register (SCC) bits SCC3 = 1 and SCC0 = 1.

(6) CPU operating from subsystem clock and main system clock stopped.

(7) Subsystem clock operating with CPU halted and main system clock stopped.

(8) STOP instruction stops main system clock and subsystem clock is running.

AC Characteristics

T_A = −40 to +70°C 75028/P036; T_A = −40 to +85°C 75036; V_{DD} = 2.7 to 6.0 V; refer to figures 25 through 27

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Cycle time (Note 1)	t_{CY}	†0.95 ‡0.95		32 64	μs	Operation with main system clock. V_{DD} = 4.5 to 6.0 V
		†3.8 ‡0.95		32 64	μs	Operation with main system clock.
		114	122	125	μs	Operation with subsystem clock.
TIO input frequency	f_{TI}	0		1	MHz	V_{DD} = 4.5 to 6.0 V
		0		275	kHz	
TIO input, low- and high-level width	t_{TIL}, t_{TIH}	0.48			μs	V_{DD} = 4.5 to 6.0 V
		1.8			μs	
Interrupt input, low- and high-level width	t_{INTL}, t_{INTH}	(Note 2)			μs	INT0
		10			μs	INT1, 2, 4
		10			μs	KR_0 to KR_7
$\overline{RESET}$ low-level width	t_{RSL}	10			μs	After V_{DD} ≥ 2.7 V

† = 75028/P036; ‡ = 75036

Notes:

(1) Cycle time (minimum instruction execution time) is determined by the frequency of the oscillator connected to the microcontroller, the system clock control register (SCC), and the processor clock control register (PCC)

(2) $2t_{CY}$ or $128/f_X$, depending on the setting of the interrupt mode register (IM0).

Figure 25. AC Timing Measurements

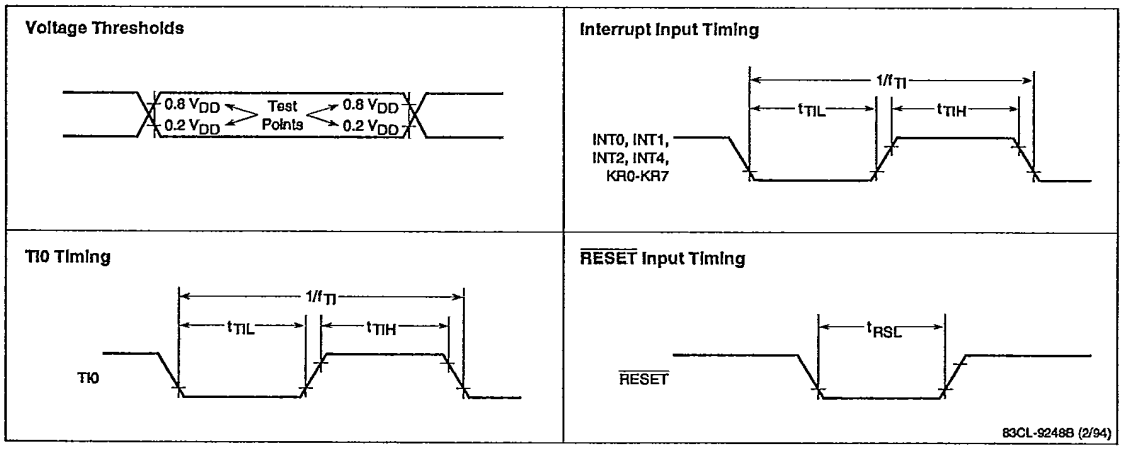


Figure 26. Main System Clock Operation t_{CY} vs V_{DD} (μPD75028/P036 only)

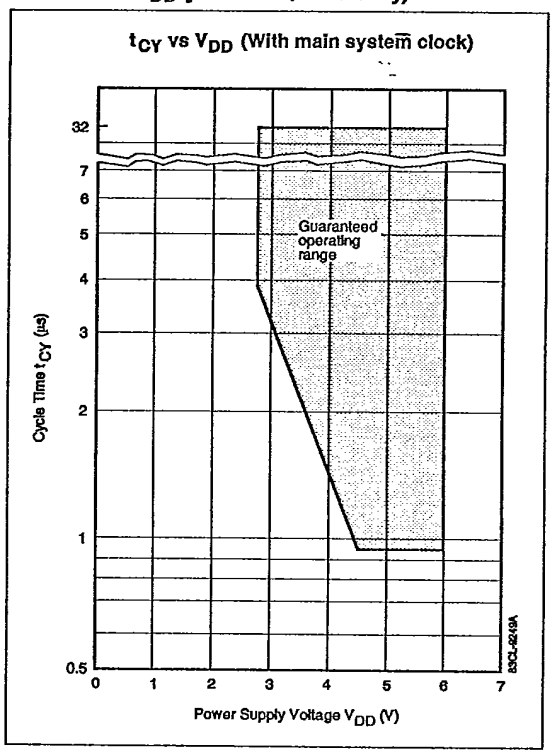


Figure 27. Main System Clock Operation t_{CY} vs V_{DD} (μPD75036 only)

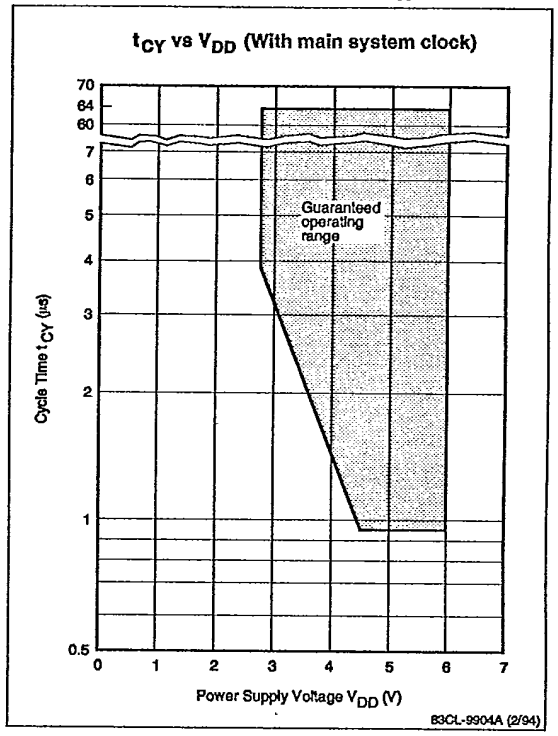
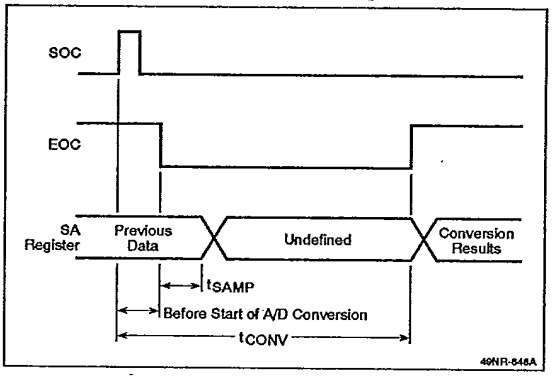


Figure 28. A/D Conversion Timing



A/D Converter Characteristics

T_A = −40 to +70°C 75028/P036; T_A = −40 to +85°C 75036; V_{DD} = 2.7 to 6.0 V; AV_{SS} = V_{SS} = 0 V; refer to figure 28

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Resolution		8	8	8	bits	
Absolute accuracy (Note 1) 2.5 V ≤ AV_{REF+} ≤ V_{DD}				±1.5	LSB	T_A = −10 to +70°C 75028/P036
				±1.5	LSB	T_A = −10 to +85°C 75036
				±2.0	LSB	T_A = −40 to −10°C
Conversion time (Note 2)	t_{CONV}			168/f_X	μs	
Sampling time (Note 3)	t_{SAMP}			44/f_X	μs	
Analog input voltage	V_{IAN}	AV_{REF-}		AV_{REF+}	V	
Analog supply voltage	AV_{DD}	2.5		V_{DD}	V	
Reference input voltage	AV_{REF+}	2.5		AV_{DD}	V	2.5 V ≤ (AV_{REF+}) − (AV_{REF-})
Reference input voltage	AV_{REF-}	0		1.0	V	
Analog input impedance	R_{AN}		1000		MΩ	
AV_{REF} current	I_{AREF}		0.25 (75028)	2.0	mA	
			1.0 (75036)	2.0	mA	
			0.35 (75P036)	2.0	mA	

Notes:

(1) The absolute accuracy does not include the quantization error (±1/2 LSB).

(2) The total conversion time until EOC = 1 is 40.1 μs at f_X = 4.19 MHz.

(3) The time until completion of sampling is 10.5 μs (f_X = 4.19 MHz). Note that the sampling time value t_{SAMP} is included in the total conversion time value t_{CONV}.

Serial Interface, 2/3-Line; Internal $\overline{SCK}$ Output

T_A = −40 to +70°C 75028/P036; T_A = −40 to +85°C 75036; V_{DD} = 2.7 to 6.0 V; refer to figure 29

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY1}	1600			ns	V_{DD} = 4.5 to 6.0 V
		3800			ns	
$\overline{SCK}$ low- and high-level width	t_{KL1}, t_{KH1}	0.5t_{KCY1} − 50			ns	V_{DD} = 4.5 to 6.0 V
		0.5t_{KCY1} − 150			ns	
SI setup time to $\overline{SCK}$ ↑	t_{SIK1}	150			ns	
SI hold time from $\overline{SCK}$ ↑	t_{KSI1}	400			ns	
$\overline{SCK}$ ↓ to SO output delay time (Note 1)	t_{KSO1}			250	ns	V_{DD} = 4.5 to 6.0 V
				1000	ns	

Note: (1) Output load R_L = 1 kΩ and C_L = 100 pF.

Serial Interface, 2/3-Line; External $\overline{SCK}$ Input

T_A = −40 to +70°C 75028/P036; T_A = −40 to +85°C 75036; V_{DD} = 2.7 to 6.0 V; refer to figure 29

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY2}	800			ns	V_{DD} = 4.5 to 6.0 V
		3200			ns	
$\overline{SCK}$ low- and high-level width	t_{KL2}, t_{KH2}	400			ns	V_{DD} = 4.5 to 6.0 V
		1600			ns	
SI setup time to $\overline{SCK}$ ↑	t_{SIK2}	100			ns	
SI hold time from $\overline{SCK}$ ↑	t_{KSI2}	400			ns	
$\overline{SCK}$ ↓ to SO output delay time (Note 1)	t_{KSO2}			300	ns	V_{DD} = 4.5 to 6.0 V
				1000	ns	

Note: (1) Output load R_L = 1 kΩ and C_L = 100 pF.

Serial Interface, SBI Mode; Internal $\overline{SCK}$ Output (Master)

T_A = −40 to +70°C 75028/P036; T_A = −40 to +85°C 75036; V_{DD} = 2.7 to 6.0 V; refer to figure 30

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY3}	1600			ns	V_{DD} = 4.5 to 6.0 V
		3800			ns	
$\overline{SCK}$ low- and high-level width	t_{KL3}, t_{KH3}	$0.5t_{KCY3}$ − 50			ns	V_{DD} = 4.5 to 6.0 V
		$0.5t_{KCY3}$ − 150			ns	
SB0, SB1 setup time to $\overline{SCK}$ ↑	t_{SIK3}	150			ns	
SB0, SB1 hold time from $\overline{SCK}$ ↑	t_{KSI3}	0.5 t_{KCY3}			ns	
$\overline{SCK}$ ↓ to SBO, SB1 output delay time (Note 1)	t_{KSO3}	0		250	ns	V_{DD} = 4.5 to 6.0 V
		0		1000	ns	
$\overline{SCK}$ ↑ to SB0, SB1 ↓	t_{KSB}	t_{KCY3}			ns	
SB0, SB1 ↓ to $\overline{SCK}$ ↓	t_{SBK}	t_{KCY3}			ns	
SB0, SB1 low-level width	t_{SBL}	t_{KCY3}			ns	
SB0, SB1 high-level width	t_{SBH}	t_{KCY3}			ns	

Note: (1) Output load R_L = 1 kΩ and C_L = 100 pF.

Serial Interface, SBI Mode; External $\overline{SCK}$ Input (Slave)

T_A = −40 to +70°C 75028/P036; T_A = −40 to +85°C 75036; V_{DD} = 2.7 to 6.0 V; refer to figure 30

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY4}	800			ns	V_{DD} = 4.5 to 6.0 V
		3200			ns	
$\overline{SCK}$ low- and high-level width	t_{KL4}, t_{KH4}	400			ns	V_{DD} = 4.5 to 6.0 V
		1600			ns	
SB0, SB1 setup time to $\overline{SCK}$ ↑	t_{SIK4}	100			ns	
SB0, SB1 hold time from $\overline{SCK}$ ↑	t_{KSI4}	$0.5t_{KCY4}$			ns	
$\overline{SCK}$ ↓ to SB0, SB1 output delay time (Note 1)	t_{KSO4}	0		300	ns	V_{DD} = 4.5 to 6.0 V
		0		1000	ns	
$\overline{SCK}$ ↑ to SB0, SB1 ↓	t_{KSB}	t_{KCY4}			ns	
SB0, SB1 ↓ to $\overline{SCK}$ ↓	t_{SBK}	t_{KCY4}			ns	
SB0, SB1 low-level width	t_{SBL}	t_{KCY4}			ns	
SB0, SB1 high-level width	t_{SBH}	t_{KCY4}			ns	

Note: (1) Output load R_L = 1 kΩ and C_L = 100 pF.

Data Memory STOP Mode; Low-Voltage Data Retention

T_A = −40 to +70°C 75028/P036; T_A = −40 to +85°C 75036; refer to figure 31

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.0		6.0	V	
Data retention current (Note 1)	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2.0 V
Release signal set time	t_{SREL}	0			μs	
Oscillation stabilization time (Note 2)	t_{WAIT}		(Notes 3, 4)		ms	Release by $\overline{RESET}$ input
			(Note 3)		ms	Release by interrupt request

Notes:

(1) Internal pullup resistor current is not included.

(2) Oscillation stabilization WAIT time is the time during which the CPU is stopped and the crystal is stabilizing. This time is required to prevent unstable operation while the oscillator is stabilizing. The interval timer can be used to delay the CPU from executing instructions by using the basic interval timer mode register (BTM) according to the following table:

BTM3	BTM2	BTM1	BTM0	WAIT Time (f_X = 4.19 MHz)
–	0	0	0	$2^{20}/f_X$ (250 ms approx)
–	0	1	1	$2^{17}/f_X$ (31.3 ms approx)
–	1	0	1	$2^{15}/f_X$ (7.82 ms approx)
–	1	1	1	$2^{13}/f_X$ (1.95 ms approx)

(3) Consult the manufacturer's resonator specification sheet for this value.

(4) The interval timer will cause a delay of $2^{17}/f_X$ seconds after a reset.

Figure 29. Serial Interface Timing; 2/3-Line

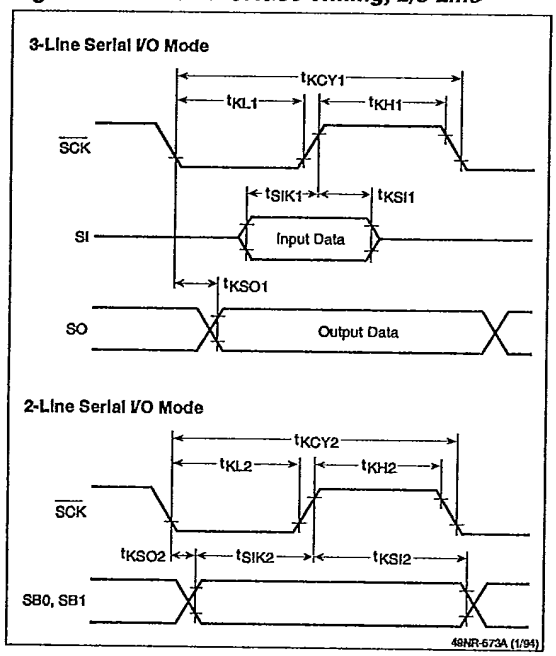


Figure 30. Serial Interface Timing; SBI Mode

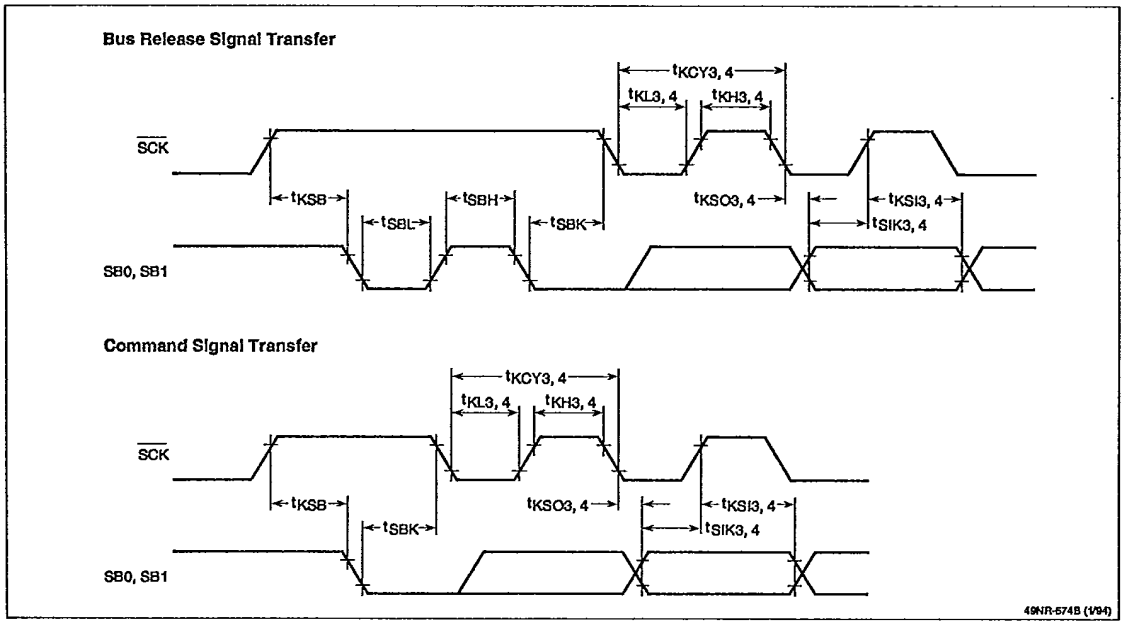
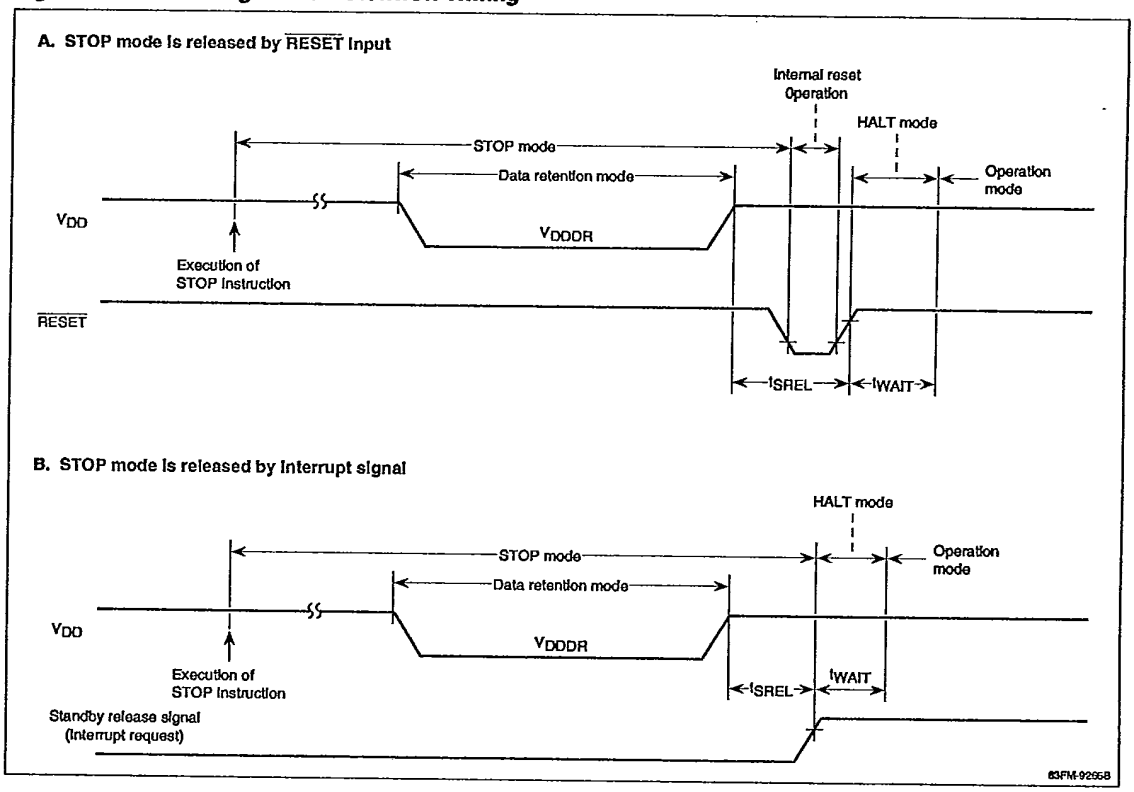


Figure 31. Low-Voltage Data Retention Timing



OTP PROGRAM MEMORY

The μPD75P036 contains 16,256 x 8 bits of one-time programmable (OTP) program memory. The memory is programmed by the pins listed in table 8. During programming, addresses are incremented by applying clock pulses to the X1 input.

Table 8. Program Memory Access

Pin	Function
V_{PP}	OTP Programming voltage pin (normally V_{DD})
X1, X2	Address increment clock input during programming. The inverted signal of X1 must be input at X2.
MD_0-MD_3	Mode selection during OTP programming
$P4_0$-$P4_3$	Low-order 4-bit data I/O during programming.
$P5_0$-$P5_3$	High-order 4-bit data I/O during programming.
V_{DD}	Supply voltage 2.7 to 6 volts during normal operation; 6 volts during programming.

Note: Because the μPD75P036 has no erasure window, program memory data cannot be erased with ultraviolet light.

OTM Operation Modes

The μPD75P036 operates in the program memory write/verify mode when +6 V is applied to V_{DD} and +12.5 V to V_{PP}. Mode pins MD_0-MD_3 select the operation modes shown in table 9.

Table 9. Program Memory Mode Selection

V_{PP} = +12.5 V; V_{DD} = +6 V

MD_0	MD_1	MD_2	MD_3	Operation Mode
H	L	H	L	Program memory address clear
L	H	H	H	Program memory write
L	L	H	H	Program memory verify
H	X	H	H	Program inhibit

X = L or H.

Program Memory Write and Verify.

The program memory write/verify procedure follows. Refer to the timing diagram, figure 32.

(1) Connect unused pins to V_{SS} through a pulldown resistor. Hold X1 low.

(2) Supply +5 V to V_{DD} and V_{PP}.

(3) Wait 10 μs.

(4) Select program memory address clear mode.

(5) Change voltage on V_{DD} to +6 V and on V_{PP} to +12.5 V.

(6) Select program inhibit mode.

(7) Write data in the 1-ms write mode.

(8) Select program inhibit mode.

(9) Select verify mode. If data is written correctly, proceed to step 10; if data is not written correctly, repeat steps 7-9 up to 20 times. If data is still incorrect after 20 tries, terminate programming and declare the device defective.

(10) Perform one additional write with an MD_0 pulse width (in ms) equal to the number of writes performed in step 7 times 1 msec. For example, MD_0 = 10 ms if the location has been written to 10 times.

(11) Select program inhibit mode.

(12) Increment program memory address by one by inputting four pulses to X1.

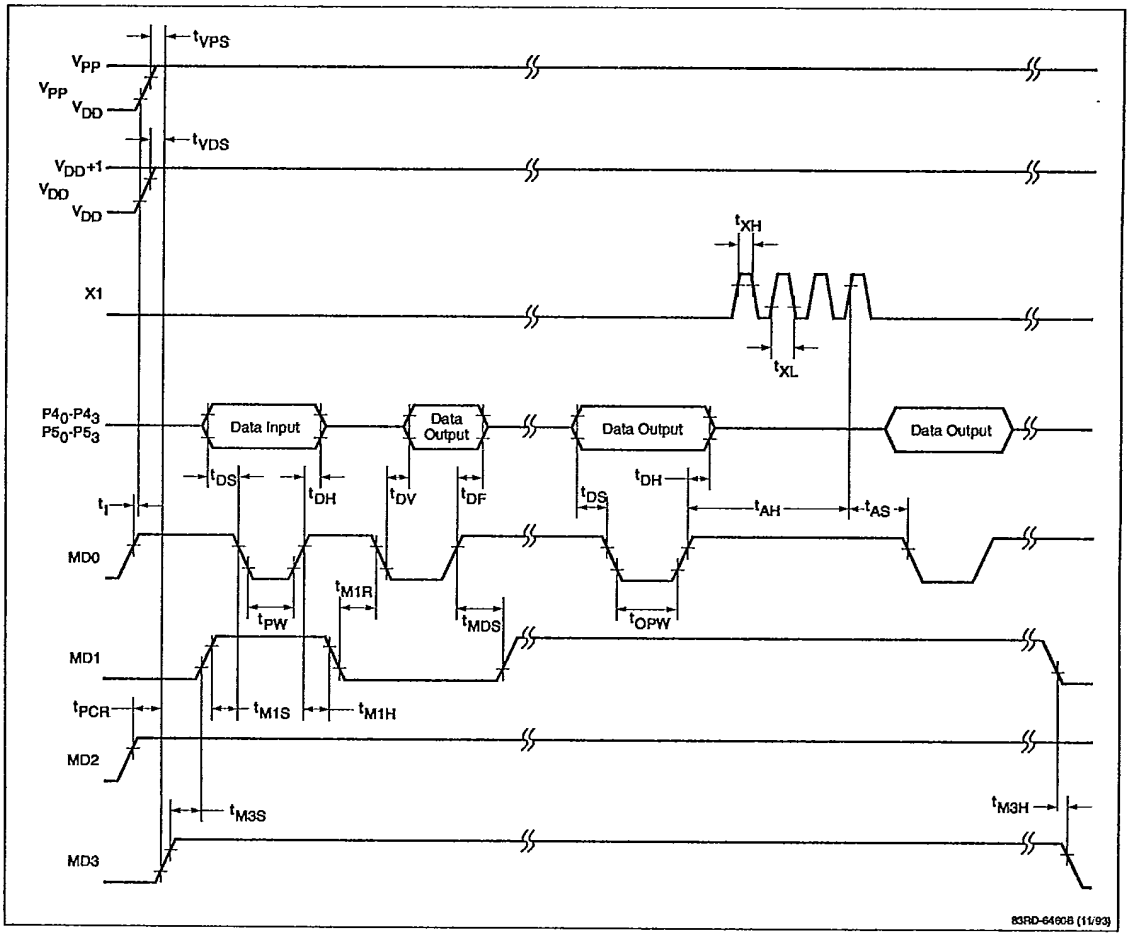
(13) Repeat steps 7-12 until the end address occurs.

(14) Select program memory address clear mode.

(15) Change voltage on V_{DD} and V_{PP} to +5 V.

(16) Turn off power.

Figure 32. Timing Diagram for Program Memory Write/Verify



Program Memory Read

The program memory read procedure follows. Refer to the timing diagram, figure 33.

(1) Connect unused pins to V_{SS} through a pulldown resistor. Hold X1 low.

(2) Supply +5 V to V_{DD} and V_{PP}.

(3) Wait 10 μs.

(4) Select program memory address clear mode.

(5) Change voltage on V_{DD} to +6 V and on V_{PP} to +12.5 V.

(6) Select program inhibit mode.

(7) Select verify mode. When four clock pulses are input to X1, data from one address is output.

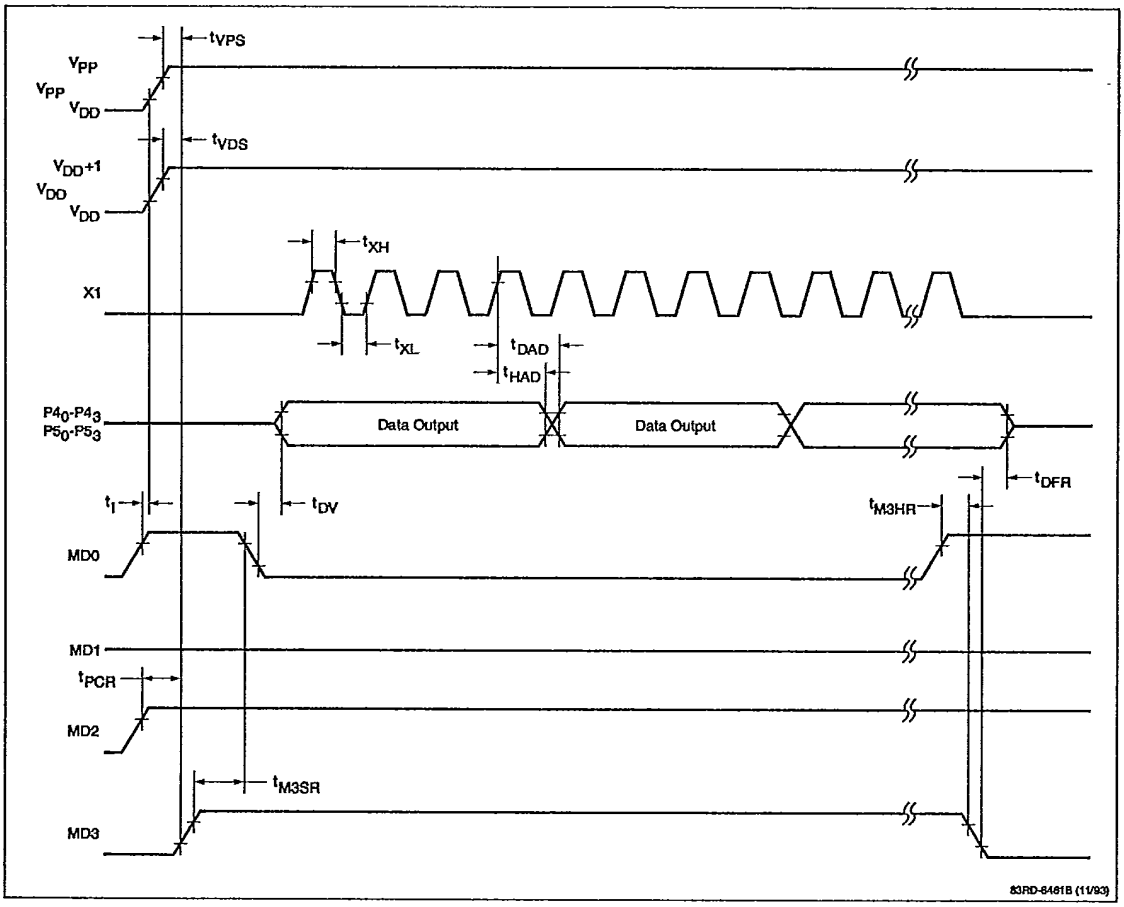
(8) Select program inhibit mode.

(9) Select program memory address clear mode.

(10) Change voltage on V_{DD} and V_{PP} to +5 V.

(11) Turn off power.

Figure 33. Timing Diagram for Program Memory Read



DC Programming; μPD75P036

T_A = 25 ±5°C; V_{DD} = 6.0 ±0.25 V; V_{PP} = 12.5 ±0.3 V; V_{SS} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}	V_{DD}		V	All except X1, X2
	V_{IH2}	V_{DD} – 0.5	V_{DD}		V	X1, X2
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	All except X1, X2
	V_{IL2}	0		0.4	V	X1, X2
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-level output voltage	V_{OH}	V_{DD} – 1.0			V	I_{OH} = 1 MA
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} supply current	I_{DD}			30	mA	
V_{PP} supply current	I_{PP}			30	mA	MD0 = V_{IL}; MD1 = V_{IH}

Notes:

(1) V_{PP} must not exceed + 13.5 V, including overshoot.

(2) V_{DD} must be applied before V_{PP} and turned off after V_{PP} is removed.

AC Programming; μPD75P036

T_A = 25 ±5°C; V_{DD} = 6.0 ±0.25 V; V_{PP} = 12.5 ±0.3 V; V_{SS} = 0 V; refer to figures 32 and 33.

Parameter	Symbol	(Note 1)	Min	Max	Unit	Conditions
X1 input frequency	f_X			4.19	MHz	
Address hold from MD0 ↑ (Note 2)	t_{AH}	t_{AH}	2		μs	
Address setup time (Note 2)	t_{AS}	t_{AS}	2		μs	
Data delay from address (Note 2)	t_{DAD}	t_{ACC}	2		μs	
Data output float delay from MD0 ↑	t_{DF}	t_{DF}	0	130	ns	
Data output float delay from MD3 ↓	t_{DFR}		2		μs	
Data hold from MD0 ↑	t_{DH}	t_{DH}	2		μs	
Data to MD0 ↓ setup	t_{DS}	t_{DS}	2		μs	
Data output delay from MD0 ↓	t_{DV}	t_{DV}		1	μs	MD0 = MD1 = V_{IL}
Data output hold from address (Note 2)	t_{HAD}	t_{OH}	0	130	μs	
Initial mode set	t_I		2		μs	
MD1 hold to MD0 ↑	t_{M1H}	t_{OEH}	2		μs	t_{M1H} + t_{M1R} ≥ 50 μs
MD1 recovery from MD0 ↓	t_{M1R}	t_{OR}	2		μs	t_{M1H} + t_{M1R} ≥ 50 μs
MD1 to MD0 ↓ setup	t_{M1S}	t_{OES}	2		μs	
MD3 hold from MD1 ↓	t_{M3H}		2		μs	
MD3 output hold from MD0 ↑	t_{M3HR}		2		μs	
MD3 setup to MD1 ↑	t_{M3S}		2		μs	
MD3 setup to MD0 ↓	t_{M3SR}		2		μs	During program read cycle
MD0 setup to MD1 ↑	t_{MOS}	t_{CES}	2		μs	
Additional program pulse width	t_{OPW}	t_{OPW}	0.95	21	ms	
Program counter reset	t_{PCR}		10		μs	
Initialized program pulse width	t_{PW}	t_{PW}	0.95	1.05	ms	
V_{DD} setup to MD3 ↑	t_{VDS}	t_{VCS}	2		μs	
V_{PP} setup to MD3 ↑	t_{VPS}	t_{VPS}	2		μs	

AC Programming; μPD75P036 (cont)

Parameter	Symbol	(Note 1)	Min	Max	Unit	Conditions
X1 input low- and high-level width	t_{XH}, t_{XL}		0.125		μs	

Notes:

(1) These symbols correspond to those of the μPD27C256 EPROM

(2) The internal address signal is incremented by the rising edge of the fourth X1 pulse; it is not connected to an external pin.

SOLDERING

Packaging and Soldering Information

Part Number	Package	Package Drawing	Recommended Soldering Code
μPD75028CW-xxx μPD75036CW-xxx μPD75P036CW	64-pin plastic shrink DIP	P64C-70-750A, C	WS60-00-1
μPD75028GC-xxx-AB8 μPD75036GC-xxx-AB8 μPD75P036GC-AB8	64-pin plastic QFP	P64GC-80-AB8-3	IR30-107-1, VP15-107-1, WS60-107-1

Soldering Conditions

Method (Note 1)	Code (Note 2)	Soldering Conditions	Exposure Limit (Note 3)
Infrared reflow	IR30-107-1	Package peak temp: 230°C Time: 30 sec max (210°C min)	Max no. of days: 7 (thereafter, 10 hours baking at 125°C is required)
Vapor phase	VP15-107-1	Package peak temp: 215°C Time: 40 sec max (200°C min)	Max no. of days: 7 (thereafter, 10 hours baking at 125°C is required)
Wave soldering	WS60-00-1	Solder bath temp: 260°C max Time: 10 sec max Preheating temp: 120°C max (package surface temp)	No limit
	WS60-107-1		Max no. of days: 7 (thereafter, 10 hours baking at 125°C is required)
Pin partial heating (SDIP)		Temperature: 260°C max Time: 10 sec max (per device side)	
Pin partial heating (QFP)		Temperature: 300°C max Time: 3 sec max (per device side)	

Notes:

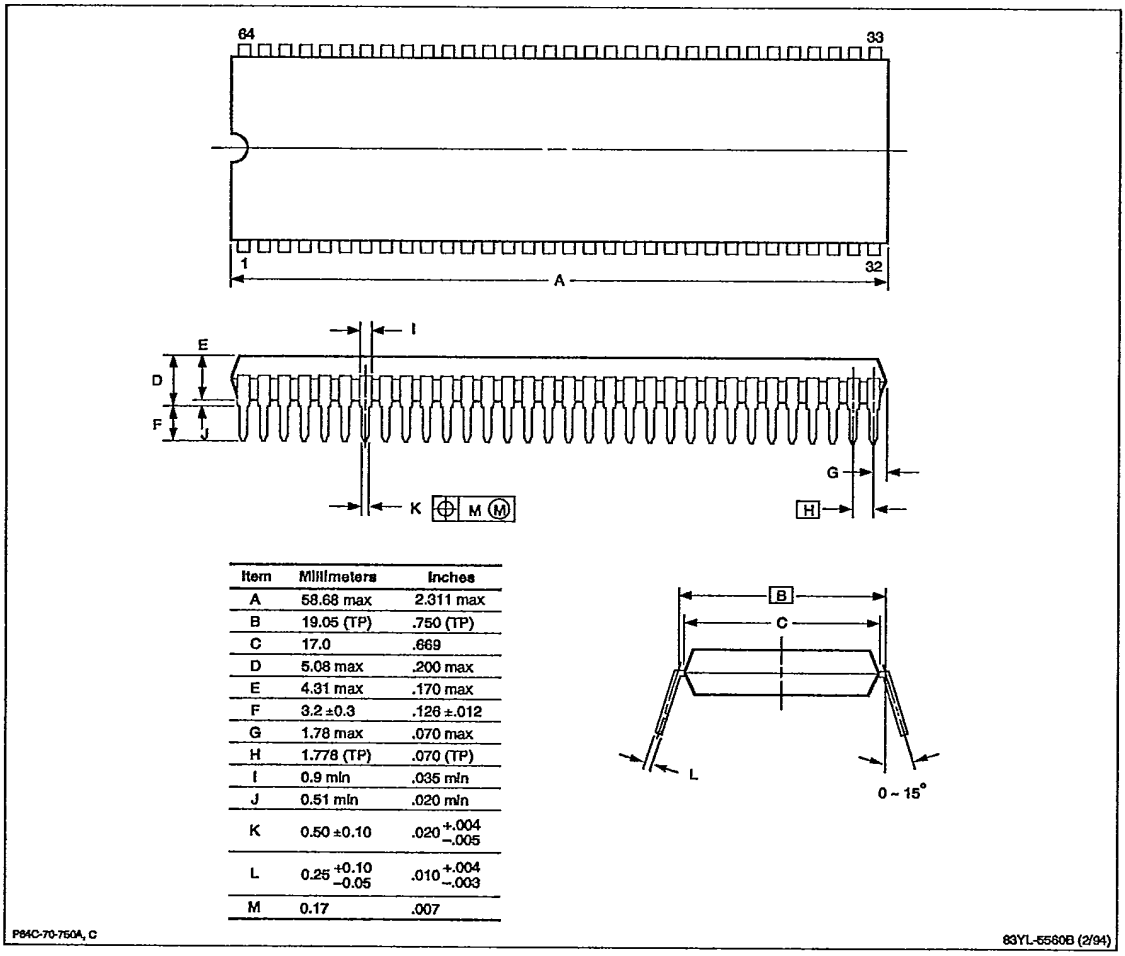
(1) Do not use different soldering methods together. However, on all devices the pin partial heating soldering method can be used alone on in combination with other soldering methods.

(2) The maximum number of soldering operations is one or two as indicated by the last digit of the soldering code: –1 or –2.

(3) Maximum no. of days refers to number of days after unpacking the dry pack. Storage conditions are 25°C and 65% RH max.

PACKAGE DRAWINGS

64-Pin Plastic Shrink DIP (750-mil)



Item	Millimeters	Inches
A	58.68 max	2.311 max
B	19.05 (TP)	.750 (TP)
C	17.0	.669
D	5.08 max	.200 max
E	4.31 max	.170 max
F	3.2 ±0.3	.126 ±.012
G	1.78 max	.070 max
H	1.778 (TP)	.070 (TP)
I	0.9 min	.035 min
J	0.51 min	.020 min
K	0.50 ±0.10	$.020^{+.004}_{-.005}$
L	$0.25^{+0.10}_{-0.05}$	$.010^{+.004}_{-.003}$
M	0.17	.007

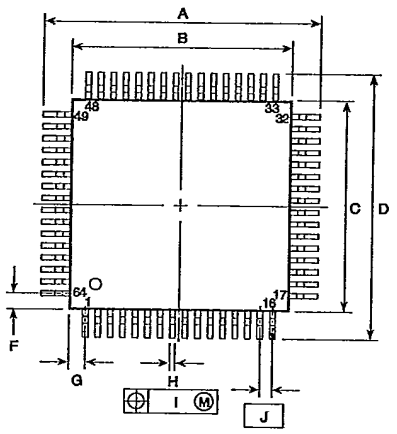
P64C-70-750A, C

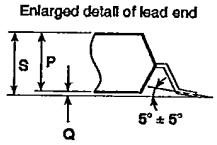
83YL-5560B (2/94)

64-Pin Plastic QFP (14 x 14 mm)

Item	Millimeters	Inches
A	17.6 ± 0.4	.693 ± .016
B	14.0 ± 0.2	.551 +.009 −.008
C	14.0 ± 0.2	.551 +.009 −.008
D	17.6 ± 0.4	.693 ± .016
F	1.0	.039
G	1.0	.039
H	0.35 ± 0.10	.014 +.004 −.005
I	0.15	.006
J	0.8 (TP)	.031 (TP)
K	1.8 ± 0.2	.071 ± .008
L	0.8 ± 0.2	.031 +.009 −.008
M	0.15 +0.10 −0.05	.006 +.004 −.003
N	0.10	.004
P	2.55	.100
Q	0.1 ± 0.1	.004 ± .004
S	2.85 max	.112 max

Note:
Each lead centerline is located within 0.15 mm (.006 inch) of its true position (TP) at maximum material condition.





P64GC-80-AB8-3

49NR-6898 (3/94)