TPS3613-01
ADJUSTABLE BATTERY-BACKUP SUPERVISOR FOR RAM RETENTION

SLVS340 – DECEMBER 2000

- **Supply Current of 40 µA (Max)**
- **Battery Supply Current of 100 nA (Max)**
- **Supply Voltage Supervision Range:**
  - **Adjustable**
  - **Other Versions Available on Request**
- **Backup-Battery Voltage Can Exceed V_{DD}**
- **Power-On Reset Generator With Fixed 100-ms Reset Delay Time**
- **Active-High and Active-Low Reset Output**
- **Chip-Enable Gating . . . 3 ns (at V_{DD} = 5 V) Max Propagation Delay**
- **10-Pin MSOP Package**
- **Temperature Range . . . –40°C to 85°C**

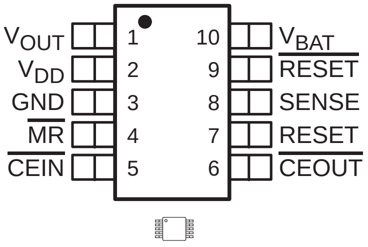
typical applications

- **Fax Machines**
- **Set-Top Boxes**
- **Advanced Voice Mail Systems**
- **Portable Battery Powered Equipment**
- **Computer Equipment**
- **Advanced Modems**
- **Automotive Systems**
- **Portable Long-Time Monitoring Equipment**
- **Point of Sale Equipment**

description

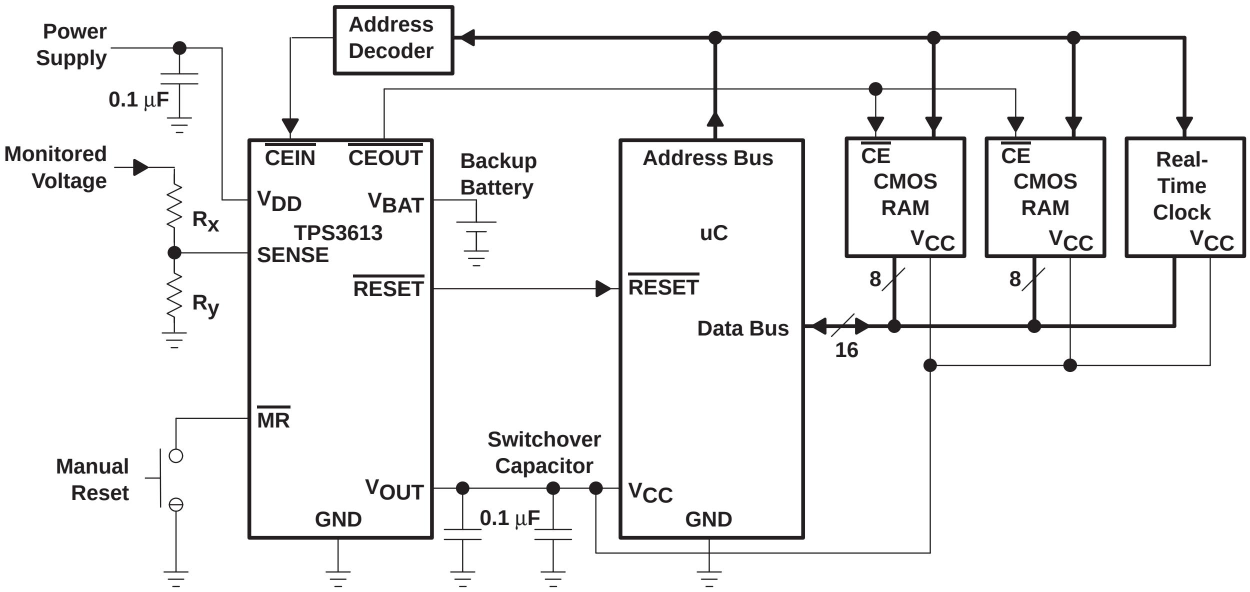
The TPS3613-01 supervisory circuit monitors and controls processor activity by providing backup-battery switchover for data retention of CMOS RAM.

DGS PACKAGE
(TOP VIEW)



ACTUAL SIZE
3,05 mm x 4,98 mm

typical operating circuit



description (continued)

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD} or V_{Bat}) becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage V_{IT}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above the threshold voltage V_{IT}.

When the supply voltage drops below the threshold voltage V_{IT}, the output becomes active (low) again.

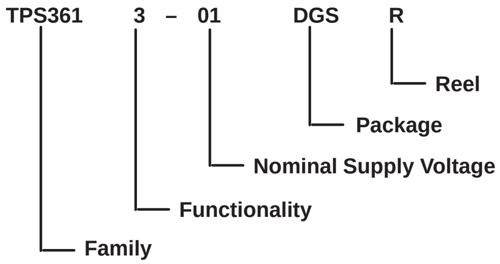
The TPS3613-01 is available in a 10-pin MSOP package and is characterized for operation over a temperature range of –40°C to 85°C.

PACKAGE INFORMATION

T_A	DEVICE NAME		MARKING
–40°C to 85°C	TPS3613–01DGSR[†]	TPS3613–01DGST[‡]	AFK

[†] The DGSR passive indicates tape and reel of 2500 parts.

ordering information application specific versions[§]



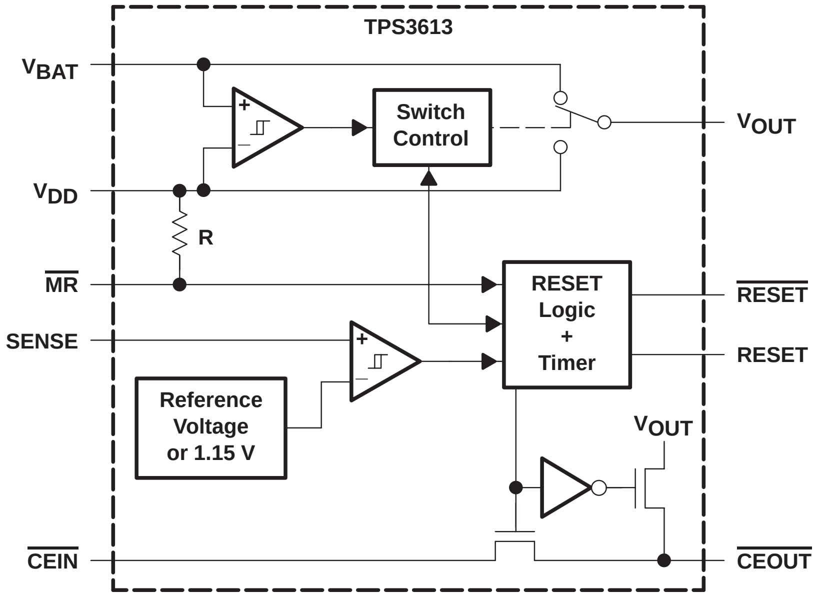
DEVICE NAME	NOMINAL VOLTAGE, V_{NOM}
TPS3613x01 DGS	Adjustable
TPS3613x18 DGS[‡]	1.8 V
TPS3613x25 DGS[‡]	2.5 V
TPS3613x30 DGS[‡]	3.0 V
TPS3613x33 DGS[‡]	3.3 V
TPS3613x50 DGS[‡]	5.0 V

[‡] For the application specific versions please contact the local TI sales office for availability and lead-time.

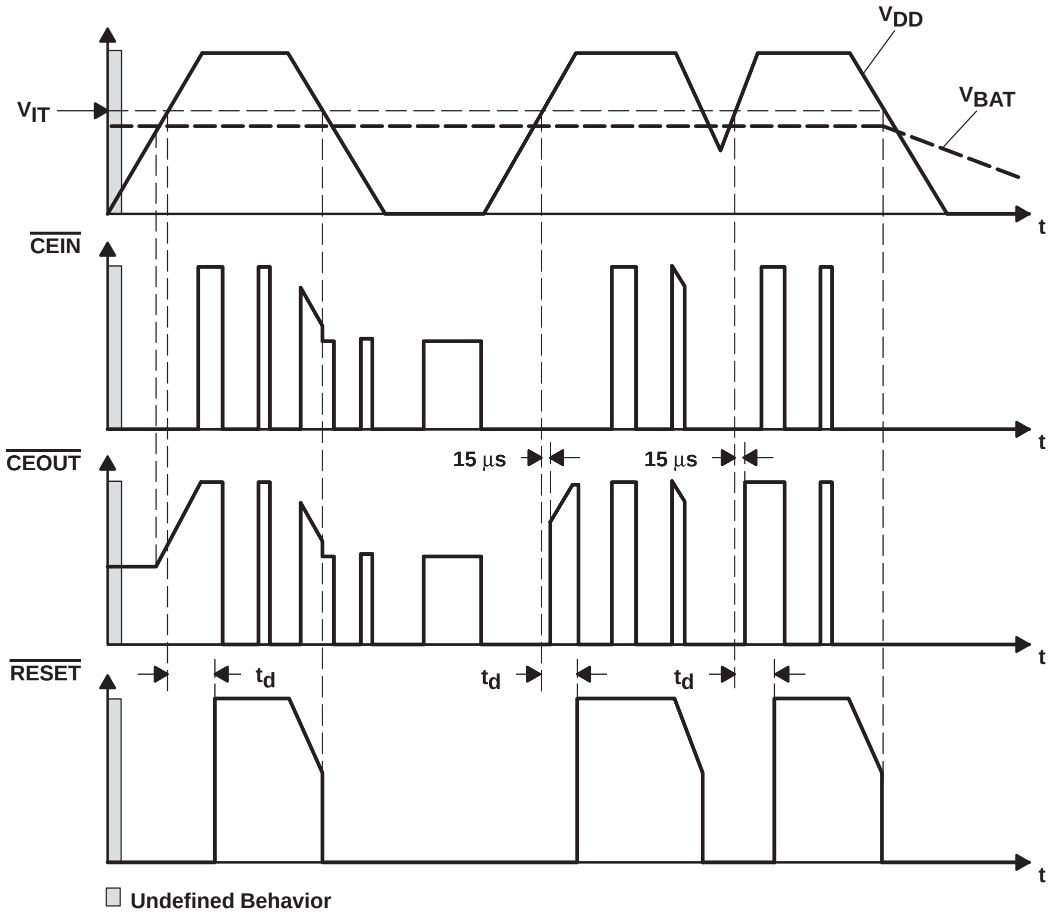
FUNCTION TABLE

SENSE > V_{IT}	$V_{DD} > V_{BAT}$	$\overline{\text{MR}}$	$\overline{\text{CEIN}}$	V_{OUT}	$\overline{\text{RESET}}$	RESET	$\overline{\text{CEOUT}}$
0	0	0	0	V_{BAT}	0	1	DIS
0	0	0	1	V_{BAT}	0	1	DIS
0	0	1	0	V_{BAT}	0	1	DIS
0	0	1	1	V_{BAT}	0	1	DIS
0	1	0	0	V_{DD}	0	1	DIS
0	1	0	1	V_{DD}	0	1	DIS
0	1	1	0	V_{DD}	0	1	DIS
0	1	1	1	V_{DD}	0	1	DIS
1	0	0	0	V_{DD}	0	1	DIS
1	0	0	1	V_{DD}	0	1	DIS
1	0	1	0	V_{DD}	1	0	0
1	0	1	1	V_{DD}	1	0	1
1	1	0	0	V_{DD}	0	1	DIS
1	1	0	1	V_{DD}	0	1	DIS
1	1	1	0	V_{DD}	1	0	0
1	1	1	1	V_{DD}	1	0	1

functional schematic



timing diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{CEIN}}$	5	I	Chip-enable input
$\overline{\text{CEOUT}}$	6	O	Chip-enable output
GND	3	I	Ground
$\overline{\text{MR}}$	4	I	Manual reset input
RESET	7	O	Active-high reset output
$\overline{\text{RESET}}$	9	O	Active-low reset output
SENSE	8	I	Adjustable sense input
V_{BAT}	10	I	Backup-battery input
V_{DD}	2	I	Input supply voltage
V_{OUT}	1	O	Supply output

detailed description

backup-battery switchover

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup battery is installed at V_{BAT}, the device automatically switches the connected RAM to backup power when V_{DD} fails. In order to allow the backup battery (e.g., 3.6-V lithium cells) to have a higher voltage than V_{DD}, these supervisors will not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD}. V_{BAT} only connects to V_{OUT} (through a 15-Ω switch) when V_{DD} falls below V_{IT} and V_{BAT} is greater than V_{DD}. When V_{DD} recovers, switchover is deferred either until V_{DD} crosses V_{BAT}, or when V_{DD} rises above the reset threshold V_{IT}. V_{OUT} will connect to V_{DD} through a 1-Ω (max) PMOS switch when V_{DD} crosses the reset threshold.

V_{DD}>V_{BAT}	V_{DD}>V_{IT}	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

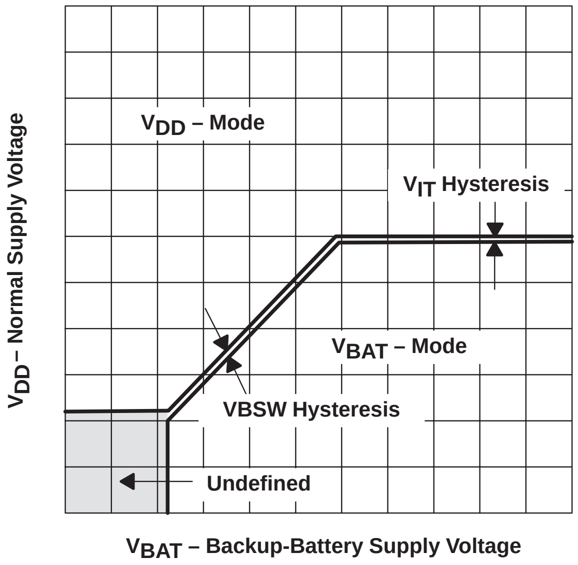


Figure 1. V_{DD} – V_{BAT} Switchover

detailed description (continued)

chip-enable signal gating

The internal gating of chip-enable (CE) signals prevents erroneous data from corrupting CMOS RAM during an under-voltage condition. The TPS3613 use a series transmission gate from $\overline{\text{CEIN}}$ to $\overline{\text{CEOUT}}$. During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from $\overline{\text{CEIN}}$ to $\overline{\text{CEOUT}}$ enables the TPS3613 device to be used with most processors.

chip-enable signal gating (continued)

The CE transmission gate is disabled and $\overline{\text{CEIN}}$ is high impedance (disable mode) while reset is asserted. During a power-down sequence when V_{DD} crosses the reset threshold, the CE transmission gate will be disabled and $\overline{\text{CEIN}}$ immediately becomes high impedance if the voltage at $\overline{\text{CEIN}}$ is high. If $\overline{\text{CEIN}}$ is low when reset is asserted, the CE transmission gate will be disabled same time when $\overline{\text{CEIN}}$ goes high, or 10 µs after reset asserts, whichever occurs first. This will allow the current write cycle to complete during power down. When the CE transmission gate is enabled, the impedance of $\overline{\text{CEIN}}$ appears as a resistor in series with the load at $\overline{\text{CEOUT}}$. The overall device propagation delay through the CE transmission gate depends on V_{OUT}, the source impedance of the drive connected to $\overline{\text{CEIN}}$, and the load at $\overline{\text{CEOUT}}$. To achieve minimum propagation delay, the capacitive load at $\overline{\text{CEOUT}}$ should be minimized, and a low-output-impedance driver is used.

In the disabled mode, the transmission gate is off and an active pullup connects $\overline{\text{CEOUT}}$ to V_{OUT}. This pullup turns off when the transmission gate is enabled.

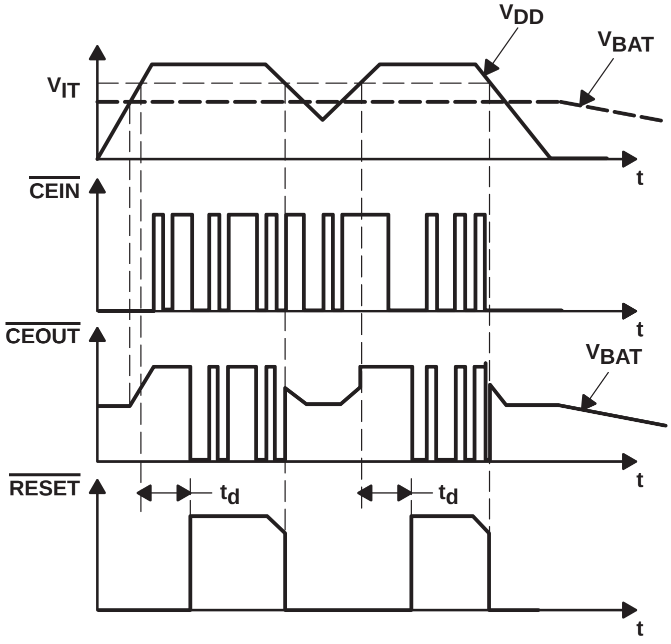


Figure 2. Chip-Enable Timing

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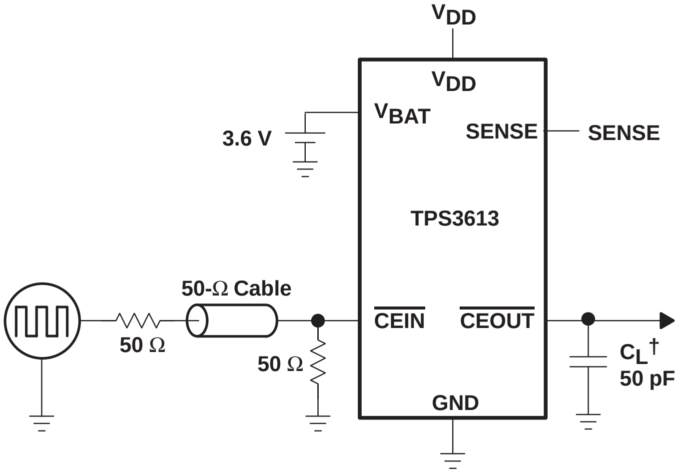
detailed description (continued)



†C_L Includes load capacitance and scope probe capacitance.

Figure 3. CE Propagation Delay Test Circuit

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note1)	7 V
All other pins (see Note 1)	–0.3 V to 7 V
Continuous output current at V_{OUT}, I_O	400 mA
Continuous output current (all other pins), I_O	±10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t=1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGS	424 mW	3.4 mW/°C	271 mW	220 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.65	5.5	V
Battery supply voltage, V_{BAT}	1.5	5.5	V
Input voltage, V_I	0	V_{DD} + 0.3	V
High-level input voltage, V_{IH}	0.7 x V_{DD}		V
Low-level input voltage, V_{IL}		0.3 x V_{DD}	V
Continuous output current at V_{OUT}, I_O		300	mA
Input transition rise and fall rate at $\overline{\text{MR}}$, $\Delta t/\Delta V$		100	ns/V
Slew rate at V_{DD} or V_{bat}		1	V/µs
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{\text{RESET}}$	V_{DD} = 1.8 V I_{OH} = –400 µA	V_{DD} – 0.2 V			V
			V_{DD} = 3.3 V, I_{OH} = –2 mA V_{DD} = 5 V, I_{OH} = –3 mA	V_{DD} – 0.4 V			
		RESET	V_{DD} = 1.8 V, I_{OH} = –20 µA	V_{DD} – 0.3 V			
			V_{DD} = 3.3 V, I_{OH} = –80 µA V_{DD} = 5 V, I_{OH} = –120 µA	V_{DD} – 0.4 V			
		$\overline{\text{CEOUT}}$ Enable mode $\overline{\text{CEIN}}$ = V_{OUT}	V_{OUT} = 1.8 V, I_{OH} = –1 mA	V_{OUT} – 0.2 V			
			V_{OUT} = 3.3 V, I_{OH} = –2.0 mA V_{OUT} = 5 V, I_{OH} = –5.0 mA	V_{OUT} – 0.3 V			
		$\overline{\text{CEOUT}}$ Disable mode	V_{OUT} = 3.3 V, I_{OH} = –0.5 mA	V_{OUT} – 0.4 V			
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$ RESET	V_{DD} = 1.8 V, I_{OL} = 400 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2.0 mA V_{DD} = 5 V, I_{OL} = 3.0 mA			0.4	
		$\overline{\text{CEOUT}}$ Enable mode $\overline{\text{CEIN}}$ = 0 V	V_{OUT} = 1.8 V, I_{OL} = 1.0 mA			0.2	
			V_{OUT} = 3.3 V, I_{OL} = 2 mA V_{OUT} = 5 V, I_{OL} = 5 mA			0.3	
V_{res}	Power-up reset voltage (see Note 2)		V_{DD} > 1.1 V or V_{BAT} > 1.1 V, I_{OL} = 20 µA			0.4	V
V_{OUT}	Normal mode		I_{OUT} = –8.5 mA, V_{DD} = 1.8 V, V_{BAT} = 0 V	V_{DD} – 50 mV			V
			I_{OUT} = –125 mA V_{DD} = 3.3 V, V_{BAT} = 0 V	V_{DD} – 150 mV			
			I_{OUT} = –200 mA V_{DD} = 5 V, V_{BAT} = 0 V	V_{DD} – 200 mV			
	Battery-backup mode		I_{OUT} = –0.5 mA V_{BAT} = 1.5 V, V_{DD} = 0 V	V_{BAT} – 20 mV			
			I_{OUT} = –7.5 mA V_{BAT} = 3.3 V, V_{DD} = 0 V	V_{BAT} – 113 mV			

NOTE 2: The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. $t_{r,(VDD)} \ge$ 15 µs/V.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	V_{DD} to V_{OUT} on-resistance		$V_{DD} = 5$ V		0.6	1	Ω
	V_{BAT} to V_{OUT} on-resistance		$V_{BAT} = 3.3$ V		8	15	
V_{IT}	Negative-going input threshold voltage (see Note 3)			1.13	1.15	1.17	V
V_{hys}	Hysteresis	Sense	$1.1 \text{ V} < V_{IT} < 1.65 \text{ V}$		12		mV
		V_{BSW} (see Note 4)	VDD = 1.8 V		55		
I_{IH}	High-level input current	$\overline{\text{MR}}$	$\overline{\text{MR}} = 0.7 \times V_{DD}$, $V_{DD} = 5.0$ V	–33		–76	µA
I_{IL}	Low-level input current		$\overline{\text{MR}} = 0$ V, $V_{DD} = 5.0$ V	–110		–255	
I_I	Input current	$\overline{\text{SENSE}}$	$V_{DD} = 1.15$ V	–25		25	nA
I_{DD}	V_{DD} supply current		$V_{OUT} = V_{DD}$			40	µA
			$V_{OUT} = V_{BAT}$			40	
I_{BAT}	V_{BAT} supply current		$V_{OUT} = V_{DD}$	–0.1		0.1	µA
			$V_{OUT} = V_{BAT}$			0.5	
I_{lkg}	$\overline{\text{CEIN}}$ leakage current		Disable mode, $V_I < V_{DD}$			±1	µA
C_i	Input capacitance		$V_I = 0$ V to 5 V		5		pF

NOTES: 3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals.
4. For $V_{DD} < 1.6$ V, V_{OUT} switches to V_{BAT} regardless of V_{BAT}

timing requirements at $R_L = 1$ MΩ, $C_L = 50$ pF, $T_A = -40°C$ to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	SENSE	$V_{IH} = V_{IT} + 0.2$ V, $V_{IL} = V_{IT} - 0.2$ V	6			µs
		$\overline{\text{MR}}$	$V_{SENSE} > V_{IT} + 0.2$ V $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	100			ns

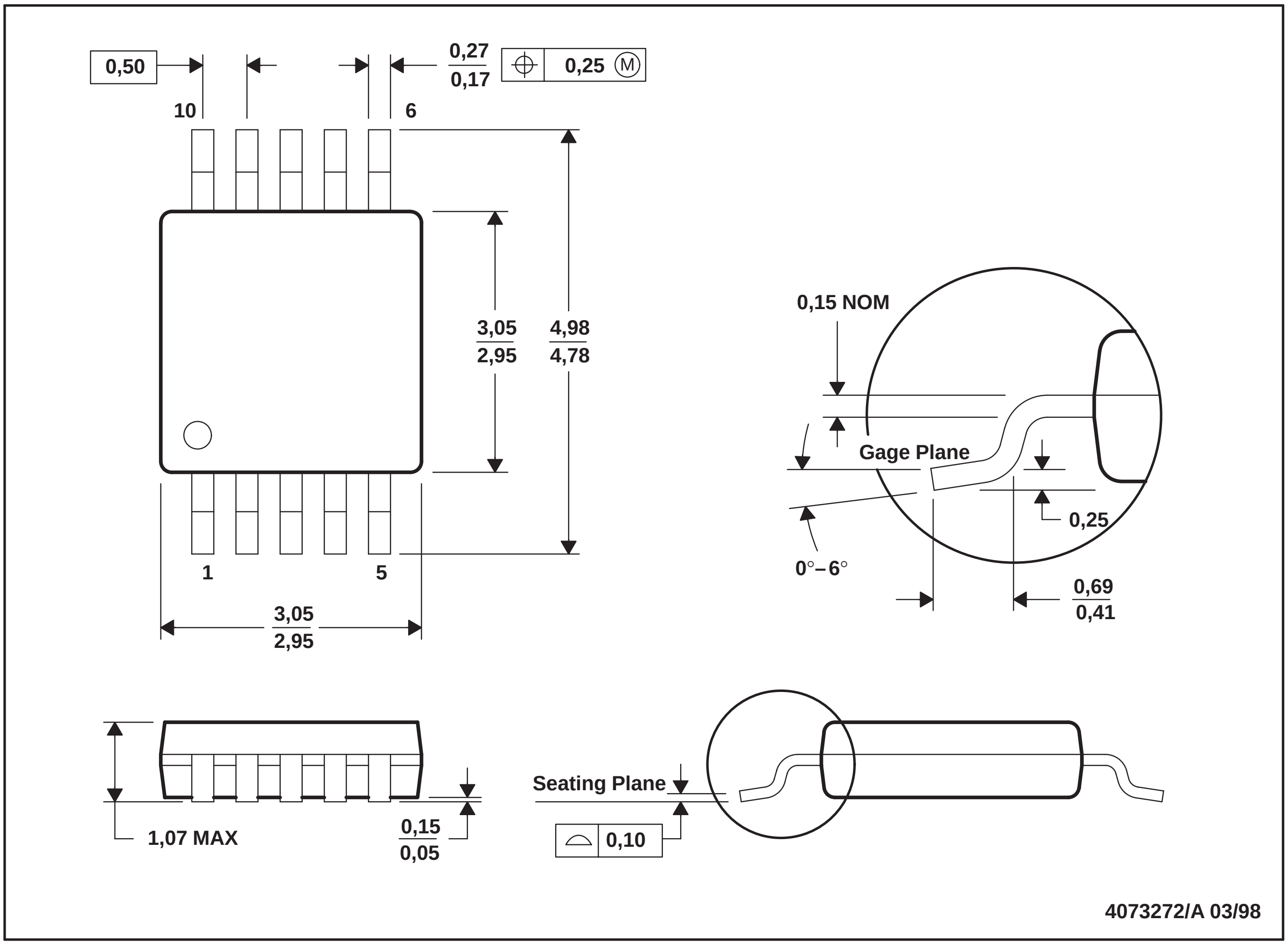
switching characteristics at $R_L = 1$ MΩ, $C_L = 50$ pF, $T_A = -40°C$ to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{SENSE} \geq V_{IT} + 0.2$ V, $\overline{\text{MR}} \geq 0.7 \times V_{DD}$, See timing diagram	60	100	140	ms
t_{PLH}	Propagation (delay) time, low-to-high-level output	50% $\overline{\text{RESET}}$ to 50% $\overline{\text{CEOUT}}$	$V_{OUT} = V_{IT}$		15		µs
		SENSE to RESET	$V_{IL} = V_{IT} - 0.2$ V, $V_{IH} = V_{IT} + 0.2$ V		2	5	
		$\overline{\text{MR}}$ to RESET	$V_{SENSE} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$		0.1	1	
t_{PHL}	Propagation (delay) time, high-to-low-level output	50% $\overline{\text{CEIN}}$ to 50% $\overline{\text{CEOUT}}$, $C_L = 50$ pF only (see Figure 3) (see Note 5) 50% $\overline{\text{CEIN}}$ to 50% $\overline{\text{CEOUT}}$, $C_L = 50$ pF only (see Figure 3) (see Note 5)	$V_{DD} = 1.8$ V		5	15	ns
			$V_{DD} = 3.3$ V		1.6	5	
			$V_{DD} = 5$ V		1	3	
		SENSE to $\overline{\text{RESET}}$	$V_{IL} = V_{IT} - 0.2$ V, $V_{IH} = V_{IT} + 0.2$ V		2	5	µs
		$\overline{\text{MR}}$ to $\overline{\text{RESET}}$	$V_{SENSE} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$		0.1	1	µs
	Transition time	V_{DD} to V_{BAT}	$V_{IH} = V_{BAT} + 0.2$ V, $V_{IL} = V_{BAT} - 0.2$ V, $V_{BAT} < V_{IT}$			3	µs

NOTE 5: Assured by design

MECHANICAL DATA

DGS (S-PDSO-G10) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

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