TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

262,144 WORDS × 16 BIT STATIC RAM

DESCRIPTION

The TC554161FTI is 4,194,304 bits static random access memory organized as 262,144 words by 16 bits using CMOS technology, and operated a single 3.0~5.5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 10mA/MHz (Typ.)and minimum cycle time of 85ns. When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 4μA (Typically). The TC554161FTI has two control inputs. Chip enable input ($\overline{CE}$) allows for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Also it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). Thus the TC554161FTI is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required, and wide operating temperature system for TC554161FTI guarantees −40~85°C operating temperature.

The TC554161FTI is offered in a 54 pin thin small-out-line plastic package.

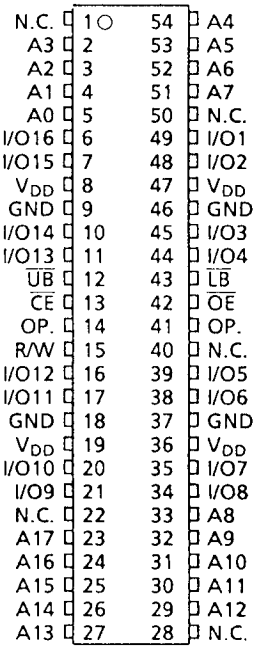
FEATURES

- Low Power Dissipation : 55mW/MHz (Typ.) Operating
- Standby Current: 8μA (Max.) at Ta = 25°C
- Single Power Supply : 3.0 ~ 5.5V
- Power Down Features : $\overline{CE}$
- Data Retention Supply Voltage : 2.0 ~ 5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Wide Temperature Operation : −40 ~ 85°C
- Access Time (Max.)

	5V ± 10%		3.0V~5.5V
	-85V	-10V	-85V/-10V
Access Time	85ns	100ns	150ns
$\overline{CE}$ Access Time	85ns	100ns	150ns
$\overline{OE}$ Access Time	45ns	50ns	75ns

- Package:
  TSOP II 54-P-400-0.80(FTI) (Weight: 0.55g typ)

PIN ASSIGNMENT (TOP VIEW)

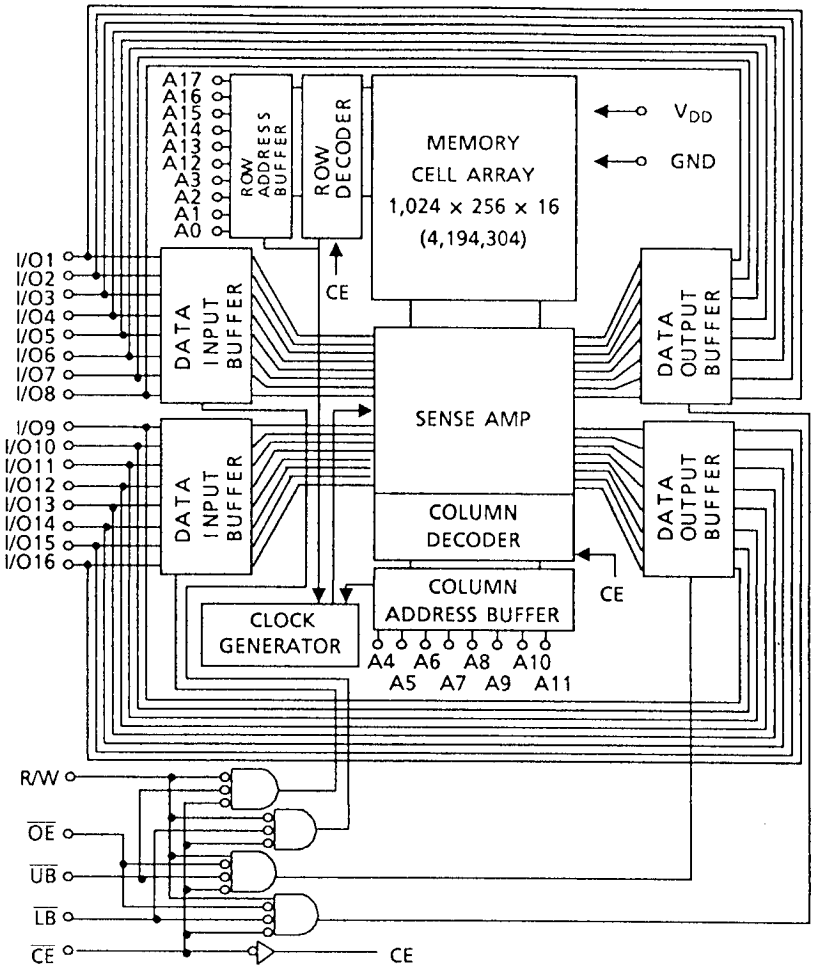


PIN NAMES

A0~A17	Address Inputs
I/O1~I/O16	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
V_{DD}	Power
GND	Ground
N.C.	No Connection
OP.*	Option

* : OP. pin must be connected to GND or open.

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Terminal Voltage	−0.3 * ~7.0	V
$V_{I/O}$	Input / Output Terminal Voltage	−0.5 * ~VDD + 0.5	V
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{strg}	Storage Temperature	−55~150	°C
T_{opr}	Operating Temperature	−40~85	°C

* : −3V at pulse width 30ns Max

DC RECOMMENDED OPERATING CONDITIONS (Ta = −40~85°C)

SYMBOL	PARAMETER	5V ± 10%			3.0~5.5V			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{DD}	Power Suply Voltage	4.5	5.0	5.5	3.0	−	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD} + 0.3	V_{DD} − 0.2V	−	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3 *	−	0.6	−0.3 *	−	0.2	V
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	2.0	−	5.5	V

* : −3V with a pulse width of 30ns

D.C. and OPERATING CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION				MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}				−	−	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/$\overline{W}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0~VDD				−	−	± 1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V				− 1.0	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V				2.1	−	−	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} R/$\overline{W}$ = V_{IH}, Iout = 0mA Other Inputs = V_{IH} / V_{IL}	Tcycle	Min.		−	−	100	mA
				1μs		−	15	−	
I_{DDO2}		$\overline{CE}$ = 0.2V, R/$\overline{W}$ = V_{DD} − 0.2V, Iout = 0mA Other Inputs = V_{DD} − 0.2V / 0.2V	Tcycle	Min.		−	−	90	mA
				1μs		−	10	−	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH} / V_{IL}				−	−	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V	V_{DD} = 2.0V~5.5V		Ta = 25°C	−	4	8	μA
					Ta = −40~85°C	−	−	140	
			V_{DD} = 3.0V		Ta = 25°C	−	2	−	
					Ta = −40~40°C	−	−	6	
					Ta = −40~85°C	−	−	70	

D.C. and OPERATING CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 3.3V ± 0.3V)

SYMBOL	PARAMETER	TEST CONDITION				MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}				−	−	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/$\overline{W}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0~V_{DD}				−	−	± 1.0	μA
I_{OH}	Output High Current	V_{OH} = V_{DD} − 0.2V				− 1.0	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.2V				0.1	−	−	mA
I_{DDO2}	Operating Current	$\overline{CE}$ = 0.2V, R/$\overline{W}$ = V_{DD} − 0.2V, Iout = 0mA Other Inputs = V_{DD} − 0.2V / 0.2V	Tcycle	MIN.		−	−	35	mA
				1μs		−	5	−	
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} − 0.2V	V_{DD} = 3.3V ± 0.3V		Ta = 25°C	−	2	4	μA
					Ta = −40~85°C	−	−	90	
			V_{DD} = 3.3V		Ta = 25°C	−	2	−	
					Ta = −40~40°C	−	−	8	
					Ta = −40~85°C	−	−	80	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	−	−	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	−	−	10	pF

NOTE : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

* : H or L

AC CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85V		-10V		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO}	$\overline{CE}$ Access Time	–	85	–	100	
t_{OE}	$\overline{OE}$ Access Time	–	45	–	50	
t_{BA}	$\overline{UB}$, $\overline{LB}$ Access Time	–	45	–	50	
t_{OH}	Output Data Hold Time from Address Change	10	–	10	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	–	0	–	
t_{BE}	Output Enable Time from $\overline{UB}$, $\overline{LB}$	0	–	0	–	
t_{OD}	Output Disable Time from $\overline{CE}$	–	35	–	40	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	35	–	40	
t_{BD}	Output Disable Time from $\overline{UB}$, $\overline{LB}$	–	35	–	40	

WRITE CYCLE

SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85V		-10V		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	55	–	60	–	
t_{CW}	Chip Enable to End of Write	70	–	80	–	
t_{BW}	$\overline{UB}$, $\overline{LB}$ Enable to End of Write	55	–	60	–	
t_{AS}	Address Set Up Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Set Up Time	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from R/W	0	–	0	–	
t_{ODW}	Output Disable Time from R/W	–	35	–	40	

AC TEST CONDITIONS

Input Pulse Level	0.4V / 2.6V
Input Pulse Rise and Fall Time	5ns
Input timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	100pF + ITTL Gate

AC CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 3.0~5.5V)

READ CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	–	ns
t_{ACC}	Address Access Time	–	150	
t_{CO}	$\overline{CE}$ Access Time	–	150	
t_{OE}	$\overline{OE}$ Access Time	–	75	
t_{BA}	$\overline{UB}$, $\overline{LB}$ Access Time	–	75	
t_{OH}	Output Data Hold Time from Address Change	10	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	–	
t_{BE}	Output Enable Time from $\overline{UB}$, $\overline{LB}$	0	–	
t_{OD}	Output Disable Time from $\overline{CE}$	–	50	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	50	
t_{BD}	Output Disable Time from $\overline{UB}$, $\overline{LB}$	–	50	

WRITE CYCLE

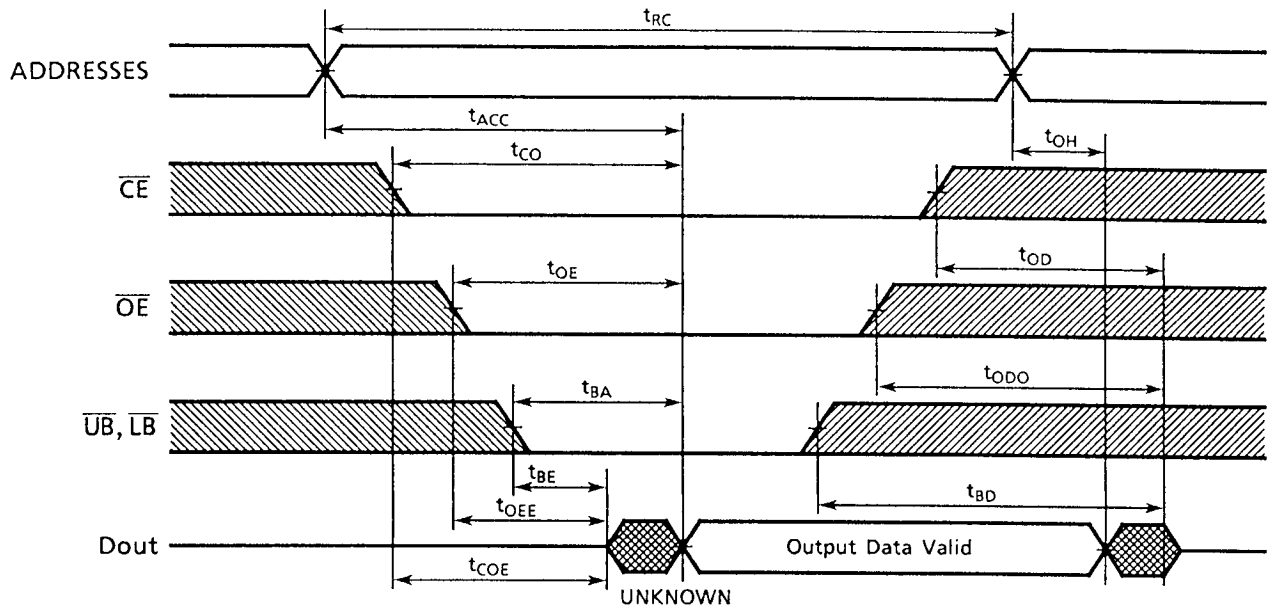
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	150	–	ns
t_{WP}	Write Pulse Width	100	–	
t_{CW}	Chip Enable to End of Write	120	–	
t_{BW}	$\overline{UB}$, $\overline{LB}$ Enable to End of Write	100	–	
t_{AS}	Address Set Up Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{DS}	Data Set Up Time	60	–	
t_{DH}	Data Hold Time	0	–	
t_{OEW}	Output Enable Time from R/W	0	–	
t_{ODW}	Output Disable Time from R/W	–	50	

AC TEST CONDITIONS

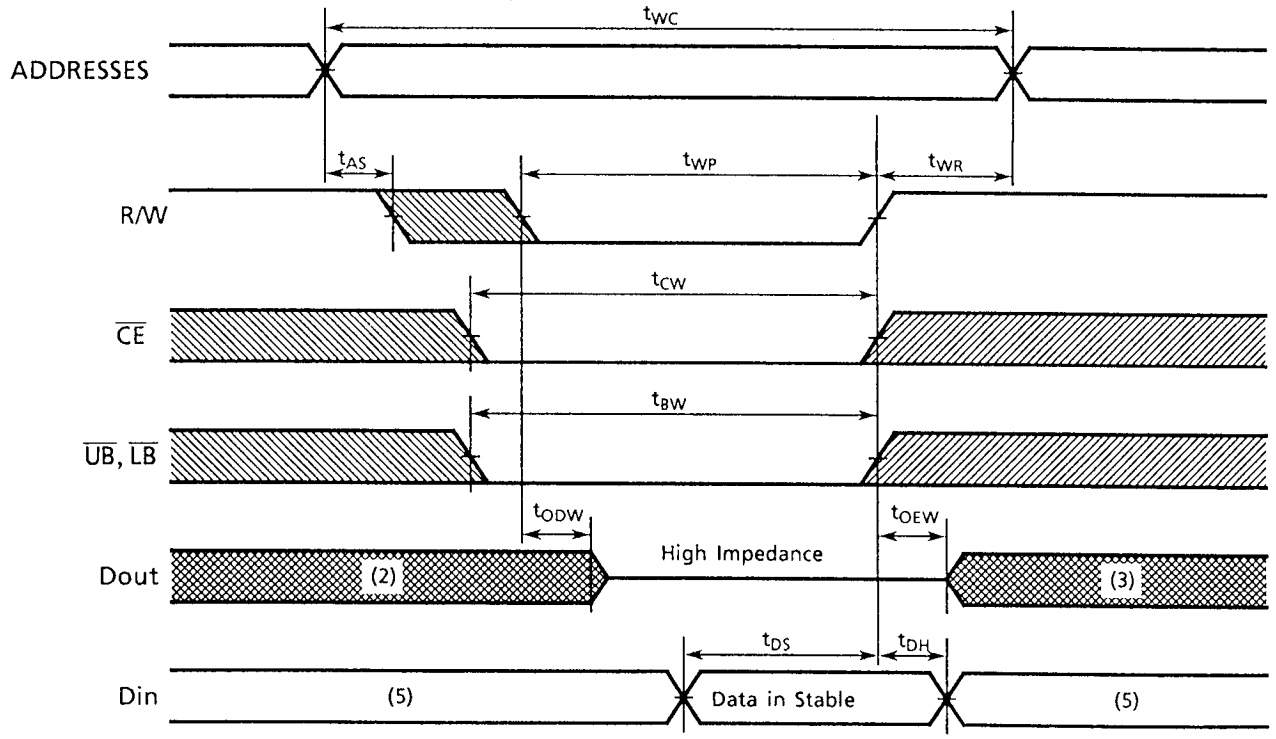
Input Pulse Level	V_{DD} − 0.2V / 0.2V
Input Pulse Rise and Fall Time	5ns
Input timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	100pF (Include Jig)

TIMING WAVEFORMS

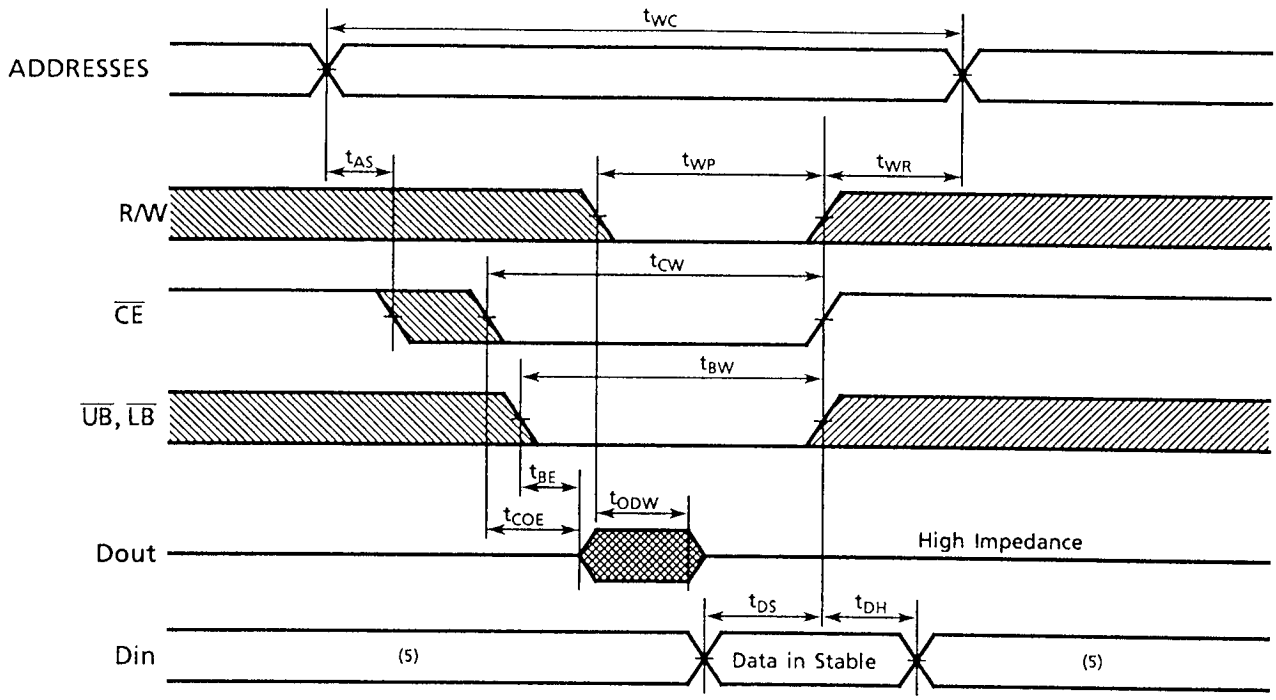
READ CYCLE (1)



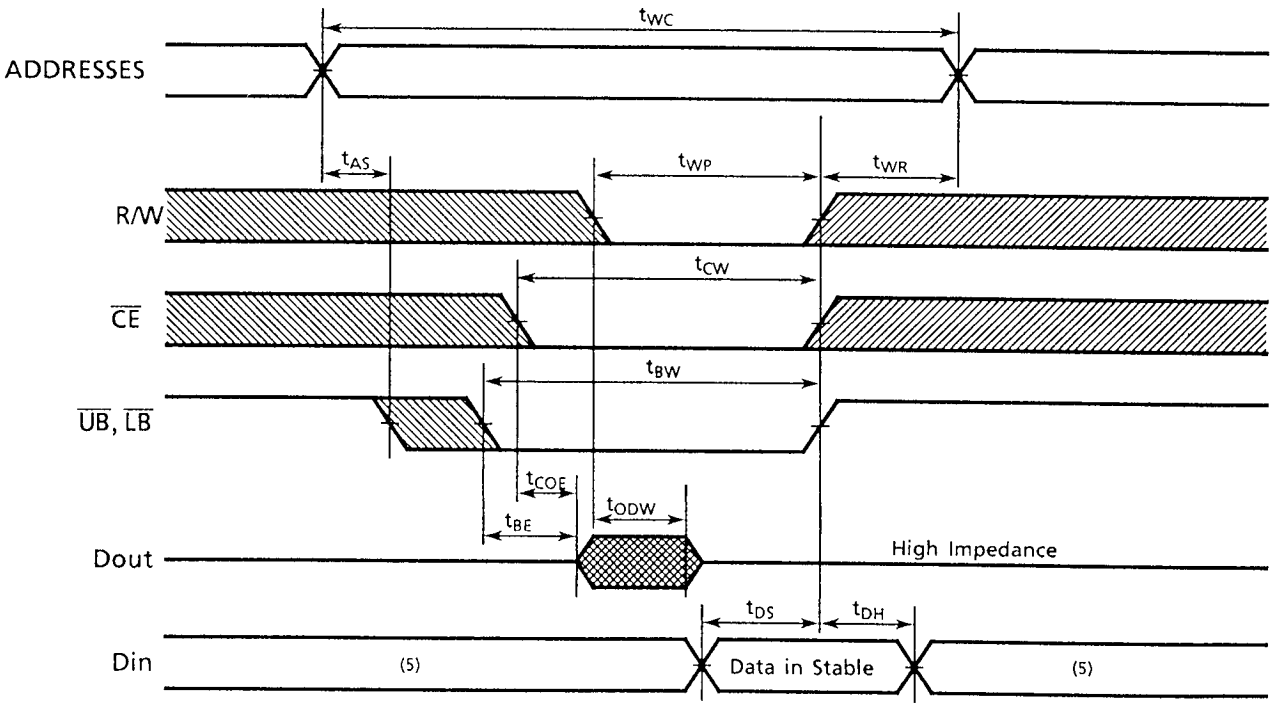
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}$ Controlled Write)



WRITE CYCLE 3 (4) ($\overline{UB}$, $\overline{LB}$ Controlled Write)



NOTE :

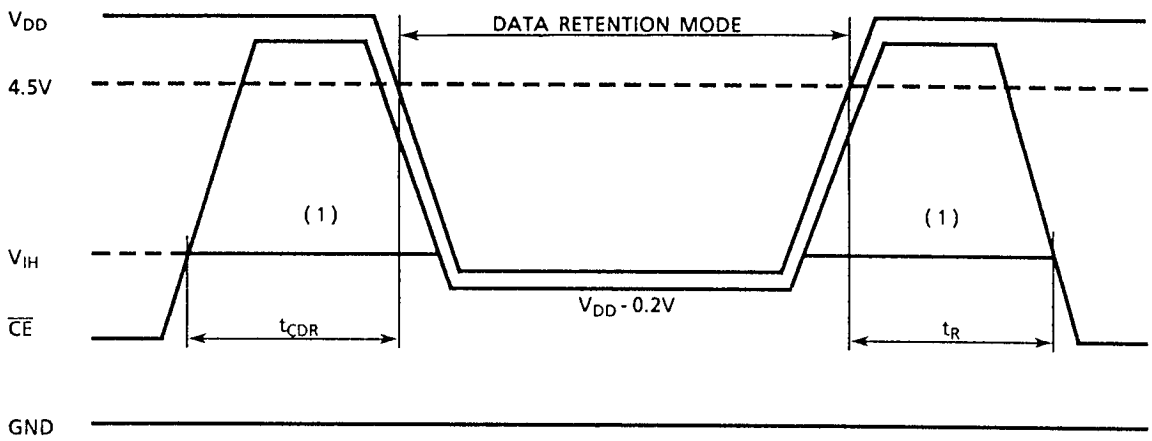
1. R/W is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.
5. The I/O may be in the output state at this time, input signals of opposite phase must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = −40 ~ 85 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.3V	–	–	80*	μA
		V_{DD} = 5.5V	–	–	140	
t_{CDR}	Chip Deselection to Data Retention Mode		0	–	–	nS
t_R	Recovery Time		5	–	–	mS

*)8μA (Max.) Ta = −40~40°C

$\overline{CE}$ Controlled Data Retention Mode

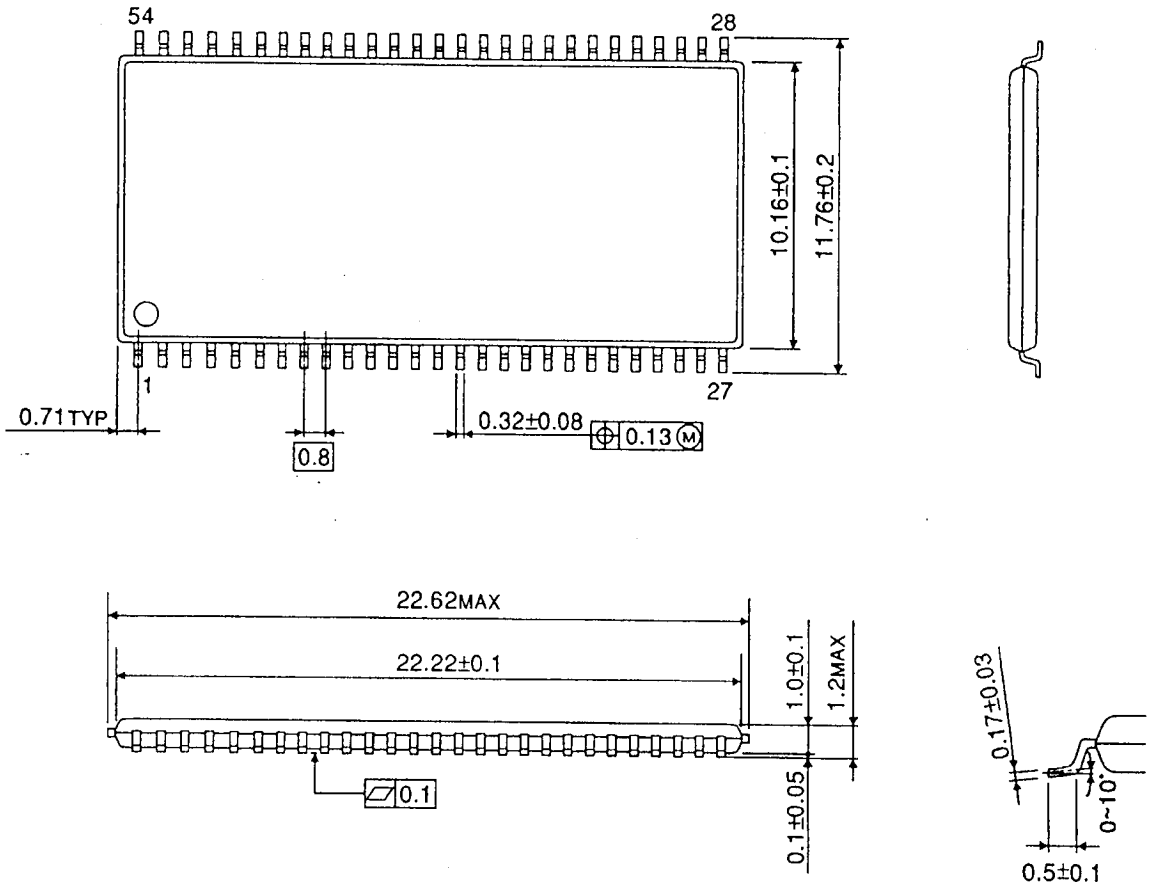


NOTE :

(1) If the V_{IH} of $\overline{CE}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

PACKAGE DIMENSIONS (TSOPII 54-P-400-0.80)

Units in mm



Weight: 0.55 g (typ)