# STL9N3LLH5

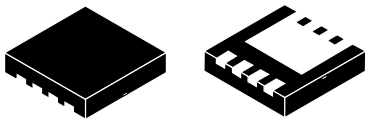
## N-channel 30 V, 0.015 Ω, 9 A, PowerFLAT™ (3.3x3.3) STripFET™ V Power MOSFET

## Features

| Type | $V_{DSS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STL9N3LLH5 | 30 V | < 0.019 Ω | 9 A (1) |

1. The value is rated according Rthj-pcb

- $R_{DS(on)}$ * $Q_g$ industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



**PowerFLAT™(3.3x3.3)**

**(Chip scale package)**

## Applications

- Switching applications

## Description

This product utilizes the 5th generation of design rules of ST's proprietary STripFET™ technology. The lowest available $R_{DS(on)}$*$Q_g$, in this chip scale package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

**Figure 1. Internal schematic diagram**

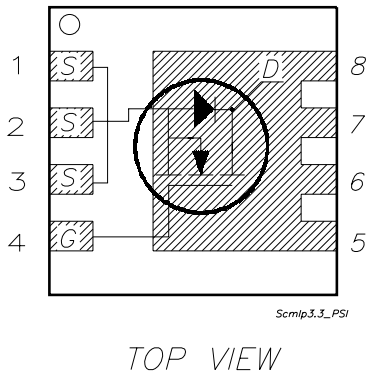



**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STL9N3LLH5 | 9N3L | PowerFLAT™ (3.3x3.3) | Tape and reel |

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 30 | V |
| $V_{GS}$ | Gate-source voltage | ± 22 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25 °C | 9 | A |
| $I_D$ (1) | Drain current (continuous) at $T_C$=100 °C | 6 | A |
| $I_{DM}$ (2) | Drain current (pulsed) | 36 | A |
| $P_{TOT}$ (3) | Total dissipation at $T_C$ = 25 °C | 50 | W |
| $P_{TOT}$ (1) | Total dissipation at $T_C$ = 25 °C | 2 | W |
| | Derating factor | 0.4 | W/°C |
| $T_J$<br>$T_{stg}$ | Operating junction temperature<br>storage temperature | -55 to 150 | °C |

1. The value is rated according Rthj-pcb
2. Pulse width limited by safe operating area.
3. The vaule is rated according Rthj-c

**Table 3. Thermal resistance**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case (drain) | 2.5 | °C/W |
| $R_{thj\text{-}pcb}$ (1) | Thermal resistance junction-pcb | 42.8 | °C/W |
| $R_{thj\text{-}pcb}$ (2) | Thermal resistance junction-pcb | 63.5 | °C/W |

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10sec
2. Steady state

# 2 Electrical characteristics

($T_{CASE}$=25 °C unless otherwise specified)

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 250 µA, $V_{GS}$= 0 | 30 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating,<br>$V_{DS}$ = Max rating @125 °C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 22 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$= $V_{GS}$, $I_D$ = 250 µA | 1 | | 2.5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$= 10 V, $I_D$= 4.5 A<br>$V_{GS}$= 4.5 V, $I_D$= 4.5 A | | 15<br>19 | 19<br>22 | mΩ<br>mΩ |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ =25 V, f=1 MHz,<br>$V_{GS}$=0 | - | 724<br>132<br>20 | | pF<br>pF<br>pF |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$=15 V, $I_D$ = 9 A<br>$V_{GS}$ =4.5 V<br>*(see Figure 14)* | - | 5<br>2<br>2 | | nC<br>nC<br>nC |
| $R_G$ | Gate input resistance | f=1 MHz Gate DC Bias = 0<br>Test signal level = 20 mV<br>Open drain | - | | 3.3 | Ω |

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on delay time<br>Rise time<br>Turn-off delay time<br>Fall time | $V_{DD}$=15 V, $I_D$= 4.5 A,<br>$R_G$=4.7 Ω, $V_{GS}$= 10 V<br>*(see Figure 13)* | - | 4<br>4.2<br>21<br>3.5 | - | ns<br>ns<br>ns<br>ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 9 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 36 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$= 9 A, $V_{GS}$=0 | - | | 1.1 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$= 9 A,<br>di/dt = 100 A/µs,<br>$V_{DD}$=20 V, Tj=150 °C<br>*(see Figure 18)* | - | 21<br>10<br>1 | | ns<br>nC<br>A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

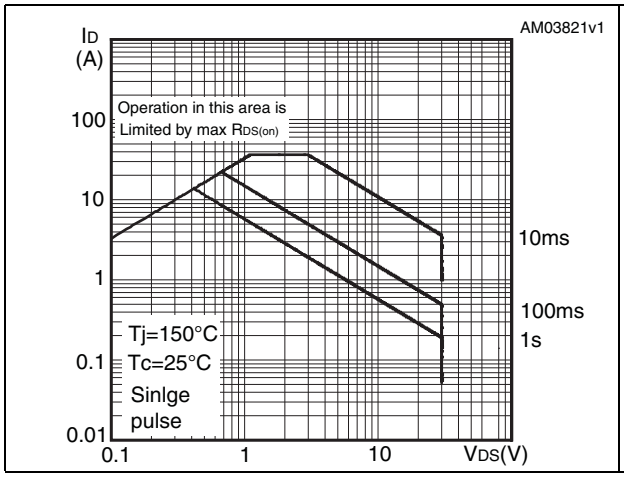



**Figure 3. Thermal impedance**

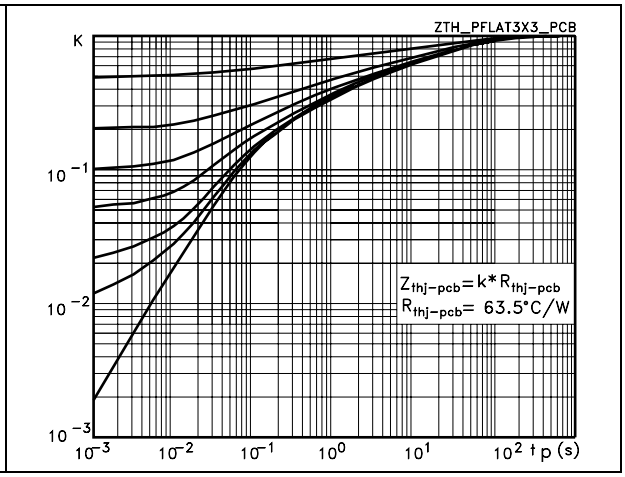



**Figure 4. Output characteristics**

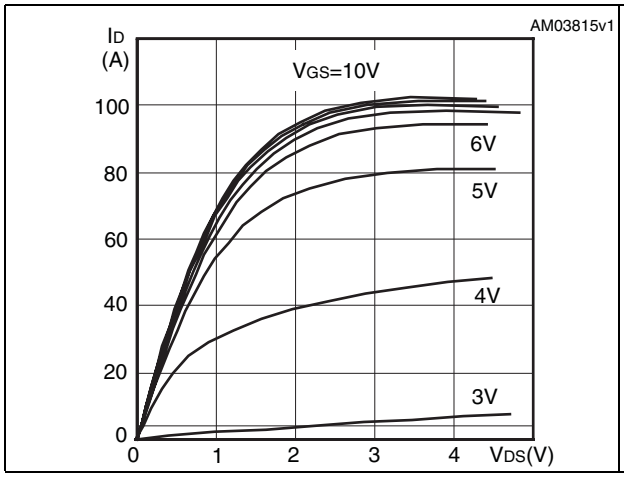



**Figure 5. Transfer characteristics**

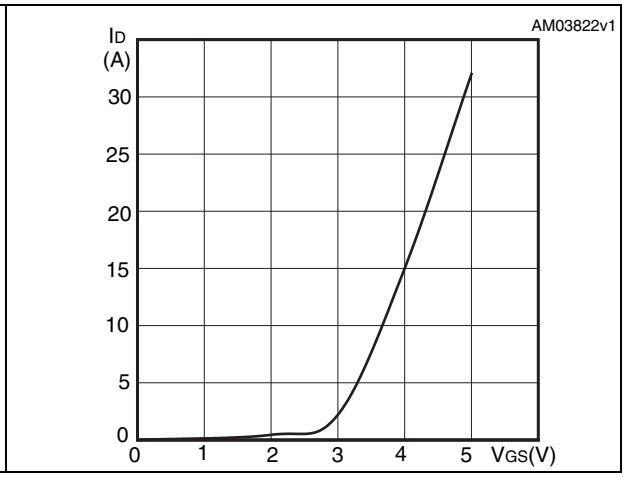



**Figure 6. Normalized $B_{VDSS}$ vs temperature**

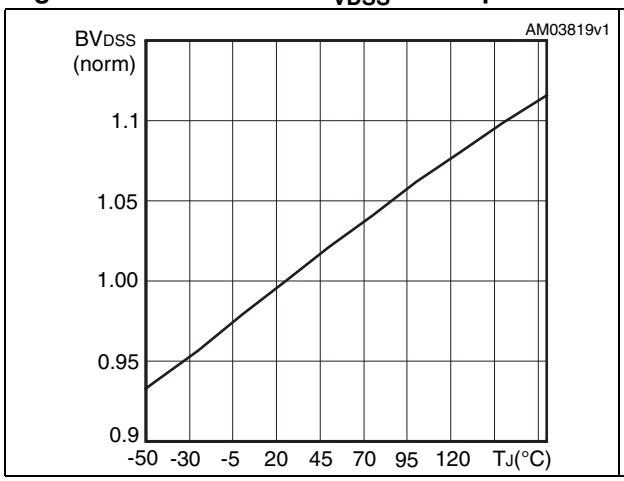



**Figure 7. Static drain-source on resistance**

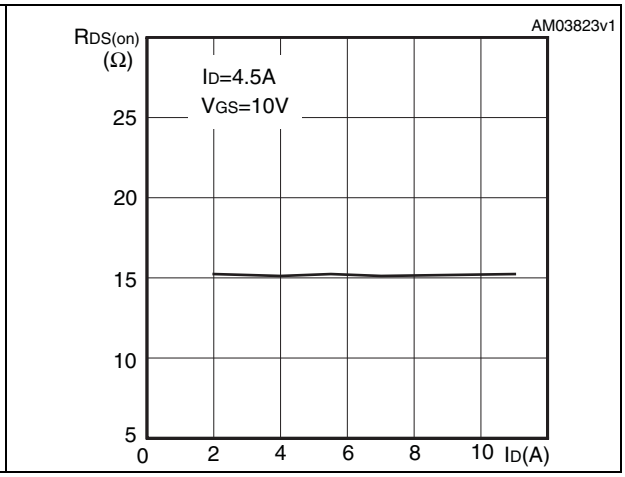


**Figure 8. Gate charge vs gate-source voltage**

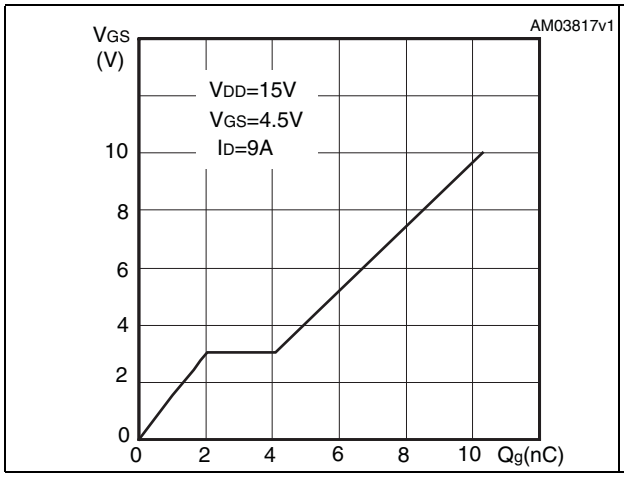



**Figure 9. Capacitance variations**

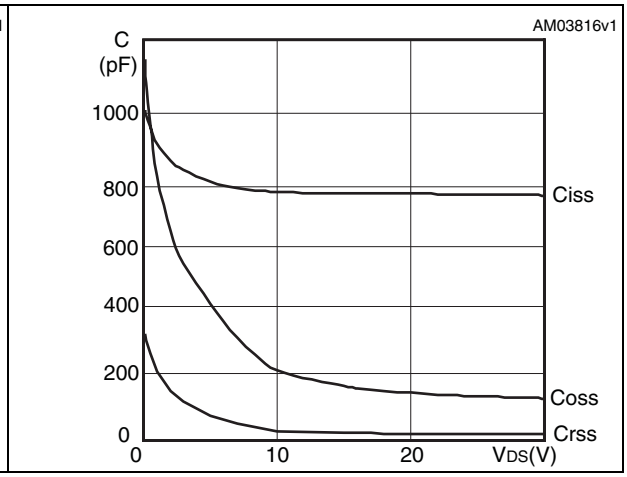



**Figure 10. Normalized gate threshold voltage vs temperature**

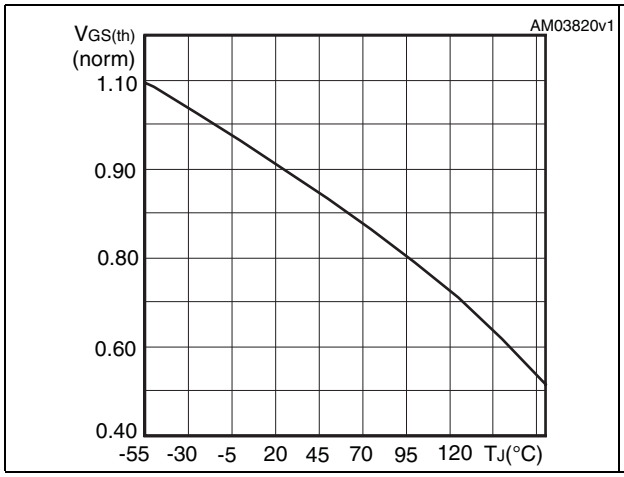



**Figure 11. Normalized on resistance vs temperature**

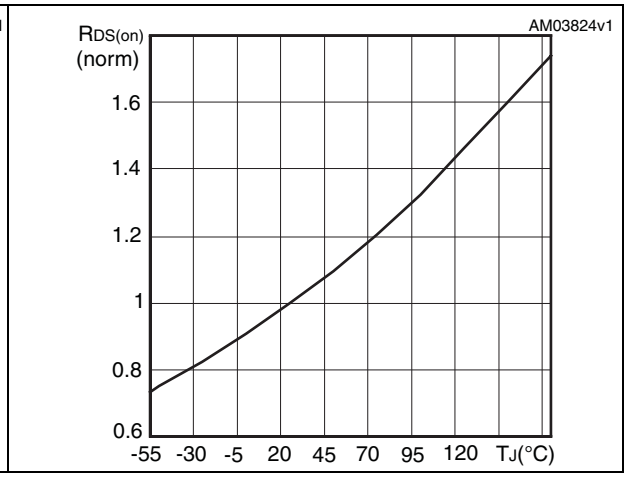
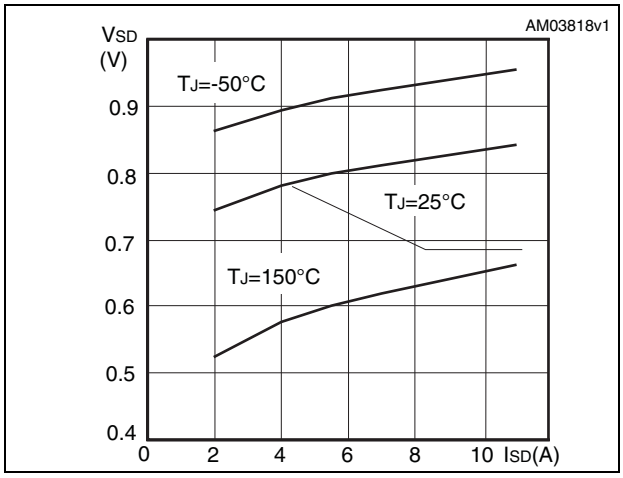



**Figure 12. Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**

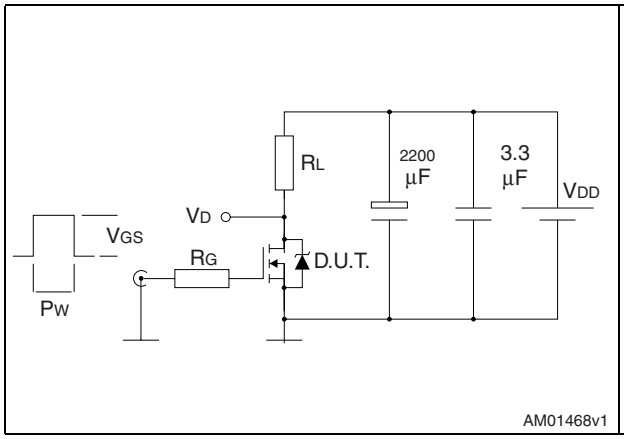



**Figure 14. Gate charge test circuit**

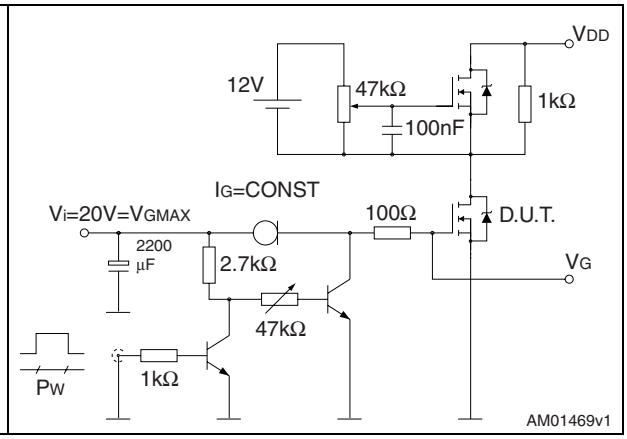



**Figure 15. Test circuit for inductive load switching and diode recovery times**

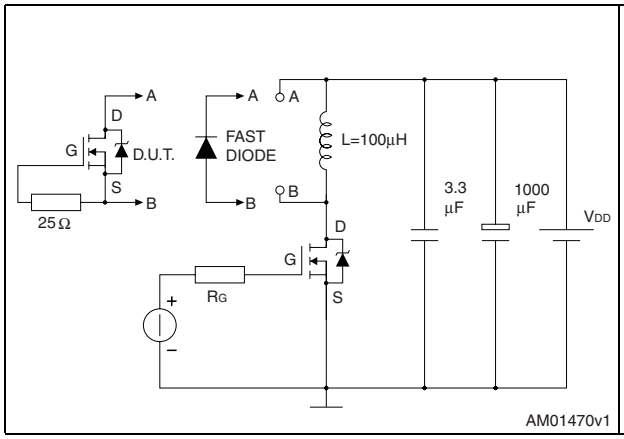



**Figure 16. Unclamped inductive load test circuit**

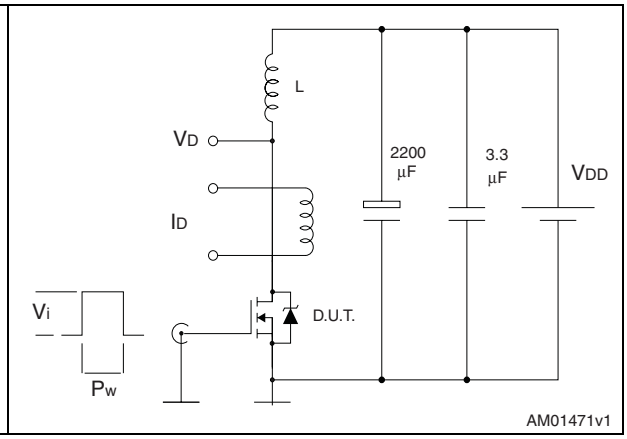



**Figure 17. Unclamped inductive waveform**

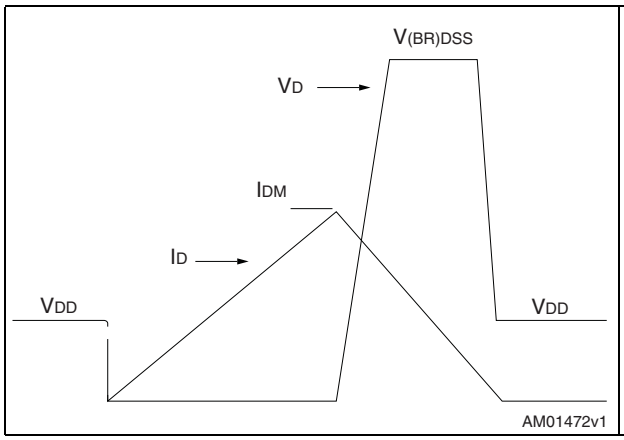
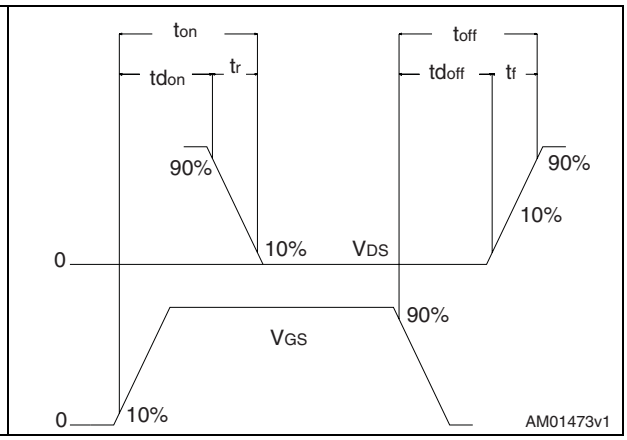



**Figure 18. Switching time waveform**

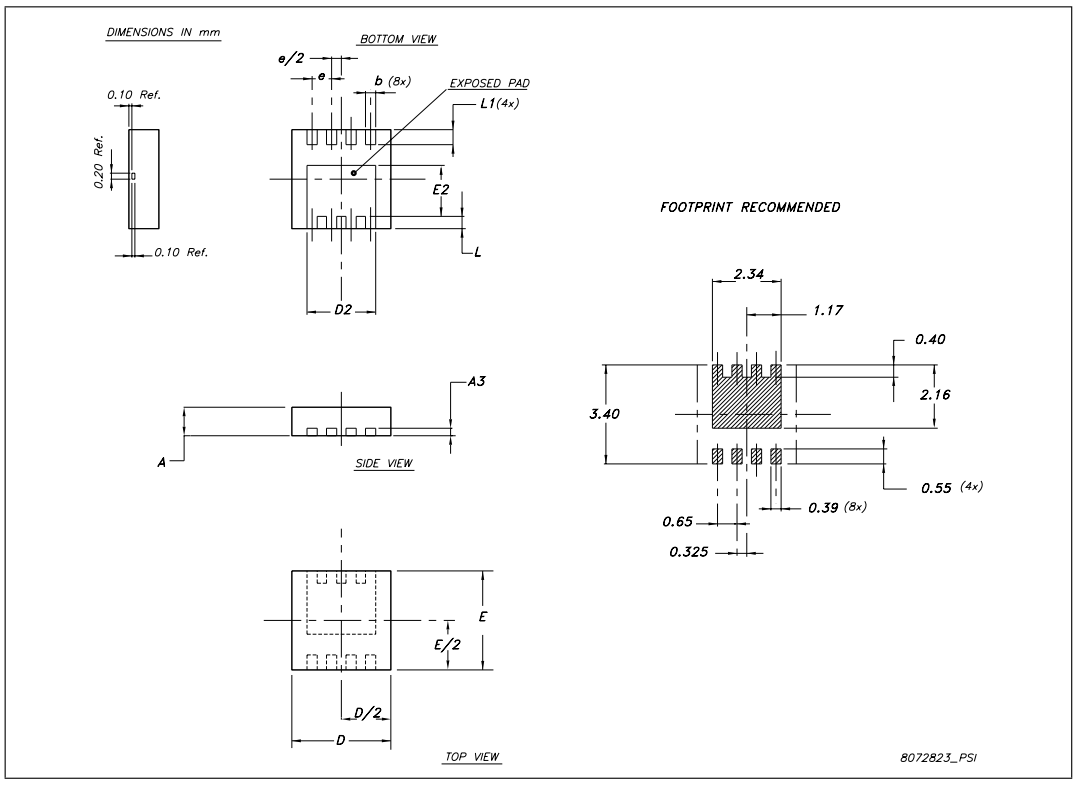


# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## PowerFLAT™ ( 3.3 x 3.3) mechanical data

| Dim | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.950 | | 1.000 | 0.037 | | 0.039 |
| A3 | | 0.200 | | | 0.008 | |
| b | 0.29 | 0.34 | 0.39 | 0.011 | 0.013 | 0.015 |
| D | 3.200 | 3.300 | 3.400 | 0.126 | 0.123 | 0.134 |
| D2 | 2.24 | 2.29 | 2.34 | 0.088 | 0.090 | 0.092 |
| E | 2.20 | 3.30 | 3.40 | 0.086 | 0.123 | 0.1338 |
| E2 | 1.660 | 1.710 | 1.760 | 0.065 | 0.067 | 0.069 |
| e | | 0.650 | | | 0.025 | |
| L | | 0.40 | | | 0.0157 | |
| L1 | 0.45 | 0.50 | 0.55 | 0.017 | 0.0196 | 0.021 |



# 5 Revision history

Table 8. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 09-Jul-2009 | 1 | First release |

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