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SAA5025
Teletext Timing Chain for USA 525-Line System

Product Specification

Linear Products

DESCRIPTION

The SAA5025 is a MOS N-channel integrated circuit which performs the timing functions for a Teletext system. It provides the necessary timing signals to extract data from a memory and produce a display according to the USA 525-line television standard (system M).

The SAA5025 may be used in conjunction with the SAA5030 (Teletext video processor; VIP) the SAA5050 (Teletext character generator; TROM), the SAA5040B (Teletext acquisition control; TAC) and the SAA5045 (Gearing and Address Logic Array; GALA).

FEATURES

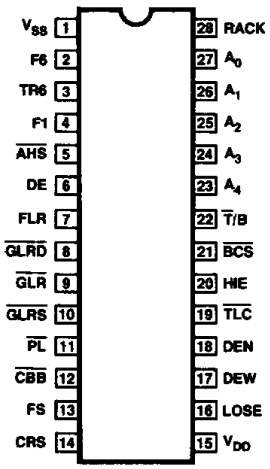
- **Designed to operate with USA 525-line television standard (system M)**
- **For 24 row (8 TV lines per row) × 40 character display**
- **Big character select input for double-height characters**
- **Composite sync signal output for display time-base synchronization**

APPLICATIONS

- **Teletext**
- **Telecaptioning**
- **Videotex**
- **Phase-locking with incoming video (when used with SAA5030)**
- **Composite sync generator**
- **Low cost display systems (when used with SAA5050 series)**

PIN CONFIGURATION

N Package



TOP VIEW

CD12310S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{SS}	Ground
2	F6	6.0419MHz clock input
3	TR6	6.0419MHz clock output
4	F1	1.007MHz clock output
5	$\overline{AHS}$	After hours sync output
6	DE	Display enable input
7	FLR	Fast line reset input
8	$\overline{GLRD}$	General line reset delay output
9	$\overline{GLR}$	General line reset output
10	$\overline{GLRS}$	General line reset starting output
11	$\overline{PL}$	Phase-locked open-drain output
12	$\overline{CBB}$	Color burst blanking output
13	FS	Field (picture) sync input
14	CRS	Character rounding select output
15	V_{DD}	Positive supply (+5V)
16	LOSE	Load output shift register enable output
17	DEW	Data entry window output
18	DEN	Display enable output (negative-going)
19	$\overline{TLC}$	Transmitted large characters input
20	HIE	High impedance enable input
21	$\overline{BCS}$	Big character select input
22	$\overline{T}$/B	Top/bottom select input
23	A_4	Memory row address outputs (3-state)
24	A_3	
25	A_2	
26	A_1	
27	A_0	
28	RACK	Read address clock output

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117D)	−20°C to +70°C	SAA5025DN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.3 to +7.5	V
V_I	Input voltage range[1]	−0.3 to +7.5	V
V_{OHZ}	High-impedance state output voltage	−0.3 to +7.5	V
V_{ODD}	Open-drain output voltage	−0.3 to +13.2	V
	Electrostatic charge protection on all inputs and outputs[2, 3]	1000	V
P_{TOT}	Total power dissipation per package	275	mW
T_A	Operating ambient temperature range	−20 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTES:

1. See also characteristics on F6 input and Figure 8.
2. Equivalent to discharging a 250pF capacitor through a 1kΩ series resistor.
3. N.B.: the SAA5025 is not protected against TV tube flash-over.
4. All outputs are TTL compatible.

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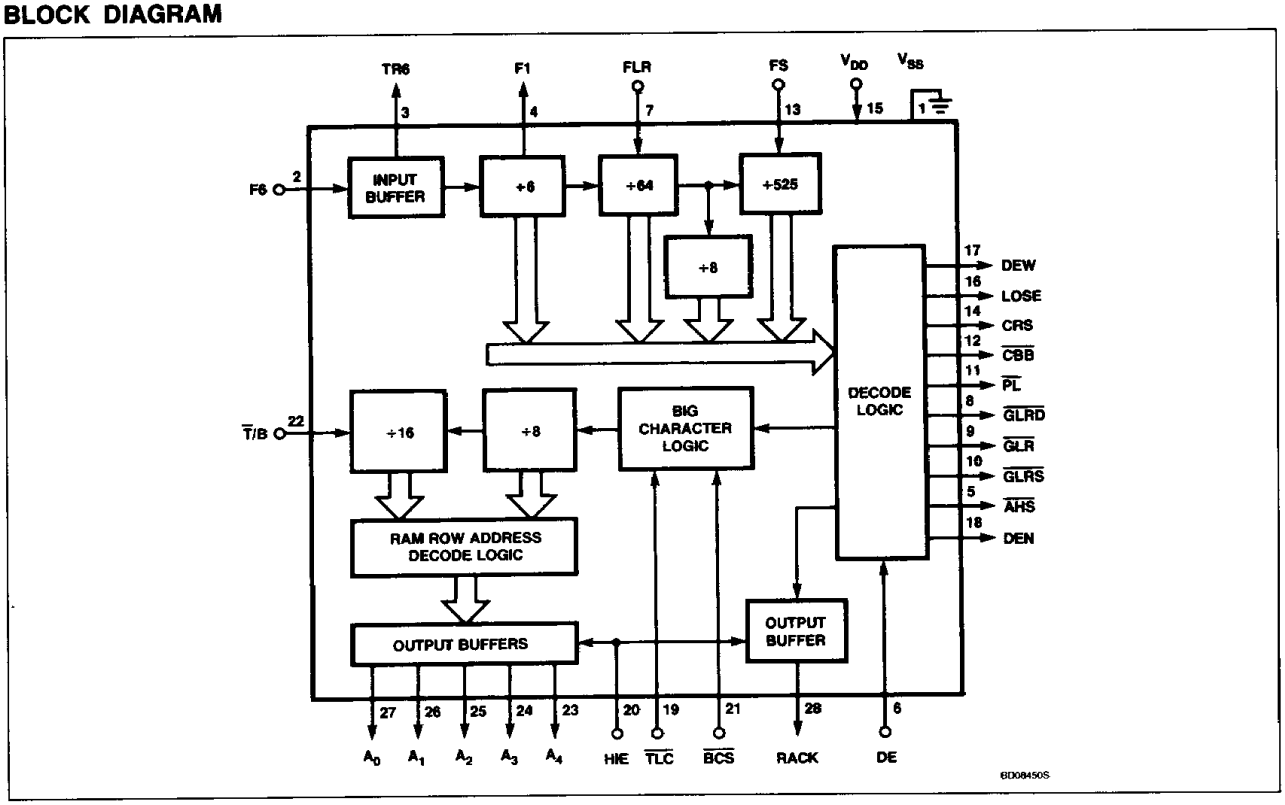
Teletext Timing Chain for USA 525-Line System — SAA5025

BLOCK DIAGRAM



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DC AND AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; F6 input frequency = 6.041957MHz, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
Supply						
V_{DD}	Supply voltage		4.5	5.0	5.5	V
I_{DD}	Supply current	5	5		50	mA
Inputs						
	Input leakage currents					
I_I	F6	5.5	0.2		10	μA
$-I_I$		0			10	μA
$\pm I_I$	FLR, $\overline{TLC}$, FS, HIE, $\overline{BCS}$, $\overline{T}$/B, DE	0 to 5.5			10	μA
C_I	Input capacitance; all inputs	5			7	pF
	High level input voltages					
V_{IH}	F6 (see Figure 8)	5	2.7		6.5	V
V_{IH}	FLR, $\overline{TLC}$, FS, HIE, $\overline{BCS}$, $\overline{T}$/B, DE	5	2.0[1]		5.5	V
V_{IL}	Low level input voltage (all inputs); (see Figure 8)	5			0.8[1]	V
t_R, t_F	Input rise and fall time F6 (see Figure 4)	0 and 2.7			30	ns
δ	Input F6 duty factor (see Figure 8)	5	40	50	56	%
Outputs						
C_O	Output node capacitance (all outputs)	5			7	pF
$\pm I_O$	Output leakage current high-impedance state; A_0 to A_4, RACK	0 to 5.5			10	μA
I_O	Output leakage current open-drain; $\overline{PL}$, $\overline{CBB}$	6			10	μA
Output TR6 6.041957MHz clock						
V_{OH}	High level output voltage $-I_{OH}$ = 100μA	5	2.75		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 100μA	5	0		0.4	V
C_L	Output load capacitance	5			15	pF
t_R, t_F	Output rise and fall times (see Figure 5)	5			30	ns
δ	Duty factor at 1.5V level depends on input F6 (see F6 data and Figure 8)	5	40		60	%
Output F1 1.007MHz clock						
V_{OH}	High level output voltage $-I_{OH}$ = 100μA	5	2.75		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 100μA	5	0		0.4	V
C_L	Output load capacitance	5			40	pF
t_R, t_R	Output rise and fall times (see Figure 5)	5			50	ns
t_{PHL}, t_{PLH}	Propagation delays from rising edge of TR6 (see Figure 6) High-to-Low and Low-to-High	5	7		60	ns
δ	Duty factor at 1.5V level	5	45	50	52	%

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

T_A = 25°C; F6 input frequency = 6.041957MHz, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
Output $\overline{AHS}$ (see Figure 6)						
V_{OH}	High level output voltage $-I_{OH}$ = 200μA	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 1.6mA	5	0		0.4	V
C_L	Output load capacitance	5			30	pF
t_R, t_F	Output rise and fall times (see Figure 7)	5			100	ns
t_{PLH}	Propagation delay from rising edge of F1 (see Figure 8) Low-to-High	5	0		350	ns
Outputs $\overline{GLR}$, $\overline{GLRD}$, $\overline{GLRS}$ (see Figure 3)						
V_{OH}	High level output voltage $-I_{OH}$ = 100μA	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 0.8mA	5	0		0.4	V
C_L	Output load capacitance	5			40	pF
t_R t_F	Output rise and fall times (see Figure 7)	5			70 50	ns ns
t_{PHL}, t_{PLH}	Propagation delay from rising edge of F1 (see Figure 8) High-to-Low and Low-to-High	5	0		300	ns
Output $\overline{PL}$ (see Figure 3)						
V_{OL}	Low level output voltage I_{OL} = 2mA	5	0		1.0	V
C_L	Output load capacitance	5			30	pF
t_F	Output fall time (see Figure 7)	5			100	ns
t_{PLH}	Propagation delay from rising edge of F1 (see Figure 8) Low-to-High	5	0		250	ns
Output $\overline{CBB}$ (see Figure 2)						
V_{OL}	Low level output voltage I_{OL} = 2mA	5	0		1.0	V
C_L	Output load capacitance	5			30	pF
t_F	Output fall time (see Figure 5)	5			200	ns
t_{PLH}	Propagation delay from rising edge of F1 (see Figure 6) Low-to-High	5	0		250	ns
Output CRS						
V_{OH}	High level output voltage $-I_{OH}$ = 100μA	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 100μA	5	0		0.4	V
C_L	Output load capacitance	5			30	pF
t_R, t_F	Output rise and fall times (see Figure 5)	5			1	μs

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

T_A = 25°C; F6 input frequency = 6.041957MHz, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
Output LOSE (see Figure 1)						
V_{OH}	High level output voltage $-I_{OH}$ = 100μA	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 100μA	5	0		0.4	V
C_L	Output load capacitance	5			30	pF
t_R, t_F	Output rise and fall times (see Figure 5)	5			50	ns
t_{PHL}, t_{PLH}	Propagation delay from rising edge of F1 (see Figure 6) High-to-Low and Low-to-High	5	0		1	μs
Output DEN						
V_{OH}	High level output voltage $-I_{OH}$ = 200μA	5	2.4			V
V_{OL}	Low level output voltage I_{OL} = 100μA	5			0.4	V
C_L	Output load capacitance	5			30	pF
t_R, t_F	Output rise and fall times	5			50	ns
t_{PHL}, t_{PLH}	Propagation delay from rising edge of F1; High-to-Low and Low-to-High	5			250	ns
Output DEW (see Figure 2)						
V_{OH}	High level output voltage $-I_{OH}$ = 200μA	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 1.6mA	5	0		0.4	V
C_L	Output load capacitance	5			50	pF
t_R, t_F	Output rise and fall times	5			200	ns
t_{PHL}, t_{PLH}	Propagation delay from rising edge of $\overline{CBB}$ (see Figure 6) High-to-Low and Low-to-High	5	6.5	6.96	7.5	μs
Outputs A_0 to A_4 (see Figure 2)						
V_{OH}	High level output voltage $-I_{OH}$ = 100μA	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 1.6mA	5	0		0.4	V
C_L	Output load capacitance	5			85	pF
t_R, t_F	Output rise and fall times	5			1	μs
t_{PHL}, t_{PLH}	Propagation delay from falling edge of $\overline{CBB}$ (see Figure 6) High-to-Low and Low-to-High	5	6.5		9.0	μs
t_{PHZ}, t_{PLZ}	Propagation delay from rising edge of HIE to high-impedance state (see Figure 7)	5	0		0.9	μs
t_{PZH}, t_{PZL}	Propagation delay from falling edge of HIE to normal active state (see Figure 7)	5	1		2.9	μs

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

T_A = 25°C; F6 input frequency = 6.041957MHz, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
Output RACK (see Figures 1 and 2)						
V_{OH}	High level output voltage $-I_{OH}$ = 100μA	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 1.6mA	5	0		0.4	V
C_L	Output load capacitance	5			40	pF
t_R t_F	Output rise and fall times (see Figure 5)	5			60 300	ns ns
t_{PHL}	Propagation delay from falling edge of F1 (see Figure 6) High-to-Low	5	150		280	ns
t_{PHZ}, t_{PLZ}	Propagation delay from rising edge of HIE to high-impedance state (see Figure 7)	5	1		2.9	μs
t_{PZH}, t_{PZL}	Propagation delay from falling edge of HIE to normal active state (see Figure 7)	5	0		0.9	μs

NOTE:
1. These values give no noise immunity.

FUNCTIONAL DESCRIPTION

The basic input to the SAA5025 is a 6.0419MHz clock signal (e.g., from SAA5030). The clock input (F6) is buffered and also available as an output at TR6 to provide a dot rate clock. The signal at F6 is divided by 6 to produce the 1.007MHz character rate clock at output F1, which is in turn divided by 64 to produce the line period of 63.556μs. A divide-by-262 or 263 counter, clocked at line rate, produces a field (picture) period of 16.683ms (average), i.e., 33.366ms for divide-by-525. The display format is 40 characters per row for 24 rows (1 row is 8 TV lines).

A big character select ($\overline{BSC}$) input is provided and it enables double-height characters (16 TV lines per row) to be displayed. The top or bottom select ($\overline{T}/B$) input must be used in conjunction with $\overline{BCS}$ to select either the top half or bottom half of the page to be displayed on the television screen.

A composite sync ($\overline{AHS}$) output is available for synchronizing the display timebase. A high-impedance enable (HIE) input is included to switch the read address clock (RACK) and the memory row address (A_0 to A_4) outputs into their high-impedance states.

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Teletext Timing Chain for USA 525-Line System

SAA5025

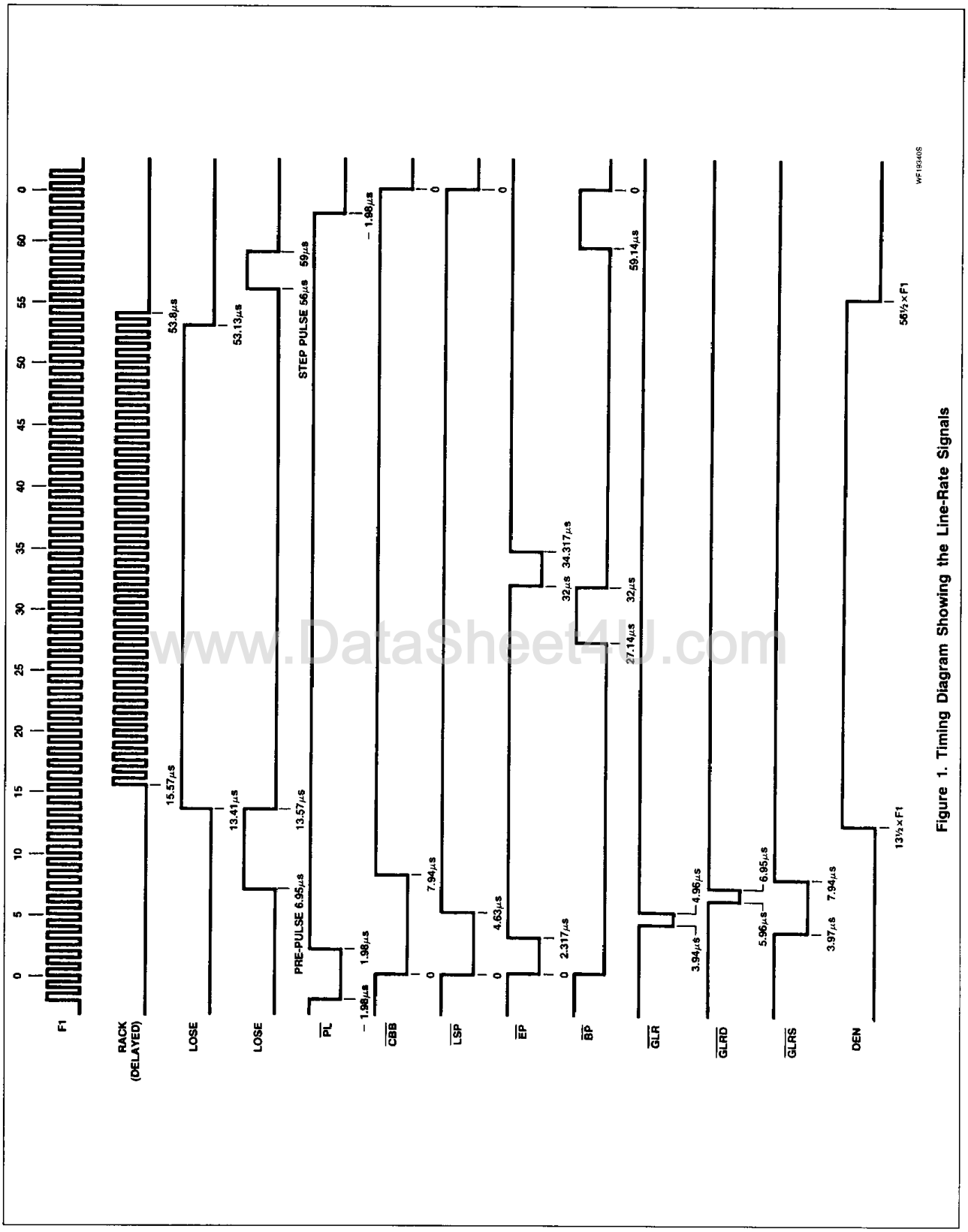

Figure 1. Timing Diagram Showing the Line-Rate Signals

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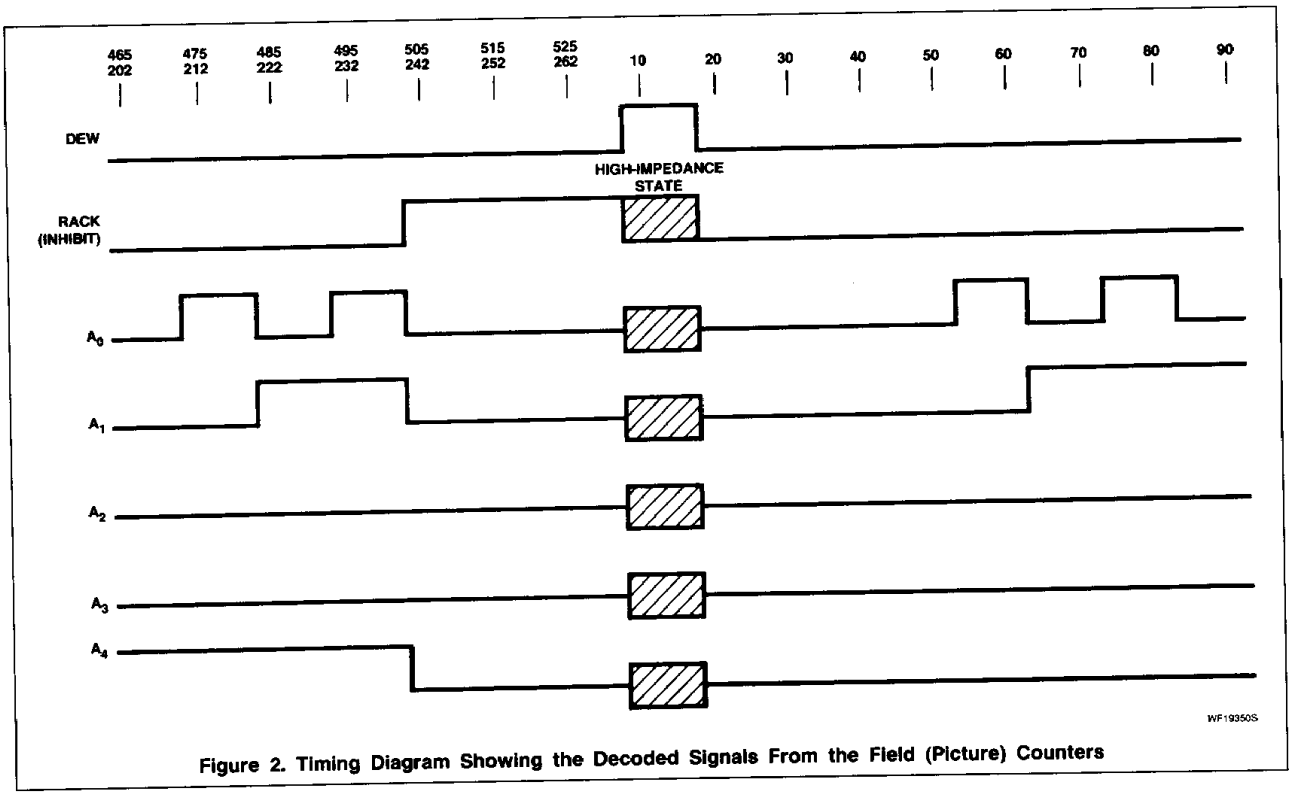

Figure 2. Timing Diagram Showing the Decoded Signals From the Field (Picture) Counters

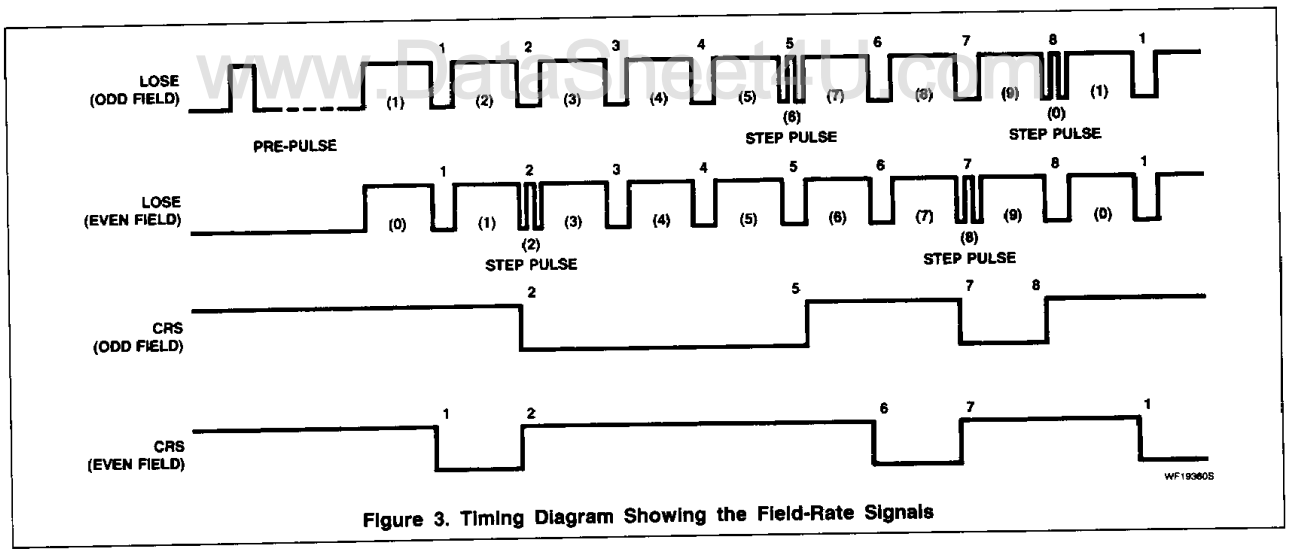

Figure 3. Timing Diagram Showing the Field-Rate Signals

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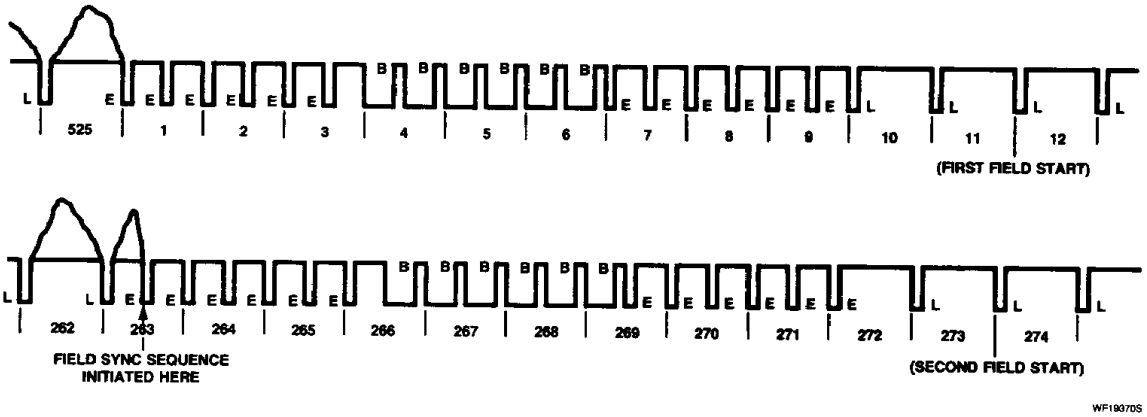
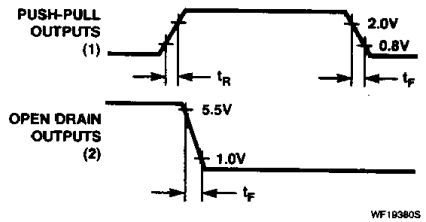


NOTES:
L = line sync pulses (4.2 to 5.1μs)
E = equalizing pulses (2.29μs ± 10%)
B = broad pulses (26.4 to 28μs)

Figure 4. After-Hours Sync Waveforms



NOTES:
1. These outputs will be tested with simulated TTL loads and with the load resistors adjusted such that the correct current conditions are obtained.
2. These outputs will be tested with 3kΩ resistors to the +6V line for outputs $\overline{PL}$ and $\overline{CBB}$.

Figure 5. Definition of the Rise and Fall Times for the Output Stages

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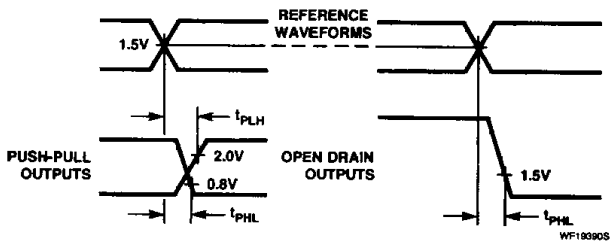

Figure 6. Definition of the Propagation Delays for the Output Stages

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Teletext Timing Chain for USA 525-Line System

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APPLICATION INFORMATION

The function is described following the corresponding pin number.

1 V_{SS} — Ground (0V)

2 F6 6.041957MHz Clock Input — Obtained from video processor (SAA5030) or other source. The permissible mark/space ratio is in the range from 56:44 to 40:60 (see also Figure 8).

3 TR6 6.041957MHz Clock Output — Dot-rate clock for Teletext character generator SAA5050 series.

4 F1 1.007MHz Clock Output — Character-rate clock for Teletext character generator SAA5050 series.

5 $\overline{AHS}$ After-Hours Sync Output — A composite sync waveform consisting of a successive sequence of line sync pulses ($\overline{LSP}$) followed by six equalizing pulses ($\overline{EP}$), six broad pulses ($\overline{BP}$), and six equalizing pulses ($\overline{EP}$), and is followed by another sequence of $\overline{LSP}$. This composite sync waveform occurs at the end and beginning of each field/picture (see also Figure 4).

6 DE Display Enable Input — A Low level signal from the Teletext acquisition and control circuit (SAA5040 series) to this input switches output DEN to the Low state.

7 FLR Fast Line Reset Input — This is the input for a positive-going pulse with a duration of 0.5μs to 63μs which resets the line rate counter (÷64). After accepting an FLR pulse, further resets are inhibited for one line period of approximately 63.5μs.

8 $\overline{GLRD}$ General Line Reset Delay Output — A negative-going pulse with a duration of 993ns which commences 5.96μs from the start of each line (see also Figure 1).

9 $\overline{GLR}$ General Line Reset Output — A negative-going pulse with a duration of 993ns which commences 3.97μs from the start of each line (see also Figure 1).

10 $\overline{GLRS}$ General Line Reset Starting Output — A negative-going pulse with starting 3.97μs and ending 7.94μs from the start of each line (see also Figure 1).

11 $\overline{PL}$ Phase-Locked Open-Drain Output — This open-drain output is used to lock the oscillator in the SAA5030 to the line rate. It is a negative-going pulse with a duration of 3.96μs which starts at 61.58μs on one line and ends at 1.98μs after the start of the following line (see also Figure 1).

12 $\overline{CBB}$ Color Burst Blanking Output — This open-drain output blanks the color burst in the SAA5030. It is a 7.94μs negative-going pulse which starts at the beginning of each line (t = 0; see also Figure 1).

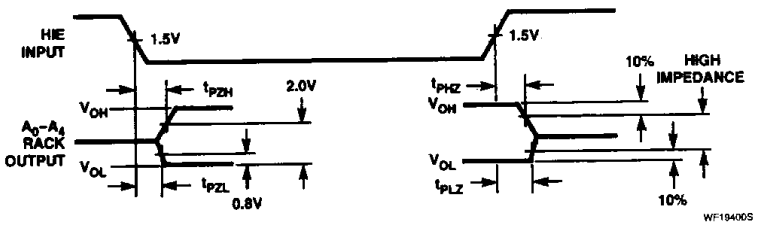
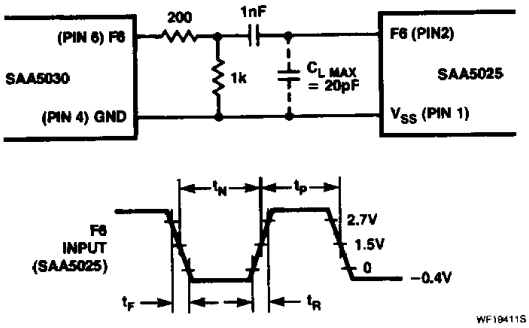


Figure 7. Definitions of the High-Impedance State Propagation Delay Times



NOTES:
1. With this circuitry the F6 input will be set to a level of approximately –0.4V in the low state. This is acceptable as the internal clamping diode in the F6 input of the SAA5025 provides an adequate current clamp.
2. Also shown is the F6 input waveform with the appropriate definitions.
3. The duty factor is defined as: $\frac{t_P}{t_P + t_N} \times 100\%$.

Figure 8. Recommended 6MHz Interface Circuitry Between the SAA5025 and the SAA5030 (Input F6)

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13 FS Field (Picture) Sync Input — This input accepts a positive-going pulse of approximately 160μs duration. Its leading edge occurs during the second half of line one on even fields (half picture) and correspondingly in odd fields (other half picture). It is ignored during the odd field.

14 CRS Character Rounding Select Output — The output signal starts High during the even field (lines 1 to 263), goes Low after the first LOSE pulse, again High after the second LOSE pulse, then Low after the sixth LOSE pulse, and finally High at the end of the seventh LOSE pulse. This sequence repeats every 8 lines (every row) for the entire display period (see also Figure 3). For the odd field (lines 264 to 525) CRS starts High, goes Low after the second LOSE pulse, again High after the fifth LOSE pulse, then Low after the seventh LOSE pulse and finally High at the end of the eighth LOSE pulse. This sequence repeats every 8 lines (every row) for the entire display period (see also Figure 3).

15 V_{DD} Positive Supply — (+5V)

16 LOSE Load Output Shift Register Enable Output — This is a positive-going output pulse of 39.72μs duration commencing 13.41μs from start of line valid during line 47 to 238 inclusive, for the even field. A step-pulse starting at the count of 3 character rate clock pulses (F1) after the second and seventh LOSE pulses and at the count of 3 character rate clock pulses repeated every row is included. For the odd field, the LOSE pulse is preceded by a pre-pulse of 7μs duration commencing 7.41μs in line 20, and has a step-pulse after the fifth and eighth pulse, repeated every row (see also Figure 3).

17 DEW Data Entry Window Output — This output defines the period during which data may be extracted from the incoming television signal. It is High during lines 7 to 18 inclusive for the even fields and line 270 to 281 inclusive for the odd fields. The positive-going pulse has a duration of 762.67μs and commences at 6.95μs from the start of the line (see also Figure 2).

18 DEN Display Enable Output — The output pulse is positive-going at 13.5μs from the start of a line to 56.5μs and is active during line 47 to 238 inclusive if the DE input is High. If the DE input is Low, the DEN is held in the Low state.

19 $\overline{TLC}$ Transmitted Large Characters Input — When this input is Low, it enables rows of double-height characters to be displayed as required. Large characters descend into the next memory row address location. $\overline{TLC}$ is

13

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always High (i.e., small) for the first line of a row, even if it contains large characters.

20 HIE High Impedance Enable Input — When this input is in the High state, it will force the RACK and memory row address output into the high-impedance state. For normal Teletext operation, this input should be connected to the DEW output (Pin 17).

21 $\overline{BCS}$ Big Character Select Input — For normal size character display, this input signal must be High while a Low gives double-height characters.

22 $\overline{T}$/B Top/Bottom Select Input — When both $\overline{BCS}$ and $\overline{T}$/B are Low, the top half of a page is displayed with double-height characters. If $\overline{T}$/B is High and $\overline{BCS}$ is Low, the bottom half of the page is also displayed with double-height characters.

23 to 27 A_0 to A_4 Memory Row Address Outputs (3-State) — These binary count outputs sequencing from 00000 (count 0) to address 10111 (count 23) for the 40 × 24 format.

The binary count changes every 8 TV lines per row in the display period of line 47 to 238 inclusive for the 24-row display. The count changes between 6.5μs and 9.0μs during the line period.

28 RACK Read Address Clock Output — This is the read address clock output to the SAA5045 (GALA) column address counter during the display period. It consists of 39 positive pulses at the 1.007MHz rate starting at 13.57μs from the start of the line period with the last negative edge occurring at 51.8μs. This sequence is active on line 45 to 238 inclusive. RACK is delayed by two F1 clock periods for the whole of the field when input DE is Low for the whole of line 39. On lines 19 to 44 inclusive, output RACK is permanently delayed by two F1 clock periods, unaffected by DE.

NOTES:

1. In the big character top mode the memory row address count is 0 to 11, and in the big character bottom mode the count is 12 to 23. Each big character row is equal to 16 television lines.
2. The memory row addresses are held Low for one line period starting 6.5μs to 9μs from the beginning of line 36 which is only valid in the big character bottom mode.

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