Integrated Device Technology, Inc.

# 64K x 32 CMOS STATIC RAM MODULE

**IDT7MP4036**

INTEGRATED DEVICE

## FEATURES:

- High-density 2MB Static RAM module
- Low profile 64-pin ZIP (Zig-zag In-line vertical Package) or 64-pin SIMM (Single In-line Memory Module)
- Ultra fast access time: 12ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

## PIN CONFIGURATION[1]

| | | | | |
|---|---|---|---|---|
| | | 1 | GND | |
| PD0 | 2 | 3 | PD1 | PD0 –OPEN |
| I/O0 | 4 | 5 | I/O8 | PD1 – GND |
| I/O1 | 6 | 7 | I/O9 | |
| I/O2 | 8 | 9 | I/O10 | |
| I/O3 | 10 | 11 | I/O11 | |
| VCC | 12 | 13 | A0 | |
| A7 | 14 | 15 | A1 | |
| A8 | 16 | 17 | A2 | |
| A9 | 18 | 19 | I/O12 | |
| I/O4 | 20 | 21 | I/O13 | |
| I/O5 | 22 | 23 | I/O14 | |
| I/O6 | 24 | 25 | I/O15 | |
| I/O7 | 26 | 27 | GND | |
| $\overline{WE}$ | 28 | 29 | A15 | |
| A14 | 30 | 31 | $\overline{CS_2}$ | |
| $\overline{CS_1}$ | 32 | | | |
| | | 33 | $\overline{CS_4}$ | |
| $\overline{CS_3}$ | 34 | 35 | NC | |
| NC | 36 | 37 | $\overline{OE}$ | |
| GND | 38 | 39 | I/O24 | |
| I/O16 | 40 | 41 | I/O25 | |
| I/O17 | 42 | 43 | I/O26 | |
| I/O18 | 44 | 45 | I/O27 | |
| I/O19 | 46 | 47 | A3 | |
| A10 | 48 | 49 | A4 | |
| A11 | 50 | 51 | A5 | |
| A12 | 52 | 53 | VCC | |
| A13 | 54 | 55 | A6 | |
| I/O20 | 56 | 57 | I/O28 | |
| I/O21 | 58 | 59 | I/O29 | |
| I/O22 | 60 | 61 | I/O30 | |
| I/O23 | 62 | 63 | I/O31 | |
| GND | 64 | | | |

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**ZIP, SIMM TOP VIEW**

**NOTE:**

1. Pins 2 and 3 (PD0 and PD1) are read by the user to determine the density of the module. If PD0 reads Open and PD1 reads GND, then the module had a 64K depth.

## DESCRIPTION:

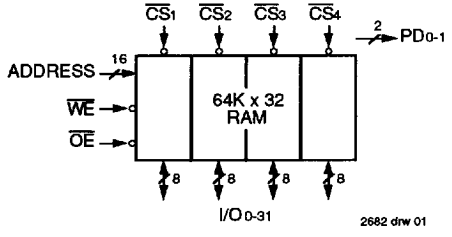
The IDT7MP4036 is a 64K x 32 Static RAM module constructed on an epoxy laminate (FR-4) substrate using eight 64K x 4 StaticRAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 256K StaticRAMs fabricated in IDT's high-performance, high-reliability CMOS technology. The IDT7MP4036 is available with access time as fast as 12ns with minimal power consumption.

The IDT7MP4036 is packaged in a 64-pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64-pin SIMM (Single In-line Memory Module). The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.50 inches high, this low-profile package is ideal for systems with minimum board spacing, while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4036 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 64K depth.

## FUNCTIONAL BLOCK DIAGRAM

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## PIN NAMES

| | |
|---|---|
| I/O0–31 | Data Inputs/Outputs |
| A0–15 | Addresses |
| $\overline{CS_{1-4}}$ | Chip Selects |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| PD0–1 | Depth Identification |
| VCC | Power |
| GND | Ground |
| NC | No Connect |

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## CAPACITANCE ($T_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter[1] | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN(D)}$ | Input Capacitance (Data) | $V_{(IN)}$ = 0V | 15 | pF |
| $C_{IN(A)}$ | Input Capacitance (Address & Control) | $V_{(IN)}$ = 0V | 70 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{(OUT)}$ = 0V | 15 | pF |

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**NOTE:**
1 This parameter is guaranteed by design but not tested

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| $V_{IH}$[2] | Input High Voltage | 2.2 | — | 6.0 | V |
| $V_{IL}$ | Input Low Voltage | –0.5[1] | — | 0.8 | V |

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**NOTES:**
1 $V_{IL}$ (min) = –1.5V for pulse width less than 10ns
2 I/O pins must not exceed $V_{CC}$ +0.5V.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade | Ambient Temperature | GND | Vcc |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |

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## TRUTH TABLE

| Mode | $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Output | Power |
|---|---|---|---|---|---|
| Standby | H | X | X | High-Z | Standby |
| Read | L | L | H | $DATA_{OUT}$ | Active |
| Write | L | X | L | $DATA_{IN}$ | Active |
| Read | L | H | H | High-Z | Active |

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## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{TERM}$[2] | Terminal Voltage with Respect to GND | –0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | 0 to +70 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –10 to +85 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | °C |
| IOUT | DC Output Current | 50 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. I/O pins must not exceed $V_{CC}$ +0.5V.

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5.0V ±10%, $T_A$ = 0°C to +70°C)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage (Address and Control) | $V_{CC}$ = Max., $V_{IN}$ = GND to $V_{CC}$ | — | 80 | µA |
| $\|I_{LI}\|$ | Input Leakage (Data) | $V_{CC}$ = Max., $V_{IN}$ = GND to $V_{CC}$ | — | 10 | µA |
| $\|I_{LO}\|$ | Output Leakage | $V_{CC}$ = Max., $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | — | 10 | µA |
| $V_{OL}$ | Output LOW | $V_{CC}$ = Min., $I_{OL}$ = 8mA | — | 0.4 | V |
| $V_{OH}$ | Output HIGH | $V_{CC}$ = Min., $I_{OH}$ = –4mA | 2.4 | — | V |

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| Symbol | Parameter | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $I_{CC}$ | Dynamic Operating Current | f = $f_{MAX}$, $\overline{CS}$ = $V_{IL}$<br>$V_{CC}$ = Max., Output Open | 1280 | mA |
| $I_{SB}$ | Standby Supply Current | $\overline{CS}$ ≥ $V_{IH}$, $V_{CC}$ = Max<br>Outputs Open, f = $f_{MAX}$ | 320 | mA |
| $I_{SB1}$ | Full Standby Supply Current | $\overline{CS}$ ≥ $V_{CC}$ – 0.2V; f = 0<br>$V_{IN}$ > $V_{CC}$ – 0.2V or < 0.2V | 240 | mA |

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## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figures 1, 2 |

2682 tbl 09

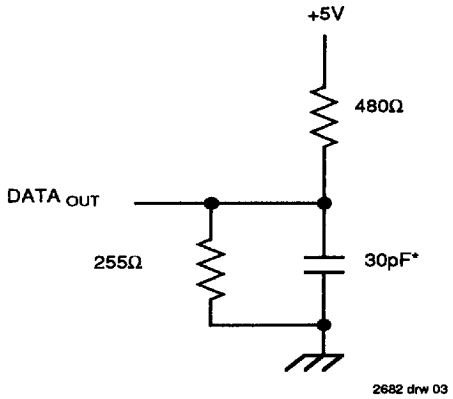


**Figure 1. Output Load**

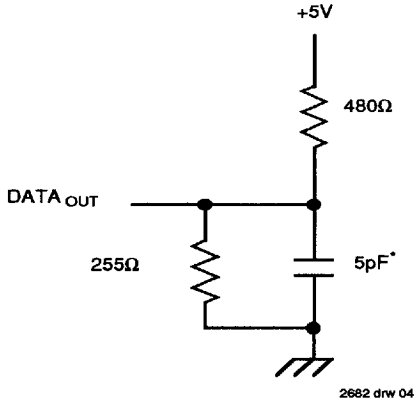


**Figure 2. Output Load**
**(for $t_{OLZ}$, $t_{OHZ}$, $t_{CHZ}$, $t_{CLZ}$, $t_{WHZ}$, $t_{OW}$)**

*incluces scope and jig.

## AC ELECTRICAL CHARACTERISTICS

INTEGRATED DEVICE

(Vcc = 5V ±10%, TA = 0°C to +70°C)

| Symbol | Parameter | 7MP4036SxxZ, 7MP4036SxxM | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | –12[2] | | –15 | | –17 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Read Cycle** | | | | | | | | |
| tRC | Read Cycle Time | 12 | — | 15 | — | 17 | — | ns |
| tAA | Address Access Time | — | 12 | — | 15 | — | 17 | ns |
| tACS | Chip Select Access Time | — | 12 | — | 15 | — | 17 | ns |
| tCLZ[1] | Chip Select to Output in Low-Z | 2 | — | 2 | — | 2 | — | ns |
| tOE | Output Enable to Output Valid | — | 7 | — | 9 | — | 10 | ns |
| tOLZ[1] | Output Enable to Output in Low-Z | 0 | — | 0 | — | 0 | — | ns |
| tCHZ[1] | Chip Deselect to Output in High-Z | — | 7 | — | 8 | — | 10 | ns |
| tOHZ[1] | Output Disable to Output in High-Z | — | 7 | — | 8 | — | 9 | ns |
| tOH | Output Hold from Address Change | 3 | — | 3 | — | 3 | — | ns |
| tPU[1] | Chip Select to Power-Up Time | 0 | — | 0 | — | 0 | — | ns |
| tPD[1] | Chip Deselect to Power-Down Time | — | 12 | — | 15 | — | 17 | ns |
| **Write Cycle** | | | | | | | | |
| tWC | Write Cycle Time | 12 | — | 15 | — | 17 | — | ns |
| tCW | Chip Select to End-of-Write | 10 | — | 12 | — | 14 | — | ns |
| tAW | Address Valid to End-of-Write | 11 | — | 13 | — | 15 | — | ns |
| tAS | Address Set-up Time | 1 | — | 1 | — | 1 | — | ns |
| tWP | Write Pulse Width | 10 | — | 12 | — | 14 | — | ns |
| tWR | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| tWHZ[1] | Write Enable to Output in High-Z | — | 7 | — | 8 | — | 9 | ns |
| tDW | Data to Write Time Overlap | 7 | — | 8 | — | 10 | — | ns |
| tDH | Data Hold from Write Time | 1 | — | 1 | — | 1 | — | ns |
| tOW[1] | Output Active from End-of-Write | 2 | — | 2 | — | 2 | — | ns |

**NOTES:**
1 This parameter is guaranteed by design, but not tested
2 Preliminary specifications only

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## AC ELECTRICAL CHARACTERISTICS

INTEGRATED DEVICE

($V_{CC}$ = 5V ±10%, $T_A$ = 0°C to +70°C)

| Symbol | Parameter | 7MP4036SxxZ, 7MP4036SxxM –20 Min. | –20 Max. | –25 Min. | –25 Max. | –35 Min. | –35 Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 20 | — | 25 | — | 35 | — | ns |
| $t_{AA}$ | Address Access Time | — | 20 | — | 25 | — | 35 | ns |
| $t_{ACS}$ | Chip Select Access Time | — | 20 | — | 25 | — | 35 | ns |
| $t_{CLZ}$(1) | Chip Select to Output in Low-Z | 3 | — | 3 | — | 3 | — | ns |
| $t_{OE}$ | Output Enable to Output Valid | — | 10 | — | 12 | — | 25 | ns |
| $t_{OLZ}$(1) | Output Enable to Output in Low-Z | 0 | — | 0 | — | 0 | — | ns |
| $t_{CHZ}$(1) | Chip Deselect to Output in High-Z | — | 10 | — | 15 | — | 22 | ns |
| $t_{OHZ}$(1) | Output Disable to Output in High-Z | — | 10 | — | 15 | — | 22 | ns |
| $t_{OH}$ | Output Hold from Address Change | 3 | — | 3 | — | 3 | — | ns |
| $t_{PU}$(1) | Chip Select to Power-Up Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{PD}$(1) | Chip Deselect to Power-Down Time | — | 20 | — | 25 | — | 35 | ns |
| **Write Cycle** | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 20 | — | 25 | — | 35 | — | ns |
| $t_{CW}$ | Chip Select to End-of-Write | 15 | — | 20 | — | 30 | — | ns |
| $t_{AW}$ | Address Valid to End-of-Write | 15 | — | 20 | — | 30 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width | 15 | — | 20 | — | 30 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{WHZ}$(1) | Write Enable to Output in High-Z | — | 12 | — | 15 | — | 18 | ns |
| $t_{DW}$ | Data to Write Time Overlap | 12 | — | 15 | — | 20 | — | ns |
| $t_{DH}$ | Data Hold from Write Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{OW}$(1) | Output Active from End-of-Write | 0 | — | 0 | — | 0 | — | ns |

**NOTE:**
1. This parameter is guaranteed by design, but not tested

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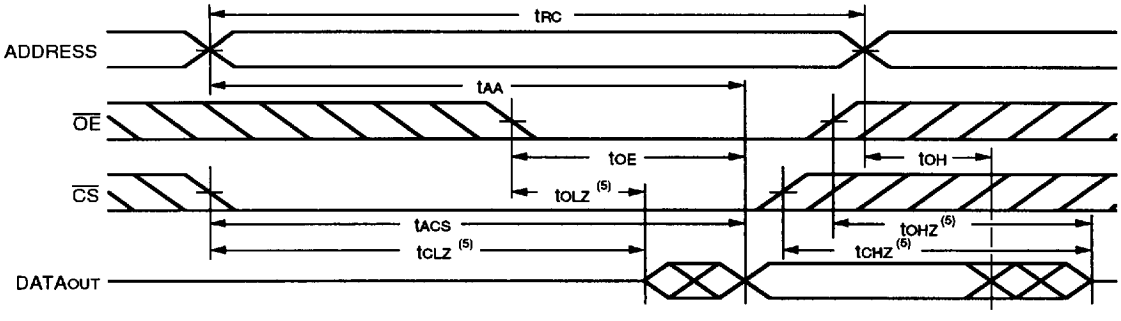
## TIMING WAVEFORM OF READ CYCLE NO. 1(1)

INTEGRATED DEVICE

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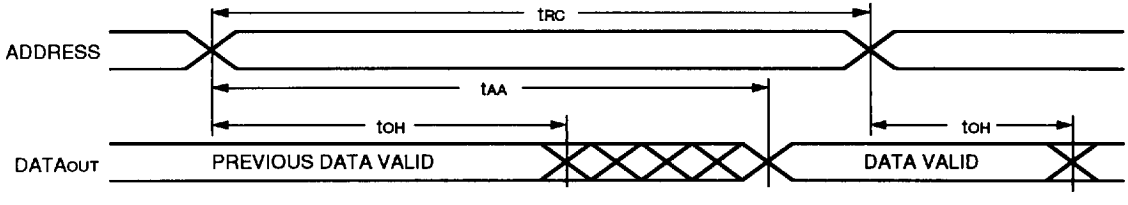
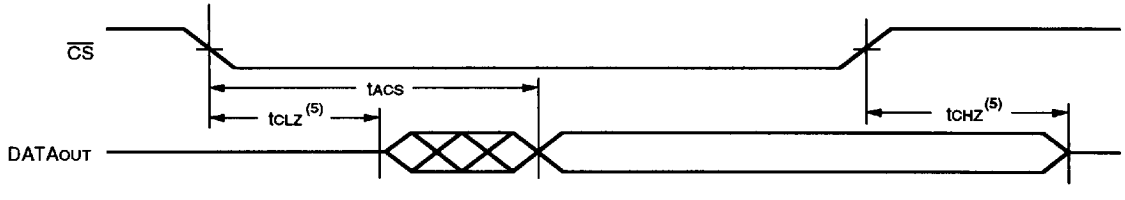
## TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)




2682 drw 08

## TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)




2682 drw 09

**NOTES:**
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = VIL
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

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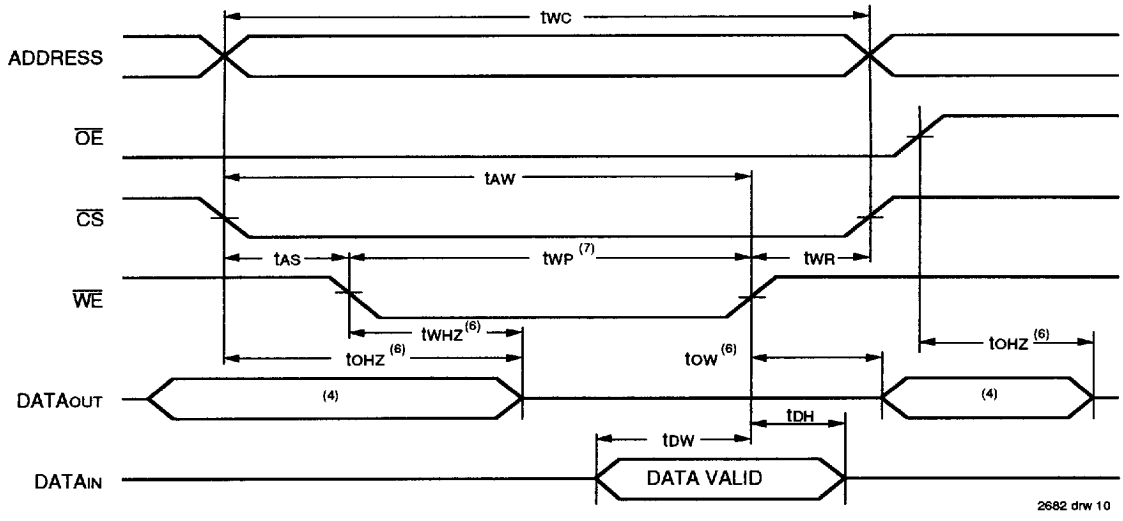
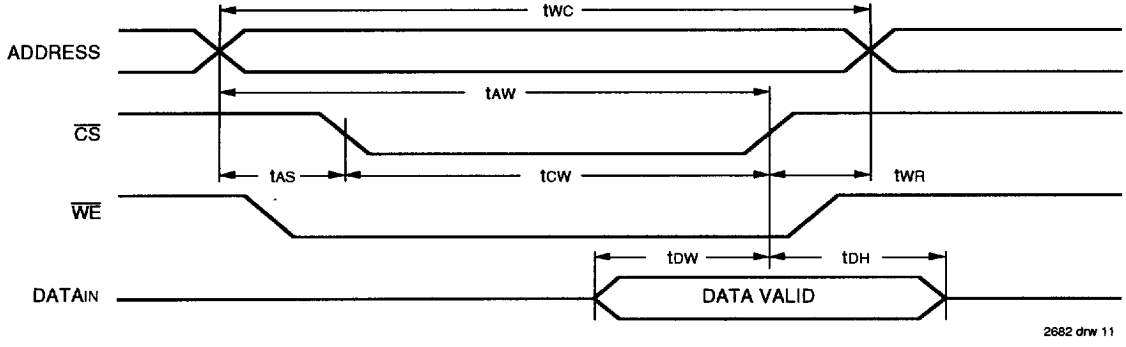
## TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLED TIMING)(1, 2, 3, 7)




INTEGRATED DEVICE

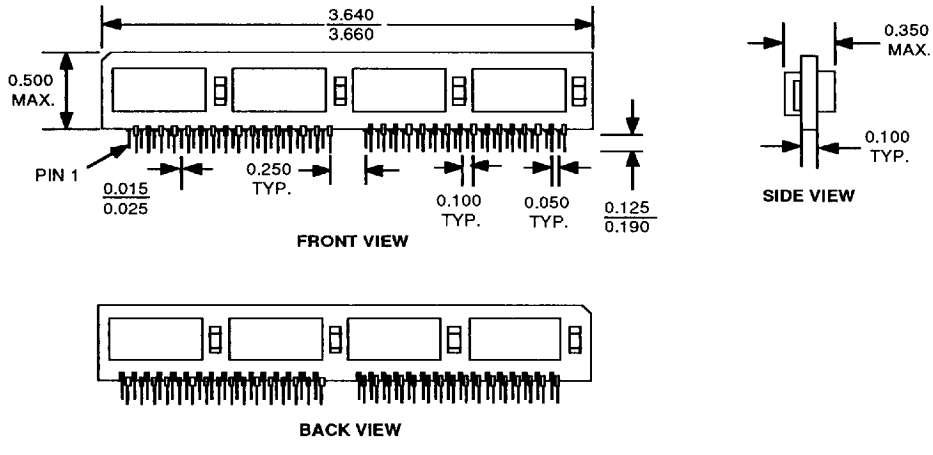
## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)




**NOTES:**
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but, not tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off data and to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

## PACKAGE DIMENSIONS

### ZIP VERSION

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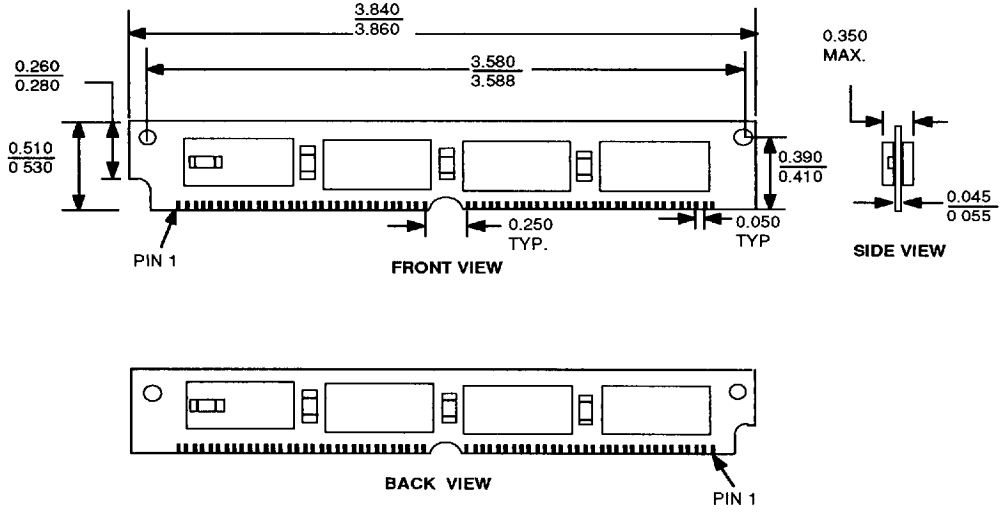
### SIMM VERSION

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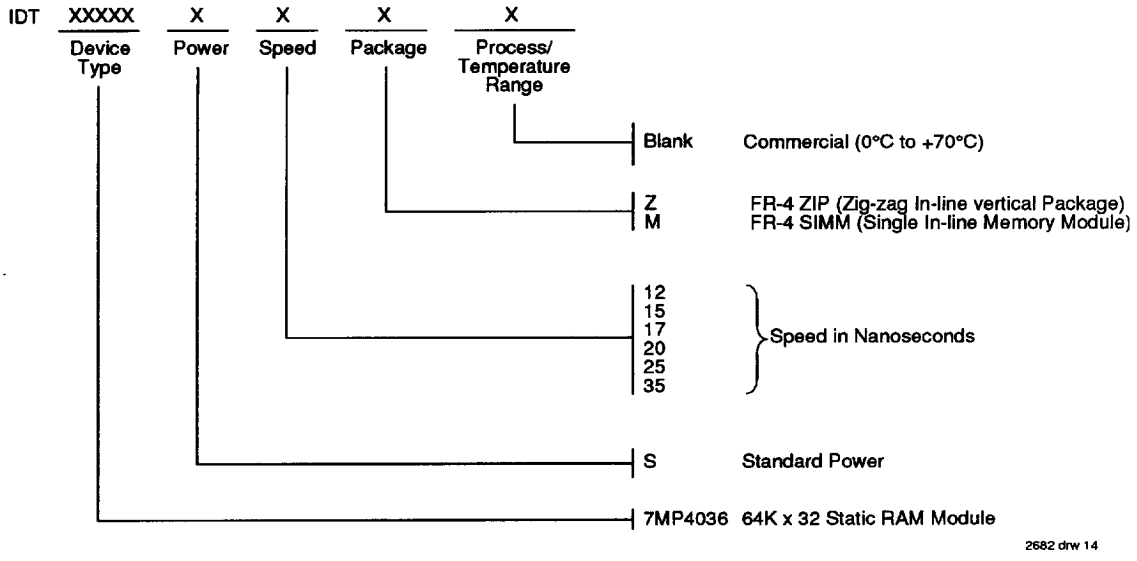
## ORDERING INFORMATION

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