



Integrated Device Technology, Inc.

128K/64K x 8 CMOS DUAL-PORT STATIC RAM MODULE

PRELIMINARY
IDT7MP1021
IDT7MP1023

FEATURES

- High density 1M/512K CMOS dual-port static RAM modules
- Fast access times: 25, 30, 35, 40, 50ns
- Fully asynchronous read/write operation from either port
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted plastic components on a 64-lead SIMM (Single In-line Memory Module)
- Multiple Vcc and GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Input/outputs directly TTL compatible

PIN CONFIGURATION

R_A(0)	2	3	VCC
R_A(1)	4	5	L_A(0)
R_A(2)	6	7	L_A(1)
R_A(3)	8	9	L_A(2)
R_A(4)	10	11	L_A(3)
GND	12	13	L_A(4)
R_A(5)	14	15	L_A(5)
R_A(6)	16	17	L_A(6)
R_A(7)	18	19	L_A(7)
R_A(8)	20	21	L_A(8)
R_A(9)	22	23	L_A(9)
R_A(10)	24	25	L_A(10)
R_A(11)	26	27	GND
R_OE	28	29	L_OE
R_RW	30	31	L_RW
R_SEM	32	33	L_SEM
R_CS	34	35	L_CS
GND	36	37	L_A(11)
R_A(12)	38	39	L_A(12)
R_A(13)	40	41	L_A(13)
R_A(14)	42	43	L_A(14)
R_A(15)	44	45	L_A(15)
N.C.	46	47	N.C.
R_I/O(0)	48	49	L_I/O(0)
R_I/O(1)	50	51	L_I/O(1)
R_I/O(2)	52	53	GND
R_I/O(3)	54	55	L_I/O(2)
R_I/O(4)	56	57	L_I/O(3)
R_I/O(5)	58	59	L_I/O(4)
R_I/O(6)	60	61	L_I/O(5)
R_I/O(7)	62	63	L_I/O(6)
VCC	64	63	L_I/O(7)

SIMM
TOP VIEW

2839 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE

©1992 Integrated Device Technology, Inc.

DESCRIPTION:

The IDT7MP1021/1023 is a 128K/64K x 8 high-speed CMOS dual-port static RAM module constructed on a multi-layer FR-4 substrate using decode logic and either eight IDT7006 (16K x 8) dual-port RAMs for the 7MP1021 or four IDT7006s for the 7MP1023.

The IDT7MP1021/1023 provide two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via semaphore (SEM) "handshake" signaling. The IDT7MP1021/1023 modules are designed to be used as stand-alone dual-port RAMs where on-chip hardware port arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7MP1021/1023 modules are packaged on a 64-lead multilayer FR-4 SIMM (Single In-line Memory Module). Maximum access times as fast as 25ns over the commercial temperature range are available.

All inputs and outputs of the IDT7MP1021/1023 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

PIN NAMES

Left Port	Right Port	Description
L_A (0-15)	R_A (0-15)	Address Inputs
L_I/O (0-7)	R_I/O (0-7)	Data Inputs/Outputs
L_RW	R_RW	Read/Write Enables
L_CS	R_CS	Chip Select
L_OE	R_OE	Output Enable
L_SEM	R_SEM	Semaphore Control
Vcc		Power
GND		Ground

NOTE:

- 2839 tbl 01
1. For the IDT7MP1023 (64K x 8) version, Pins 45 & 46 must be connected to GND for proper operation of the module. These pins become L_A(16) and R_A(16) respectively for the IDT7MP1021 (128K x 8) version.

7

7-11-1

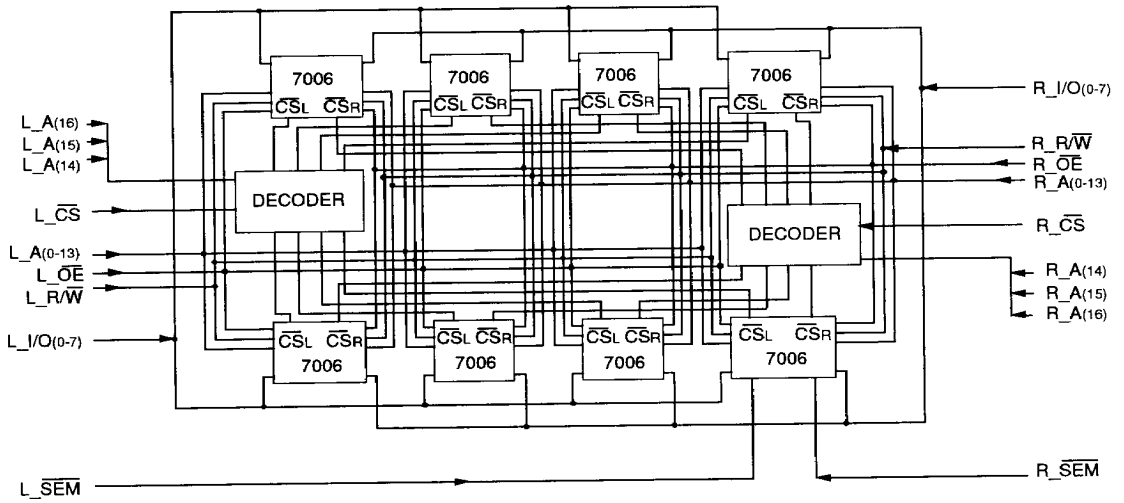
APRIL 1992

DSC-70853

1

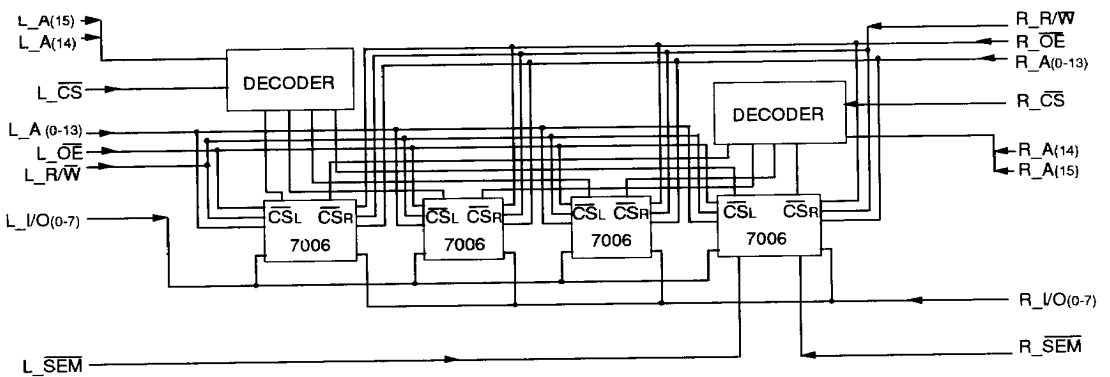
FUNCTIONAL BLOCK DIAGRAM

7MP1021



2839 drw 02

7MP1023



2839 drw 03

7-11-2

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

2839 tbl 02

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE⁽¹⁾ (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Test Conditions	Max.	Unit
CIN1	Input Capacitance (CS or SEM)	VIN = 0V	15	pF
CIN2	Input Capacitance (Data, Address, All Other Controls)	VIN = 0V	100	pF
COU	Output Capacitance (Data)	VOUT = 0V	100	pF

2839 tbl 03

NOTE:

1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2839 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	-	6.0	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	-	0.8	V

2839 tbl 05

NOTE:

1. VIL (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MP1021/1023			Unit
			Min.	Max. ⁽¹⁾	Max. ⁽²⁾	
ICC2	Dynamic Operating Current (Both Ports Active)	Vcc = Max., CS ≤ VIL, SEM ≥ VIH Outputs Open, f = fMAX	—	940	660	mA
ICC1	Standby Supply Current (One Port Active)	Vcc = Max., L_CS or R_CS ≥ VIH Outputs Open, f = fMAX	—	750	470	mA
ISB1	Standby Supply Current (TTL Levels)	Vcc = Max., L_CS and R_CS ≥ VIH Outputs Open, f = fMAX L_SEM and R_SEM ≥ Vcc - 0.2V	—	565	285	mA
ISB2	Full Standby Supply Current (CMOS Levels)	L_CS and R_CS ≥ Vcc - 0.2V VIN > Vcc 0.2V or < 0.2V L_SEM and R_SEM ≥ Vcc - 0.2V	—	125	65	mA

NOTES:

- For IDT7MP1021 (128K x 8) version only.
- For IDT7MP1023 (64K x 8) version only.

2839 tbl 06

7

7-11-3

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = 0°C to +70°C)

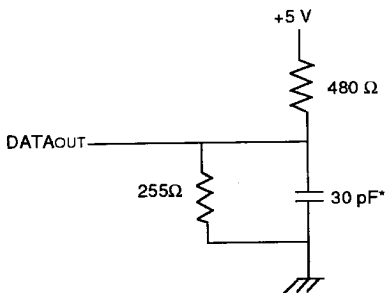
Symbol	Parameter	Test Conditions	IDT7MP1021		IDT7MP1023		Unit
			Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage (Address, Data & Other Controls)	V _{CC} = Max. V _{IN} = GND to V _{CC}	—	80	—	40	μA
I _{LI}	Input Leakage (CS and SEM)	V _{CC} = Max. V _{IN} = GND to V _{CC}	—	10	—	10	μA
I _{LO}	Output Leakage (Data)	V _{CC} = Max. CS ≥ V _{IH} , V _{OUT} = GND to V _{CC}	—	80	—	40	μA
V _{OL}	Output Low Voltage	V _{CC} = Min. I _{OL} = 4mA	—	0.4	—	0.4	V
V _{OH}	Output High Voltage	V _{CC} = Min. I _{OH} = -4mA	2.4	—	2.4	—	V

2839 tbl 07

AC TEST CONDITIONS

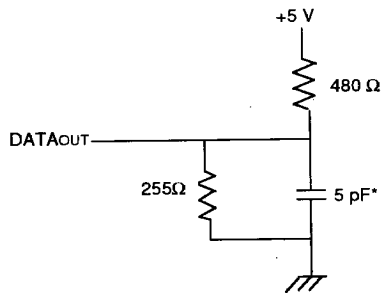
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2839 tbl 08



2839 drw 04

Figure 1. Output Load



2839 drw 05

Figure 2. Output Load
 (for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

*Including scope and jig.

7-11-4

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP1023SxxM, 7MP1021SxxM										Unit
		-25 ⁽⁶⁾		-30 ⁽⁶⁾		-35 ⁽⁶⁾		-40		-50		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t _{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	50	—	ns
t _{AA}	Address Access Time	—	25	—	30	—	35	—	40	—	50	ns
t _{ACS} ⁽²⁾	Chip Select Access Time	—	25	—	30	—	35	—	40	—	50	ns
t _{OE}	Output Enable Access Time	—	13	—	15	—	20	—	25	—	30	ns
t _{OH}	Output Hold From Address Change	3	—	3	—	3	—	3	—	3	—	ns
t _{CLZ} ⁽¹⁾	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	3	—	ns
t _{CHZ} ⁽¹⁾	Chip Deselect to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t _{OLZ} ⁽¹⁾	Output Enable to Output in Low Z	3	—	3	—	3	—	3	—	3	—	ns
t _{OHZ} ⁽¹⁾	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t _{PV} ⁽¹⁾	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t _{PD} ⁽¹⁾	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	—	50	ns
t _{ISOP}	SEM Flag Update Pulse (OE or SEM)	12	—	12	—	15	—	15	—	15	—	ns
Write Cycle												
t _{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	50	—	ns
t _{CW} ⁽²⁾	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t _{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t _{AS1} ⁽³⁾	Address Set-up to Write Pulse Time	5	—	5	—	5	—	5	—	5	—	ns
t _{AS2}	Address Set-up to CS Time	0	—	0	—	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	40	—	ns
t _{WR} ⁽⁴⁾	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t _{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	35	—	ns
t _{DH} ⁽⁴⁾	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t _{OHZ} ⁽¹⁾	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t _{WHZ} ⁽¹⁾	Write Enable to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t _{OW} ^(1, 4)	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns
t _{SWRD}	SEM Flag Write to Read Time	10	—	13	—	15	—	15	—	15	—	ns
t _{SPS}	SEM Flag Contention Window	10	—	13	—	15	—	15	—	15	—	ns
Port-to-Port Delay Timing												
t _{WDD} ⁽⁶⁾	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	—	70	ns
t _{DDP} ⁽⁶⁾	Write Data Valid to Read Data Valid	—	35	—	40	—	45	—	50	—	55	ns

NOTES:

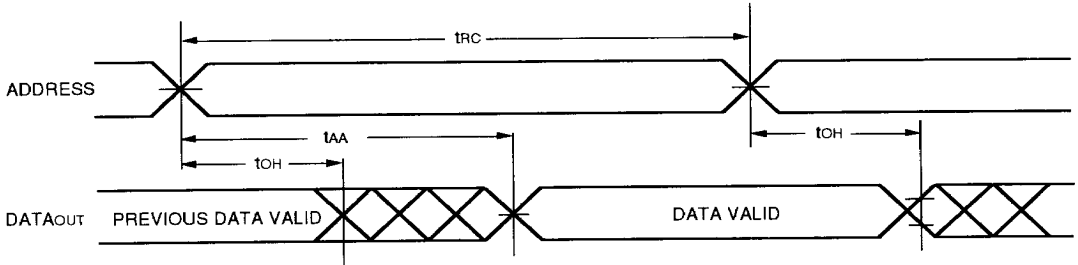
2839 tbi 09

1. This parameter is guaranteed by design but not tested.
2. To access RAM CS ≤ V_{IL} and SEM ≥ V_{IH}. To access semaphore, CS ≥ V_{IH} and SEM ≤ V_{IL}.
3. t_{AS1} = 0 if R/W is asserted low simultaneously with or after the CS low transition.
4. For CS controlled write cycles, t_{WR} = 5ns, t_{DH} = 5ns, t_{OW} = 5ns.
5. Preliminary specifications only.
6. Port-to-Port delay through the RAM cells from the writing port to the reading port.

7

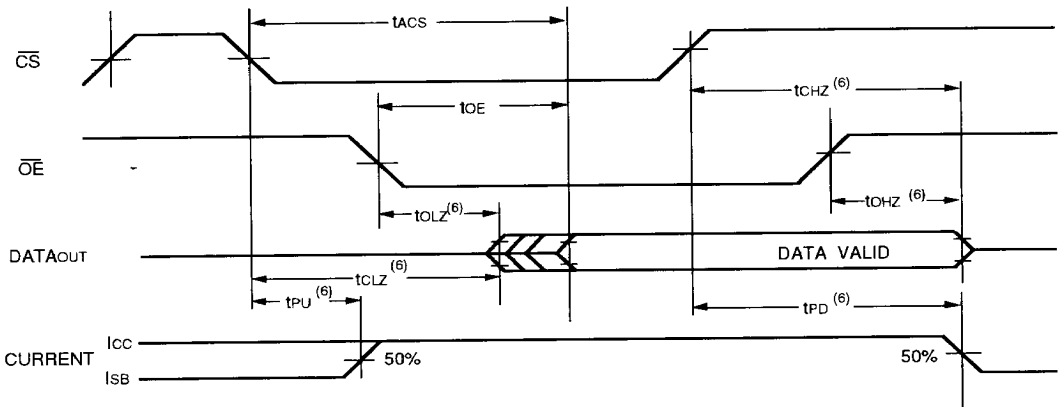
7-11-5

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE)^(1,2,4)



2839 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE)^(1,3,5)



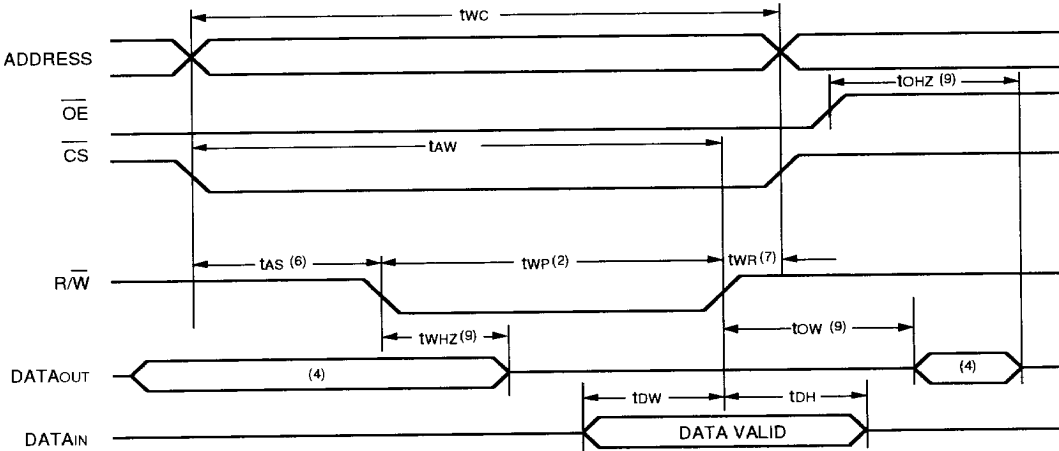
2839 drw 07

NOTES:

1. R/\overline{W} is High for Read Cycles
2. Device is continuously enabled. $\overline{CS} = \text{Low}$. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with \overline{CS} transition low.
4. $\overline{OE} = \text{Low}$.
5. To access RAM, $\overline{CS} = \text{Low}$, $\overline{SEM} = \text{H}$. To access semaphore, $\overline{CS} = \text{H}$ and $\overline{SEM} = \text{Low}$.
6. This parameter is guaranteed by design but not tested.

7-11-6

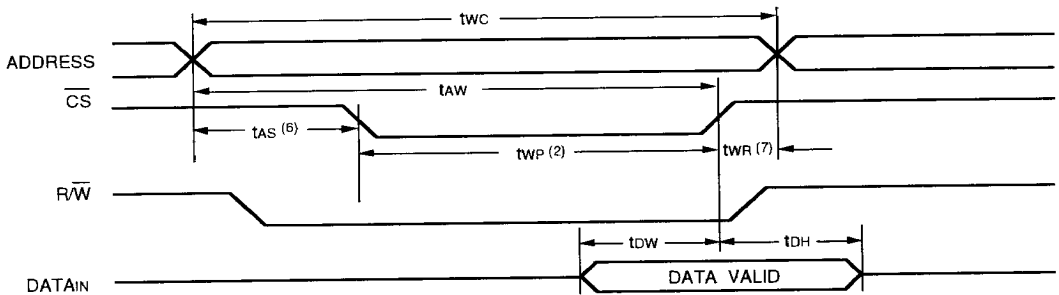
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/W CONTROLLED TIMING)^(1,3,5,8)



2839 drw 08

- NOTES:**
1. R/W is High for Read Cycles
 2. Device is continuously enabled. CS = Low. This waveform cannot be used for semaphore reads.
 3. Addresses valid prior to or coincident with CS transition low.
 4. OE = Low.
 5. To access RAM, CS = Low, SEM = H. To access semaphore, CS = H and SEM = Low.
 6. Timing depends on which enable signal is asserted last.
 7. Timing depends on which enable signal is de-asserted first.
 8. If OE is Low during a R/W controlled write cycle, the write pulse width must be larger of tWP or (twz + tow) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If OE is High during a R/W controlled write cycle, this requirement does not apply and the write pulse width be as short as the specified tWP.
 9. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS CONTROLLED TIMING)^(1,3,5,8)



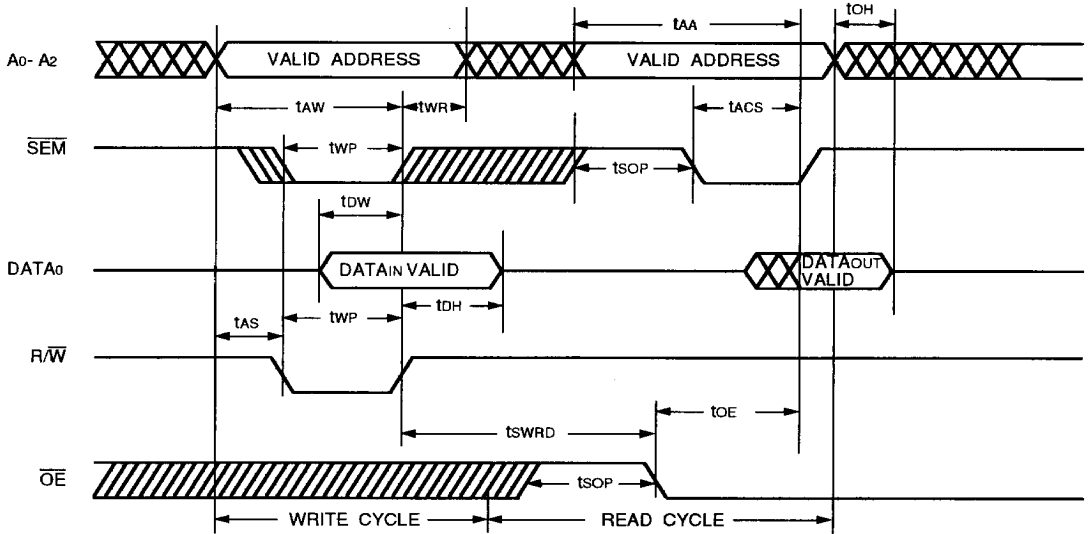
2839 drw 09

- NOTES:**
1. R/W must be high during all address transitions.
 2. A write occurs during the overlap (tWP) of a Low CS and a Low R/W for memory array writing cycle.
 3. tWR is measured from the earlier of CS or R/W (or SEM or R/W) going high to the end of write cycle.
 4. During this period, the I/O pins are in the output state and input signals must not be applied.
 5. If the CS or SEM low transition occurs simultaneously with or after the R/W low transition, the outputs remain in the high impedance state.
 6. Timing depends on which enable signal is asserted last.
 7. Timing depends on which enable signal is de-asserted first.
 8. If OE is low during a R/W controlled write cycle, the write pulse width must be the larger of tWP or (twz + tow) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If OE is high during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
 9. This parameter is guaranteed by design but not tested.

7

1-11-7

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING (EITHER SIDE)⁽¹⁾

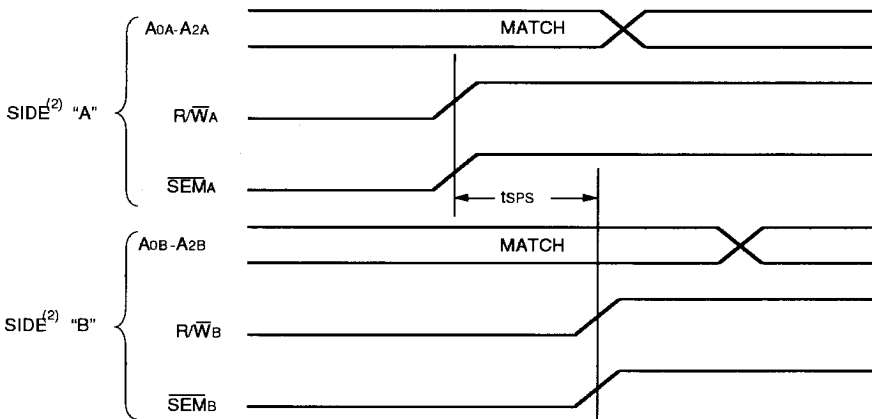


NOTE:

1. \overline{CS} = High for the duration of the above timing (both write and read cycle).

2839 drw 10

TIMING WAVEFORM OF SEMAPHORE CONTENTION^(1,3,4)



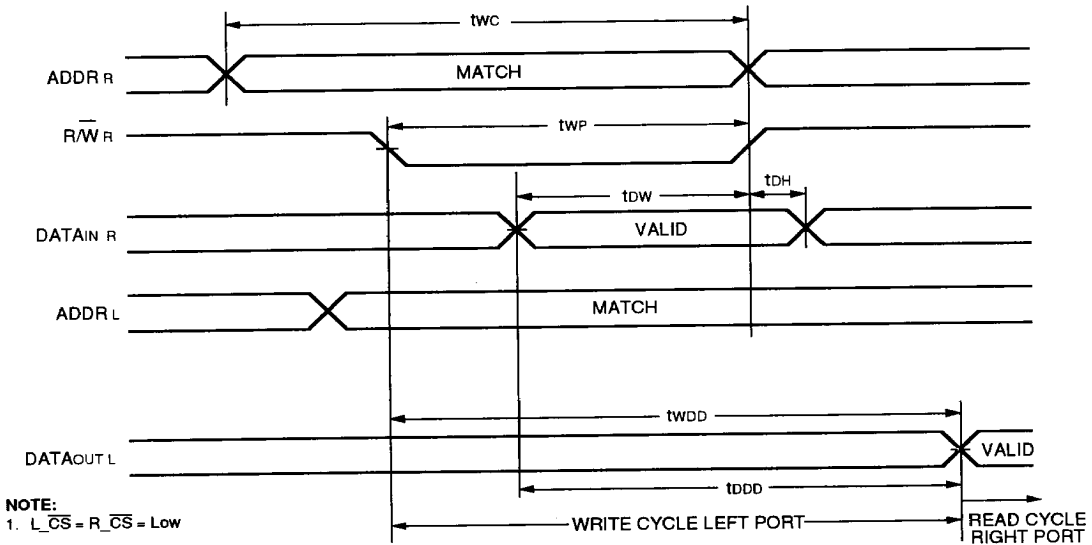
2839 drw 11

NOTES:

1. $D0R = D0L = Low$, $L\overline{CS} = R\overline{CS} = High$. Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/\overline{W}_A or $SEMA$ going High to R/\overline{W}_B or $SEMB$ going High.
4. If $tSPS$ is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

7-11-8

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY⁽¹⁾



2839 drw 12

TRUTH TABLES

TABLE I: NON-CONTENTION READ/WRITE CONTROL⁽¹⁾

Inputs ⁽¹⁾				Outputs	Mode
\overline{CS}	R/W	\overline{OE}	SEM	I/O ₀ - I/O ₇	
H	X	X	H	Hi-Z	Deselected: Power Down
L	L	X	H	DATA _{IN}	Write to Memory
L	H	L	H	DATA _{OUT}	Read from Memory
X	X	H	X	Hi-Z	Outputs Disabled

NOTE:
1. A_{0L} — A₁₂ ≠ A_{0R} — A_{12R}

2839 tbl 10

TABLE II: SEMAPHORE READ/WRITE CONTROL⁽¹⁾

Inputs				Outputs	Mode
\overline{CS}	R/W	\overline{OE}	SEM	I/O ₀ - I/O ₇	
H	H	L	L	DATA _{OUT}	Read Data in Semaphore Flag
X		X	L	DATA _{IN}	Write D ₁₀ into Semaphore Flag
L	X	X	L	—	Not Allowed

NOTE:
1. A_{0L} — A₁₂ ≠ A_{0R} — A_{12R}

2839 tbl 11

SEMAPHORE OPERATION

For more details regarding semaphores & semaphore operations, please consult the IDT7006 datasheet.

PACKAGE DIMENSIONS — PLEASE CONSULT FACTORY

7-11-9

7