HT9260/HT9261

Serial Interface Combined PCM Codec & Filter

Features

- Transmit high pass and low pass filter
- Receive low pass filter with sine x/x correction
- Active RC noise filter
- HT9260 is a μ-law CODEC, HT9261 is a A-law CODEC
- Internal precision voltage reference
- Serial I/O interface
- Internal auto-zero circuitry +5V and –5V operation
- Auto power down
- Low operating power — 60 mW typ.
- Low power down standby mode — 3 mW

General Description

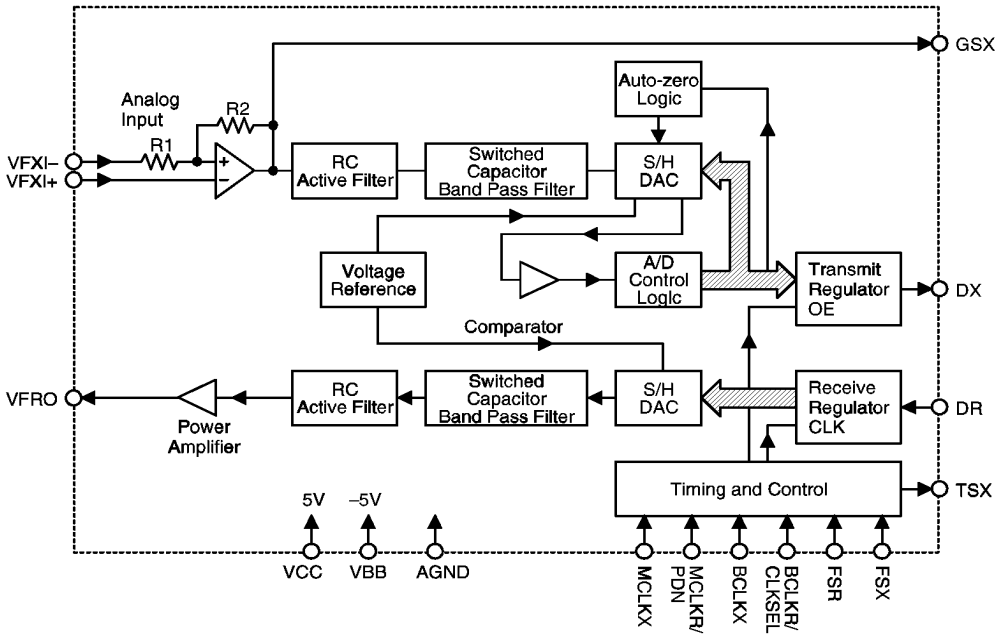
HT9260/HT9261 are μ-law and A-law monolithic PCM CODEC. The chip consists of two portions; one is the encoding portion and another is the decoding portion.

The encoding portion consists of an input gain amplifier, an active RC pre-filter which eliminates the high frequency noise, auto-zero circuitry and the companding coder which samples the filtered signal and encodes it in the companding μ-law or A-law format.

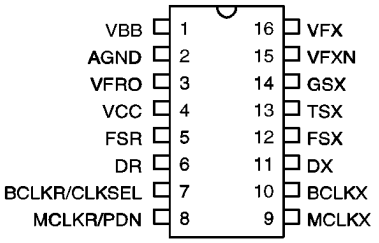
The decoding portion consists of an expanding decoder, which reconstructs the analog signal from the companding μ-law or A-law code, a low pass filter which corrects the sine x/x response of the decoder output and rejects the signals above 3400Hz followed by a single-ended power amplifier driving low impedance loads.

The chip requires a master clock with a frequency of 1.536/1.544MHz or 2.048MHz. For asynchronous operation separate transmit and receive clocks can be used. The bit clock can range from 64kHz to 2.048MHz.

Block Diagram



Pin Assignment



HT9260/HT9261
– 16 DIP/SOP

Pin Description

Pin Name	Description
AGND	Analog ground
VFRO	Receive power amplifier analog output
VBB	Negative power supply, V_{BB}= –5V±5%

Pin Name	Description
VCC	Positive power supply, V_{CC}= 5V±5%
FSR	Receive frame sync pulse which enables BCLKR to shift PCM data in DR
DR	Receive data input. PCM data is shifted into DR following the FSR leading edge.
BCLKR/CLKSEL	The bit clock which shifts the data into DR after the FSR leading edge. It ranges from 64kHz to 2.048MHz. Alternatively, it can be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for the master clock in synchronous mode and BCLKX is used for both transmit and receive.
MCLKR/PDN	Receive master clock. Must be 1.536MHz/1.544MHz or 2.048MHz. Asynchronous with MCLKX. When MCLKR is held low, MCLKX is selected for all internal timing. When MCLKR is pulled high, the chip is powered down.
MCLKX	Transmit master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. Asynchronous with MCLKR.
FSX	Transmit frame sync pulse input which enables BCLKX to shift out the PCM data on DX.
BCLKX	Shifts out the PCM data on DX. May vary from 64kHz to 2.048MHz.
DX	PCM data output which is enabled by FSX
TSX	Open drain output with low pulse during the encoder time slot.
GSX	Analog output of transmit input amplifier which is used to externally set gain.
VFXN	Inverting input of transmit input amplifier.
VFX	Non-inverting input of the transmit input amplifier.

Absolute Maximum Ratings*

Supply voltage, V_{CC} 7V

Supply voltage, V_{BB} ..... –7V

Voltage range at any analog input or output ..... V_{CC}+0.3V to V_{BB}–0.3V

Voltage range at any digital input or output ..... V_{CC}+0.3V to V_{AGND}–0.3V

Operating free-air temperature range ..... 0°C to 70°C

Storage temperature range ..... –65°C to 150°C

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

All signals are referenced to V_{AGND}, Typically specified at V_{CC}=5.0V, V_{BB}=–5.0V, Ta=25°C

• Digital interface

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level Input Voltage	—	—	—	0.6	V
V_{IH}	High-level Input Voltage	—	2.2	—	—	V
V_{OL}	Low-level Output Voltage	DX, I_L=3.2mA TSX, I_L=3.2mA, Open	—	—	0.4	V
V_{OH}	High-level Output Voltage	DX, I_H=–3.2mA	2.4	—	—	V
I_{IL}	Low-level Input Current	$V_{AGND}<V_{IN}<V_{IL}$	–10	—	–10	μA
I_{IH}	High-level Input Current	$V_{IH}<V_{IN}<V_{CC}$	–10	—	10	μA
I_{OZ}	Output Current in High-impedance	DX, $V_{AGND}<V_O<V_{CC}$	–10	—	10	μA

• Analog interface with the transmit input amplifier

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{XA}	Input Leakage	–2.5V<V<2.5V	–200	—	200	nA
R_{IXA}	Input Resistance	–2.5V<V<2.5V	10	—	—	MΩ
R_{OXA}	Output Resistance	Close loop, unit gain	—	1	3	Ω
R_{LXA}	Load Resistance	GSX	10	—	—	kΩ
C_{LXA}	Load Capacitance	GSX	—	—	50	pF
V_{OXA}	Output Range	GSX, R_L>10kΩ	–2.8	—	2.8	V
A_{VXA}	Voltage Gain	VFX to GSX	5000	—	—	

• Analog interface with the receive filter

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{ORF}	Output Resistance	VFRO	—	1	3	Ω
R_{LRF}	Load Resistance	VFRO=±2.5V	600	—	—	Ω
C_{LRF}	Load Capacitance	—	—	—	500	pF
V_{OSRO}	Output DC Offset Volt	—	–200	—	200	mV

• Power consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC0}	Power Down	No load	—	0.5	1.5	mA
I_{BB0}	Power Down	No load	—	0.05	0.3	mA
I_{CC1}	Power Up Active	No load	—	11.4	—	mA
I_{BB1}	Power Up Active	No load	—	10.8	—	mA

Functional Description

- Power-up

  When power is first applied, the power-on reset circuitry initializes the whole chip and places it into power down state. The non-essential circuits are deactivated and the DX and VFRO output are put in high impedance. To power up the this chip, a logical low or clock must be applied to the MCLKR /PDN pin; FSX and/or FSR pulse must be present. There are two power-down modes are available; the first is to pull MCLKR/PDN pin to high; the alternative is to hold both FSX and FSR inputs continuously low. The power-up will occur on the first FSX or FSR pulse. TRI-STATE PCM data output, DX, will remain in the high impedance state until the second FSX pulse.

- Synchronous operation

  For synchronous operation, the same master clock and bit clock should be used for the transmit and receive direction. In this mode, the clock must be applied to MCLKX and MCLKR/PDN pin can be used as power down control. The MCLKX will be selected as the master clock for both the transmit and receive circuit. A bit clock must be applied to BCLKX and BCLKR/CLKSEL can be used to select proper internal divider for a master clock of 1.536 MHz, 1.544MHz or 2.048MHz. With the fixed level on the BCLKR/CLKSEL pin, the BCLKX will be selected as the bit clock for both transmit and receive direction. Table 1 indicates the frequencies of operation which can be selected, depending on the state of BCLKR/CLKSEL. In the synchronous mode, the bit clock, BCLKX, may be from 64kHz to 2.048 MHz, but must be synchronous with the MCLKX. Each FSX pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled DX output on the positive edge of BCLKX. After 8 bit clock periods, the DX is returned to a high impedance state. With the FSR pulse, PCM data is latched via the DX input on the negative edge of the BCLKX. FSX and FSR must be synchronous with MCLKX/R.

BCLKR/ CLKSEL	Master Clock Freq Selected
Clocked	1.536MHz or 1.544MHz
0	2.048MHz
1 or open circuit	1.536MHz or 1.544MHz

Table 1. Selection of Master Clock Frequency

- Asynchronous operation

  For the asynchronous operation, separate transmit and receive clocks may be applied. MCLKX and MCLKR need not be synchronous. FSX starts each encoding cycle and must be synchronous with BCLKX and MCLKX. FSR starts the decoding cycle and must be synchronous with the BCLKR. In asynchronous mode, BCLKR must be a clock, i.e. can not be a logic level; the valid frequency ranges from 64kHz to 2.048MHz.

- Short frame synchronous operation

  In this mode, both FSR and FSX must be one bit clock period long. With FSX high during a falling edge of BCLKX , the next rising edge of BCLKX enables the DX output buffer, which will output the sign bit. The following seven rising edges clock output the remaining seven bits. and the next falling edge disables the DX output. With FSR high during a falling edge of BCLKR latches in the sign bit. The following seven falling edges latch in the seven remaining bits.

- Long frame synchronous operation

  In this mode, both frame sync pulses, FSR and FSX, must be three or more bit clock periods long. Based on the transmit frame sync, FSX, the chip will sense whether short or long frame sync pulses are being used. The DX tristate output buffer is enabled with the rising edge of FSX or the rising edge of BCLKX., and the first bit clocked out is the sign bit. The following seven BCLKX rising edge clock out the remaining seven bits. DX output is disabled by the falling BCLKX edge following the eighth rising edge or by the FSX going low. A rising edge on the receive frame sync, FSR, will cause the PCM data at DR to be latched on the next eight falling edges of BCLKR.

- Transmit section

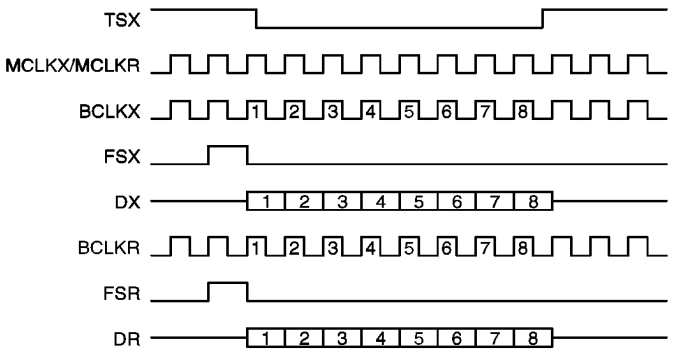
  The input in the transmit section is an operational amplifier with provision for gain adjustment using two external resistors. The low noise and wide bandwidth allow gains in excess of 20dB across the audio passband to be realized. The op amplifier drives a unity-gain filter consisting of RC active pre-filter followed by an eighth order switched capacitor filter clocked at 256kHz. The output of this filter directly drives a sample-hold circuit. The FSX frame sync pulse controls the sampling of the filter output, then the successive-approximation encoding cycle begins. The 8-bit code is loaded into a buffer and shifted out through DX at the next FSX pulse. The total encoding delay will be approximately 165μs (transmit filter delay) plus 125μs (encoding delay), which total 290μs. Any offset voltage due to the filter or comparator is canceled by sign bit integration.

- Receive section

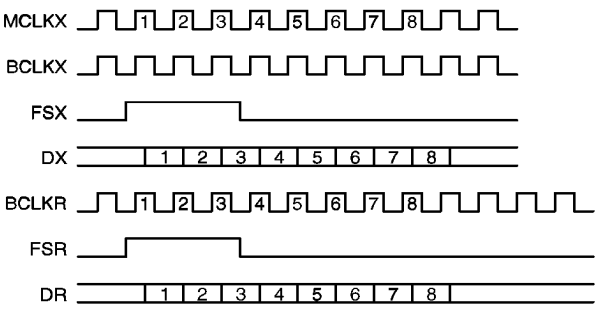
  The receive section consists of an expanding DAC which drives a fifth order switched capacitor filter clocked at 256kHz. The decoder which is the 5th order low pass filter corrects for the sine x/x attenuation due to the 8kHz sample-hold. The filter is followed by the 2nd order RC active post-filter capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unit-gain. Upon the occurrence of FSR, the data at the DR input is clocked in on the falling edge of the next eight BCLKR or BCLKX period. At the decoder time slot, the decoding cycle begins and 10μs later, the decode DAC output is updated. The total decoder delay is about 10 us (decoder update) plus 110μs (filter delay) plus 62.5μs (half frame), which gives approximately 180μs.

Timing Diagrams

• Short frame sync timing



• Long frame sync timing



Application Circuits

While the pins of the HT9260/HT9261 are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications, as shown in the following figure, where the printed circuit board may be plugged into a hot socket with power and clocks already preset, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the AGND pin. This minimizes the interaction of ground return currents flowing through common bus impedance. V_{CC} and V_{BB} supplies should be decoupled by connecting 0.1μF decoupling capacitors to this common point. These bypass capacitors must be connected as close as possible to V_{CC} and V_{BB}.

For best performance, the ground point of each codec/filter on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10μF capacitors.