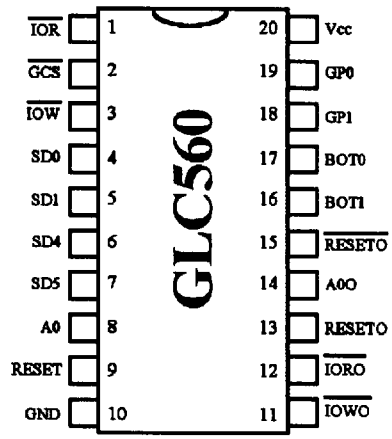
Description

GLC560 is an integrated chip of two timers, two OR-gates, control signal buffers and game data buffers. It can support one game controller without any additional TTL devices. Thus, it offers simple solution to the Super I/O card. Game port logic completes the compatibility with the IBM PC/AT.

Pin Configuration



Features

- 2 timers (GLC556) built-in for game port.
- Support 1 Game controller for joystick.
- IOR, IOW, RESET, A0 buffer built-in.
- Support RESET pin for IDE port.
- + 5V power supply.
- 20 pin DIP and SOP package.

Application

- IBM PC/AT Super I/O Add-on-cards on all-in-one PC system.
- Sound Card for supporting the Joy Stick.

Absolute Maximun Ratings (Voltage Referenced to GND)

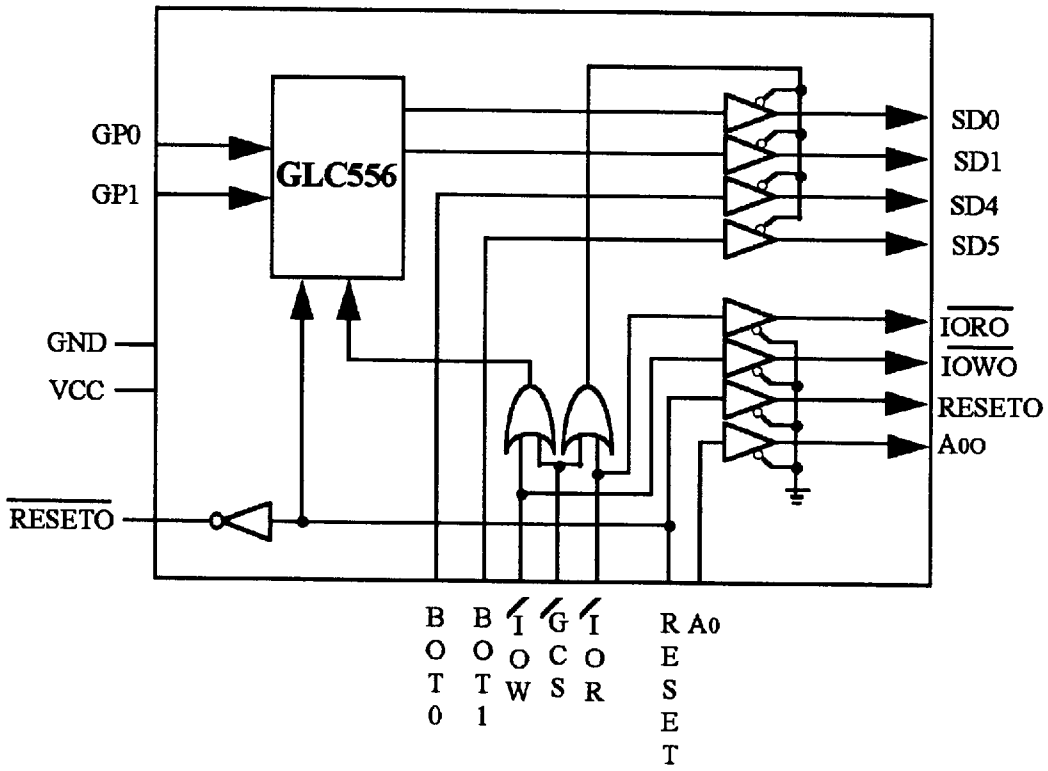
RATING	VALUE	UNIT
DC Supply Voltage	-0.3 to 7.0	V
Input Voltage	-0.3 to V_{DD} + 0.3	V
DC Input Current	-10 to 10	mA
Storage Temperature Range	-40 to 125	℃

Note : Stresses above those listed under Absolute Maximum Rations may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

Recommended Operating Conditions (Voltage Referenced to GND)

RATING	VALUE	UNIT
DC Supply Voltage	4.75 to 5.25	V
Operating Ambient Temperature Range	0 to 70	℃

Block Diagram



Description of Pin function

PIN NO.	NAME	SYMBOL	INPUT OUTPUT	FUNCTION
1	I/O Read	$\overline{IOR}$	I	This active low signal is issued by the Host sysstem to indicate a read operation
2	Game Port Chip Select	$\overline{GCS}$	I	This active low signal is the Game Port Chip Select. It will go active when the I/O address is 201H
3	I/O Write	$\overline{IOW}$	I	This active low signal is issued by the Host system to indicate a Write operation
4	Data Bus Bit 0	SD0	O	Game Port data bus bit 0
5	Data Bus Bit 1	SD1	O	Game Port data bus bit 1
6	Data Bus Bit 4	SD4	O	Game Port data bus bit 4
7	Data Bus Bit 5	SD5	O	Game Port data bus bit 5
8	Address 0	A0	I	Address bit 0
9	Reset	RESET	I	This active high signal is issued by the Host sysstem to reset the GLC560

(Continued)

PIN NO.	NAME	SYMBOL	INPUT OUTPUT	FUNCTION
10	Ground	GND	G	0V Reference
11	I/O Write Output	$\overline{\text{IOWO}}$	O	This active low signal is buffered for the Super I/O controller (Prime 3A/3B) to indicate a Write operation
12	I/O Read Output	$\overline{\text{IORO}}$	O	This active low signal is buffered for the Super I/O controller (Prime 3A/3B) to indicate a Read operation
13	Reset output	RESETO	O	This active high signal is buffered for the Super I/O controller (Prime 3A/3B) to reset operation
14	Address 0 output	A0O	O	Address bit 0
15	$\overline{\text{Reset}}$ output	$\overline{\text{RETSETO}}$	O	This active low signal is buffered for the IDE Port to reset operation
16	Button 1	BOT1	I	Game data bit 5. Game Port input signal.
17	Button 0	BOT0	I	Game data bit 4. Game Port input signal.
18	Game Y-postion	GP1	I	Y threshold. Game port Y-direction displacement signal
19	Game X-postion	GP0	I	X threshold. Game port X-direction displacement signal
20	Power	VCC	P	+5V Power pin

Electrical Characteristics

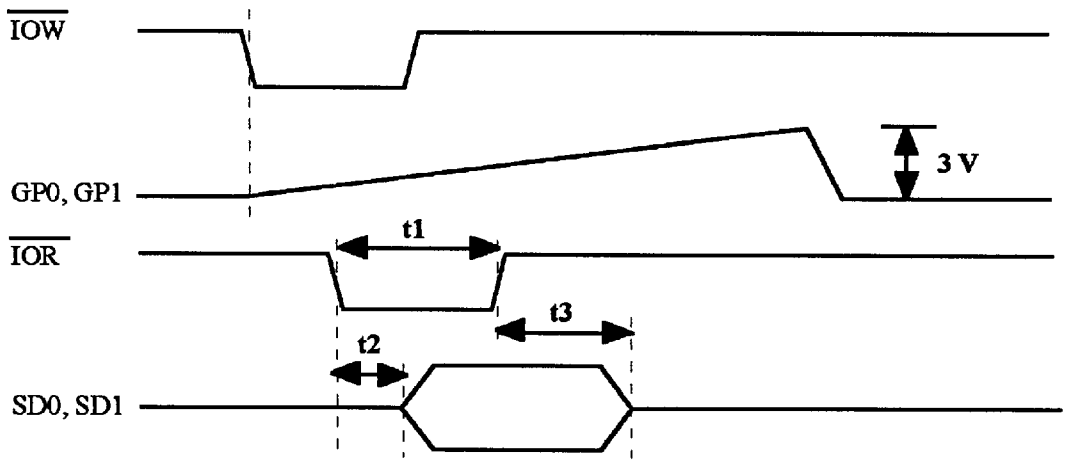
DC Characteristics (V_{DD} = 5V ± 5% over Operating Temp. Range 0℃ ~ 70℃)

CHARACTERISTIC	CONDITIONS	SYMBOL	V_{DD}	Min.	Typ.	Max.	UNIT
High Level Input Voltage	GP0,1 = 3.5 V	V_{IH}	—	2.0	---	---	V
Low Level Input Voltage	GP0,1 = 2.5 V	V_{IL}	—	---	---	0.8	V
High Level Input Current	V_{IN} = V_{DD}	I_{IH}	5.25	- 10	---	10	μA
Low Level Input Current	V_{IN} = V_{SS} ~ 0.8	I_{IL}	5.25	- 10	---	10	μA
High Level Output Voltage	I_{OH} = - 0.2 mA	V_{OH}	4.75	2.4	---	---	V
Low Level Output Voltage	I_{OL} = 8 mA	V_{OL}	4.75	---	---	0.4	V
Quiescent Supply Current	GP0,1 = VSS V_{IN} = V_{DD} or V_{SS}	I_{CC}	5.25	---	---	6	mA
GP0,1 Pin Threshold Voltage	---	V_{TH}	5 ± 5%	3/5V_{DD}	---	---	V

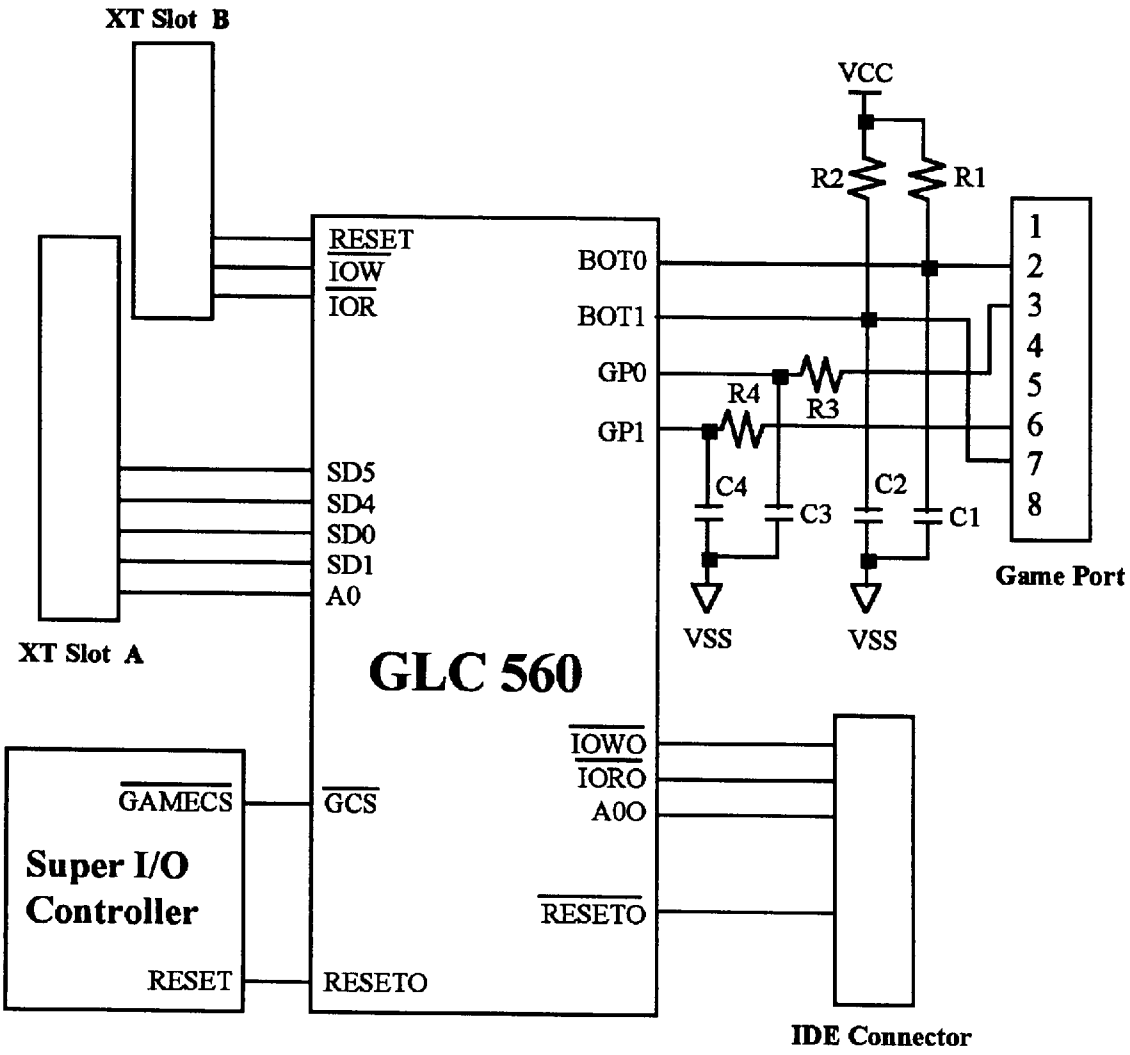
AC Characteristics : All Timings are Referenced to Valid 0 and Valid 1.

(VDD = 5V ± 5% Over Operatig TEMP. Range 0℃ ~ 70℃)

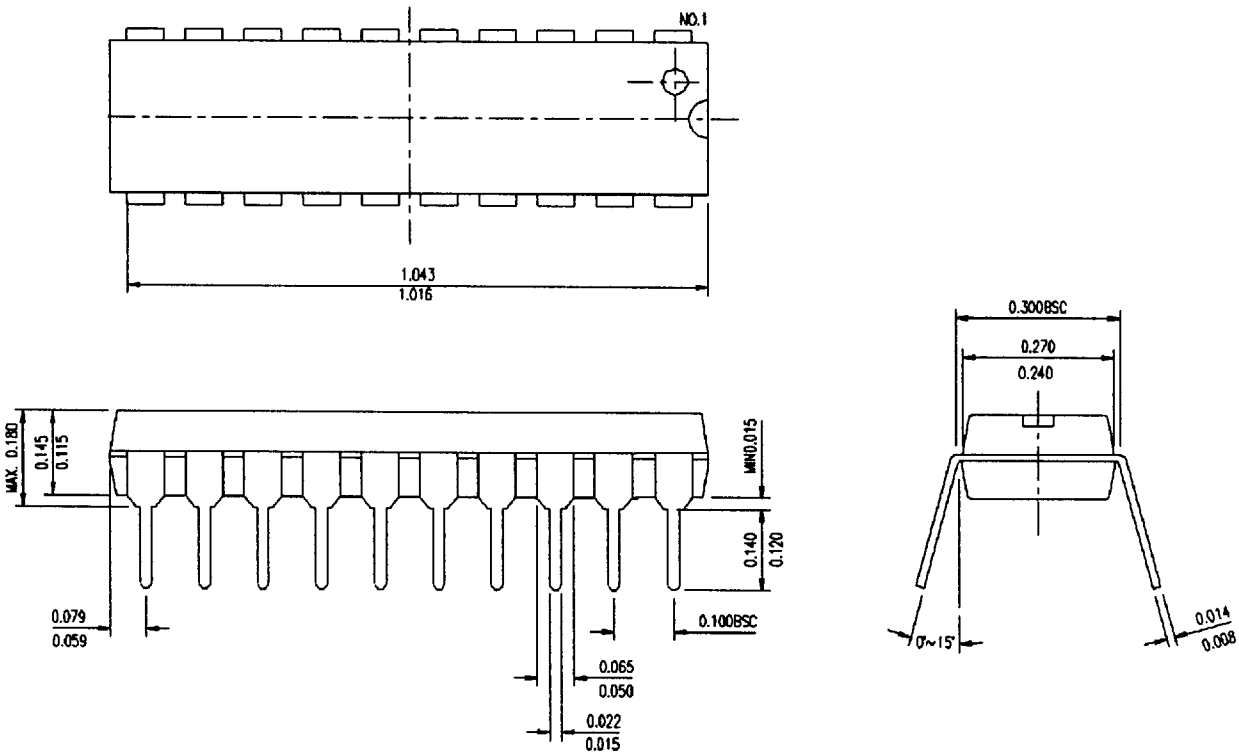
SYMBOL	DESCRIPTION	Min.	Max.	UNIT
t1	$\overline{IOR}$ and $\overline{IOW}$ Pulse Width	150	---	ns
t2	Data Propagation Delay from $\overline{IOR}$	---	100	ns
t3	Data Hold Time from $\overline{IOR}$	10	60	ns



Application Circuit



R1, R2 : 4.7K
R3, R4 : 2.2K
C1, C2 : 47p
C3, C4 : 103


NO.1
1.043
1.016
MAX. 0.180
0.145
0.115
MIN0.015
0.140
0.120
0.079
0.059
0.100BSC
0.065
0.050
0.022
0.015
0.300BSC
0.270
0.240
0~15°
0.014
0.008