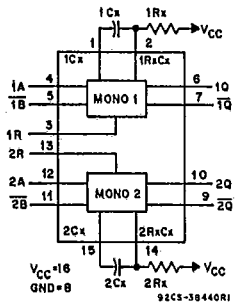
T-51-19-00

CD54/74HC4538
CD54/74HCT4538

File Number **1671**

HARRIS SEMICOND SECTOR 27E D 4302271 0017993 5 HAS

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual Retriggerable Precision Monostable Multivibrator

Type Features:

- *Retriggerable/resettable capability*
- *Trigger and Reset propagation delays independent of R_x, C_x*
- *Triggering from the leading or trailing edge*
- *Q and $\overline{Q}$ Buffered Outputs available*
- *Separate Resets*
- *Wide Range of Output-Pulse Widths*
- *Schmitt Trigger input on A and $\overline{B}$ inputs*
- *Retrigger Time is independent of C_x.*

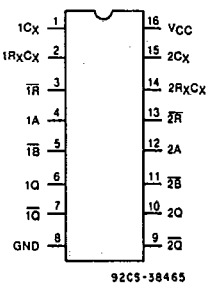
The RCA-CD54/74HC4538 and CD54/74HCT4538 are dual retriggerable/resettable monostable precision multivibrators for fixed voltage timing applications. An external resistor (R_x) and an external capacitor (C_x) control the timing and the accuracy for the circuit. Adjustment of R_x and C_x provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The propagation delay from trigger input-to-output transition and the propagation delay from reset input-to-output transition are independent of R_x and C_x.

Leading-edge triggering (A) and trailing edge triggering ($\overline{B}$) inputs are provided for triggering from either edge of the input pulse. An unused "A" input should be tied to Gnd and an unused $\overline{B}$ should be tied to V_{CC}. On power up the IC is reset. Unused resets and sections must be terminated. In normal operation the circuit retriggers on the application of each new trigger pulse. To operate in the non-retriggerable mode $\overline{Q}$ is connected to $\overline{B}$ when leading edge triggering (A) is used or Q is connected to A when trailing edge triggering ($\overline{B}$) is used. The period (τ) can be calculated from $\tau = (0.7)\ R_x\ C_x$; R_{min} is 5k ohms. C_{min} is 0 pF.

The CD54HC/HCT4538 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT4538 are supplied in 16-lead dual-in-line plastic packages (E suffix), also in 16-lead dual-in-line surface mount plastic packages (M suffix). The CD54/74HC/HCT4538 are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC4538
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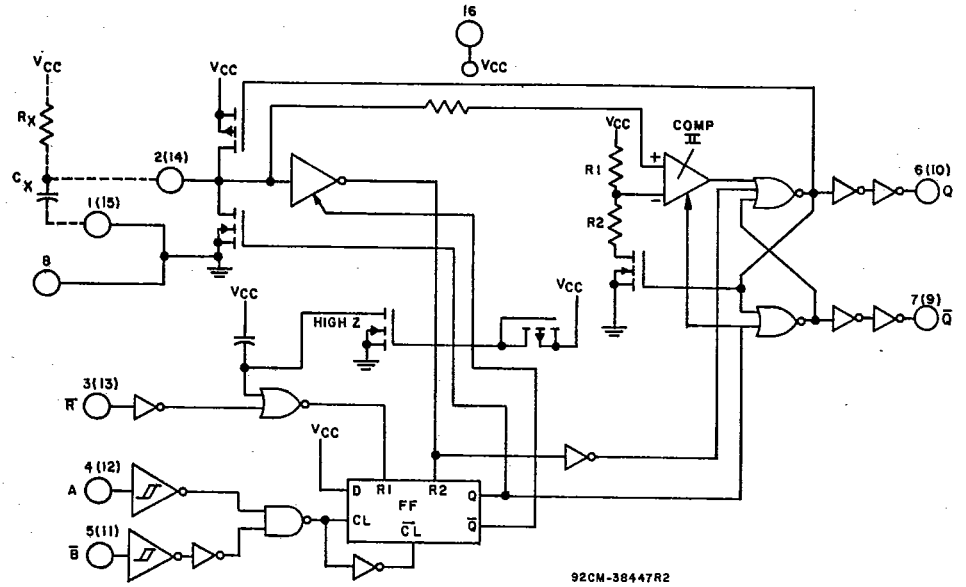
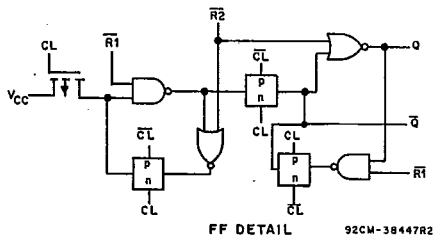


Fig. 1 - Logic diagram (1 mono).



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{R}$	A	$\overline{B}$	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↘	⊓	⊔
H	↗	H	⊓	⊔

H = High Level
L = Low Level
↗ = Transition from Low to High
↘ = Transition from High to Low
⊓ = One High Level Pulse
⊔ = One Low Level Pulse
X = Irrelevant

HC/HCT4538 FUNCTIONAL TERMINAL CONNECTIONS

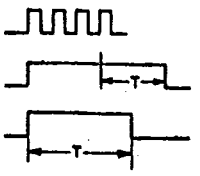
FUNCTION	V_{CC} TO TERM. NO.		Gnd TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/ Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/ Non-Retriggerable	3	13			5	11	4-6	12-10

NOTES:
1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD (T) REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.

INPUT PULSE TRAIN

RETRIGGERABLE MODE PULSE WIDTH (A MODE)

NON-RETRIGGERABLE MODE PULSE WIDTH (A MODE)



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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
*DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$V) ..... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125° C
PACKAGE TYPE E, M ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C
*DC INPUT CURRENT FOR C_X R_X PIN = 30 mA

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
Reset Input			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns
Trigger Inputs A or $\overline{B}$			
at 2 V	0	Unlimited	ns
at 4.5 V	0	Unlimited	ns
at 6 V	0	Unlimited	ns
External Timing Resistor, R_x	5kΩ	#	
External Timing Capacitor, C_X	0	#	

*Unless otherwise specified, all voltages are referenced to Ground.

#The maximum allowable values of R_x and C_X are a function of leakage of capacitor C_X, the leakage of the HC4538, and leakage due to board layout and surface resistance. Values of R_x and C_x should be chosen so that the maximum current into pin 2 or pin 14 is 30 mA. Susceptibility to externally induced noise signals may occur for $R_x > 1$ MΩ.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4538/CD54HC4538										CD74HCT4538/CD54HCT4538								UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE	
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C	
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads Standard Output	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current A, $\overline{B}$, R I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
• Input Leakage Current $R_X C_X$ I_I			6	—	—	±0.05	—	±0.5	—	±0.5		5.5		—	±0.05	—	±0.5	—	±0.5	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Active Device Current Q = High & Pins 2 & 14 @ $V_{CC}/4$ I_{CC}	V_{CC} or Gnd	0	6	—	—	0.6	—	0.8	—	1	V_{CC} or Gnd	5.5	—	—	0.6	—	0.8	—	1	mA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
• When testing I_{IL} the Q output must be high. If Q is low (device not triggered) the pull-up P device will be ON and the low resistance path from V_{DD} to the test pin will cause a current far exceeding the specification.

HCT Input Loading Table

Input	Unit Loads*
All	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL 54/74HC	TYPICAL 54/74HCT	UNITS
Propagation Delay					
A, $\overline{B}$ to Q	t_{PLH}	15	21	23	ns
A, $\overline{B}$ to $\overline{Q}$	t_{PHL}	15	21	23	ns
$\overline{R}$ to Q	t_{PHL}	15	21	17	ns
$\overline{R}$ to $\overline{Q}$	t_{PLH}	15	21	21	ns
Power Dissipation Capacitance	C_{PD}*	—	136	134	pF

*C_{PD} is used to determine the dynamic power consumption, per one shot.
$P_D = (C_{PD} + C_L) V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where:
f_i = input frequency.
f_o = output frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.
assuming $f_i \ll \frac{1}{\tau}$

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	LIMITS 25° C HC Min.	HC Max.	HCT Min.	HCT Max.	-40° C to +85° C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55° C to +125° C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Input Pulse Widths A, $\overline{B}$	t_{WH}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	t_{WL}	6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{R}$	t_{WL}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Recovery Time	t_{REC}	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Retrigger Time (See Fig. 5)	t_{rr}	5	Typical 175												ns

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SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, A, $\overline{B}$ to Q	t_{PLH}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	55	—	63	—	69	—	75	—	83	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
A, $\overline{B}$ to $\overline{Q}$	t_{PHL}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	55	—	63	—	69	—	75	—	83	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
$\overline{R}$ to Q	t_{PHL}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	40	—	63	—	50	—	75	—	60	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
$\overline{R}$ to $\overline{Q}$	t_{PLH}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	50	—	63	—	63	—	75	—	75	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Output Pulse Width R_X=10Ω, C_X=0.1 μF	τ	3	0.64	0.78	—	—	0.612	0.812	—	—	0.605	0.819	—	—	ms
		5	0.63	0.77	0.63	0.77	0.602	0.798	0.602	0.798	0.595	0.805	0.595	0.805	
Output Pulse Width Match, Same Pkg.			Typ ± 1%												
Input Capacitance	C_i		—	10	—	10	—	10	—	10	—	10	—	10	pF

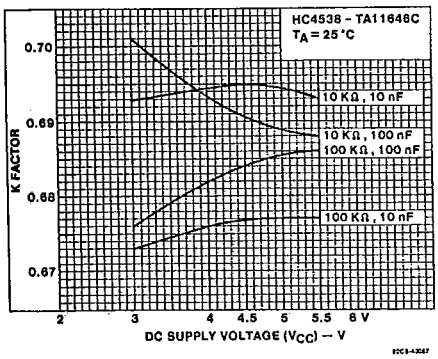

Fig. 2 - K Factor Vs DC Supply Voltage (V_{CC})-V.

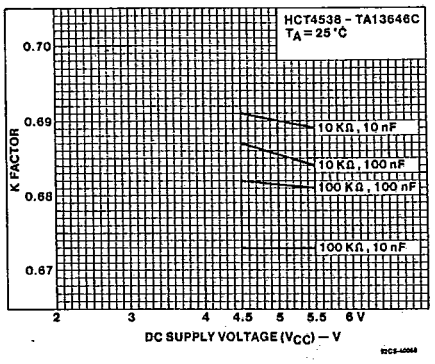

Fig. 3 - K Factor Vs DC Supply Voltage (V_{CC})-V.

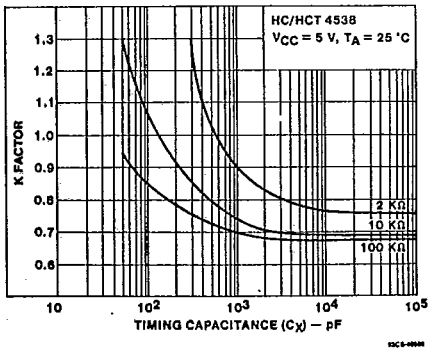

Fig. 4 - K Factor Vs C_X.

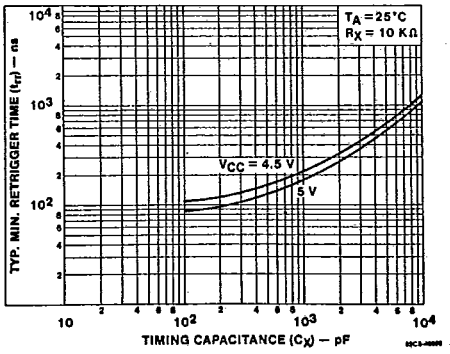

Fig. 5 - Minimum Retrigger Time Vs Timing Capacitance.

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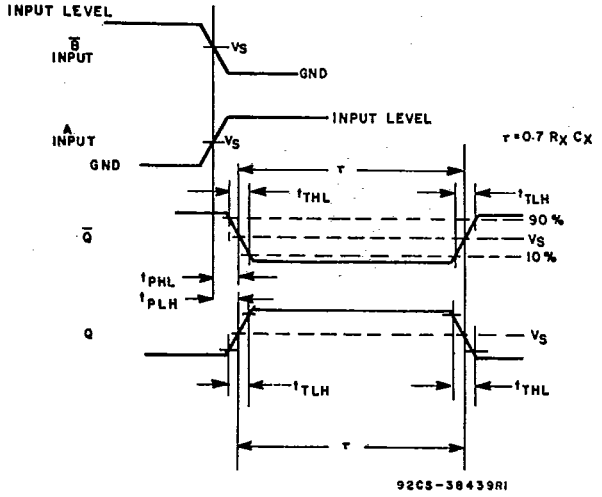

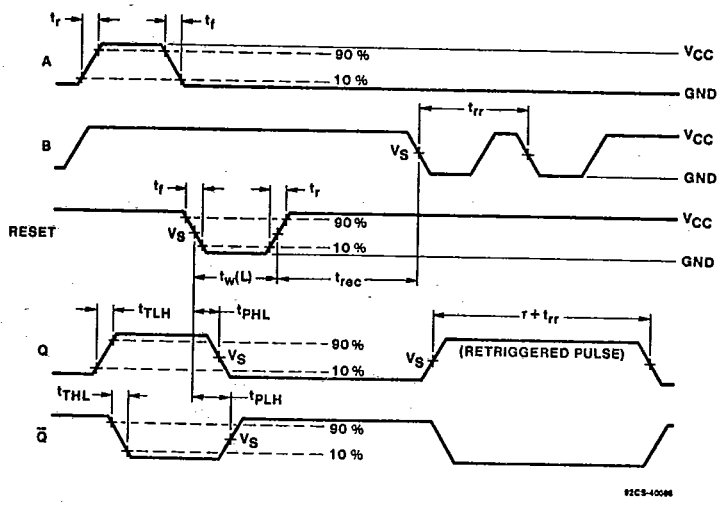

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 6 — Switching Waveforms

Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit or with a poorly filtered power supply, the energy stored in C_X could discharge into Pin 2 or 14. To avoid possible device damage in this mode, when C_X is ≥ 0.5 microfarad, a protection diode with a 1-ampere or higher rating (1N5395 or equivalent) and a separate ground return for C_X should be provided as shown in Fig. 7.

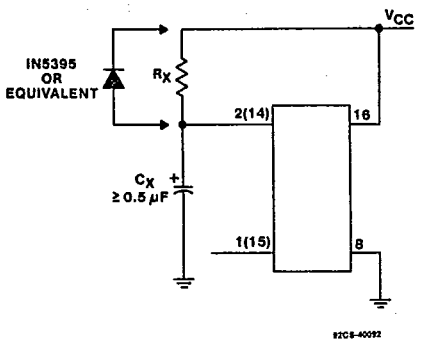

Fig. 7 — Rapid power-down protection circuit.

An alternate protection method is shown in Fig. 8, where a 51-ohm current-limiting resistor is inserted in series with C_X. Note that a small pulse width decrease will occur however, and R_X must be appropriately increased to obtain the originally desired pulse width.

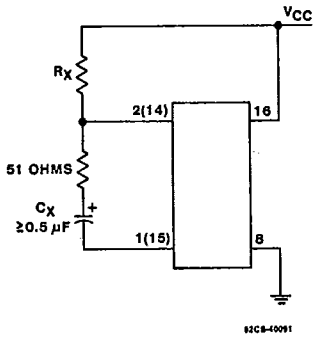

Fig. 8 — Alternate rapid power-down protection circuit.