REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21												

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
93-06-24

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, FAST CMOS, 8 BIT, BUS INTERFACE, D REGISTERS WITH CLOCK ENABLE, ASYNCHRONOUS CLEAR, THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS AND LIMITED OUTPUT VOLTAGE SWING, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-92230
A	67268	

SHEET 1 OF 21

DESC FORM 193
JUL 91

5962-E229-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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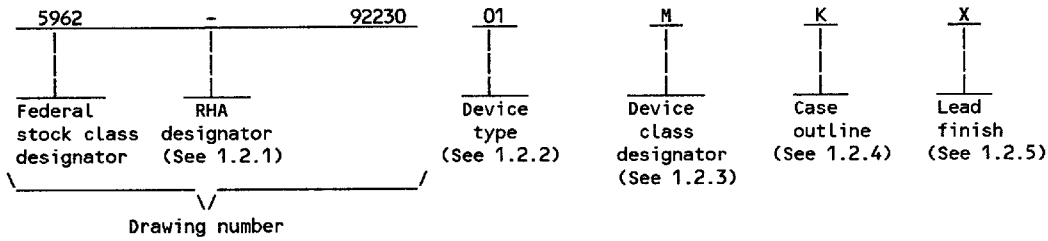
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01, 02	54FCT825AT	Fast CMOS, 8-bit, bus interface D registers with clock enable, asynchronous clear, three-state outputs, TTL compatible inputs and limited output voltage swing.
03, 04	54FCT825BT	Fast CMOS, 8-bit, bus interface D registers with clock enable, asynchronous clear, three-state outputs, TTL compatible inputs and limited output voltage swing.
05, 06	54FCT825CT	Fast CMOS, 8-bit, bus interface D registers with clock enable, asynchronous clear, three-state outputs, TTL compatible inputs and limited output voltage swing.

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	flat package
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line
3	CQCC1-N28	28	leadless-chip-carrier package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc 4/
DC input clamp current (I_{IK}) (V_{IN} = -0.5 V)	-20 mA
DC output clamp current (I_{OK}) (V_{OUT} = -0.5 V and +7.0 V)	±20 mA
DC output source current (I_{OH}) per output	-30 mA
DC output sink current (I_{OL}) per output	+70 mA
DC V_{CC} current (I_{CC})	±268 mA
DC ground current (I_{GND})	±588 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Case temperature under bias (T_{BIAS})	-65°C to +135°C
Maximum power dissipation (P_D)	500 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V
Minimum high level input voltage (V_{IH})	2.0 V
Case operating temperature range (T_C)	-55°C to +125°C
Maximum input rise and fall rate (t_r, t_f):	
(from V_{IN} = 0.3 V to 2.7 V, 2.7 V to 0.3 V)	5 ns/V
Maximum high level output current (I_{OH}):	
Device types 01, 03, and 05	-6 mA
Device types 02, 04, and 06	-12 mA
Maximum low level output current (I_{OL})	32 mA

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ For $V_{CC} \geq 6.5$ V, the upper limit on the range is limited to 7.0 V.

5/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510	-	Microcircuits, General Specification for.
MIL-I-38535	-	Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480	-	Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883	-	Test Methods and Procedures for Microelectronics.
MIL-STD-1835	-	Microcircuit Case Outlines

BULLETIN

MILITARY

MIL-BUL-103	-	List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780	-	Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce load circuit and waveforms shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range. Test conditions for these specified characteristics and limits are as specified in table I.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 38 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 2/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
High level output voltage 3006	V_{OH1} 4/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL}, $V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$; For all other inputs $V_{IN} = V_{CC}$ or GND; $I_{OH} = -300\ \mu A$	All	4.5 V	1,2,3	2.7	V_{CC}-0.5	V
	V_{OH2}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL}, $V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$; For all other inputs $V_{IN} = V_{CC}$ or GND; $I_{OH} = -6\ mA$	01,03, 05	4.5 V	1,2,3	2.4	V_{CC}-0.5	
		$I_{OH} = -12\ mA$	01,03, 05			2.0	V_{CC}-0.5	
		$I_{OH} = -12\ mA$	02,04, 06			2.4	V_{CC}-0.5	
Low level output voltage 3007	V_{OL1} 4/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL}, $V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$; For all other inputs $V_{IN} = V_{CC}$ or GND; $I_{OL} = 300\ \mu A$	All	4.5 V	1,2,3		0.20	V
	V_{OL2}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL}, $V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$; For all other inputs $V_{IN} = V_{CC}$ or GND; $I_{OL} = 32\ mA$	All	4.5 V	1,2,3		0.55	
Three-state output leakage current high 3021	I_{OZH} 5/ 6/	$\overline{OEn} = V_{IH}$ or V_{IL}, $V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$; For all other inputs $V_{IN} = V_{CC}$ or GND; $V_{OUT} = V_{CC}$	01,03, 05	5.5 V	1,2		1.0	µA
					3		10.0	
			02,04, 06		1		0.1	
					2,3		2.0	
Three-state output leakage current low 3020	I_{OZL} 5/ 6/	$\overline{OEn} = V_{IH}$ or V_{IL}, $V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$; For all other inputs $V_{IN} = V_{CC}$ or GND; $V_{OUT} = GND$	01,03, 05	5.5 V	1,2		-1.0	µA
					3		-10.0	
			02,04, 06		1		-0.1	
					2,3		-2.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 2/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
Negative input clamp voltage 3022	V_{IC-}	For input under test $I_{IN} = -18$ mA	01,03, 05	4.5 V	1,2,3		-1.2	V
		For input under test $I_{IN} = -15$ mA	02,04, 06				-1.3	
Input current high 3010	I_{IH}	For input under test $V_{IN} = V_{CC}$ For all other inputs $V_{IN} = V_{CC}$ or GND	01,03, 05	5.5 V	1,2		1.0	µA
					3		5.0	
			02,04, 06		1,2		0.1	
					3		1.0	
Input current low 3009	I_{IL}	For input under test $V_{IN} = GND$ For all other inputs $V_{IN} = V_{CC}$ or GND	01,03, 05	5.5 V	1,2		-1.0	µA
					3		-5.0	
			02,04, 06		1,2		-0.1	
					3		-1.0	
Input capacitance 3012	C_{IN} 7/	See 4.4.1c $T_C = +25°C$	All	GND	4		10	pF
Output capacitance 3012	C_{OUT} 7/	See 4.4.1c $T_C = +25°C$	All	GND	4		12	pF
Short circuit output current 3005	I_{OS} 8/	For all inputs $V_{IN} = V_{CC}$ or GND $V_{OUT} = GND$	All	5.5 V	1,2,3	-60	-225	mA
Dynamic Power supply current	I_{CCD} 4/ 9/	Outputs open	All	5.5 V	4,5,6		0.25	mA/ MHz•Bit
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 10/	For input under test $V_{IN} = V_{CC} - 2.1$ V For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1,2,3		2.0	mA
Quiescent supply current output high 3005	I_{CCH}	For all inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1,2,3		1.5	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 2/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type	V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
Quiescent supply current output low 3005	I_{CCL}	For all inputs $V_{IN} = V_{CC}$ or GND		All	5.5 V	1,2,3		1.5	mA
Quiescent supply current output three-state 3005	I_{CCZ} 5/	For all inputs $V_{IN} = V_{CC}$ or GND		All	5.5 V	1,2,3		1.5	mA
Total supply current	I_{CCT} 11/	Outputs open, $\overline{OE} = \overline{EN}$ = GND, $\overline{CLR} = V_{CC}$, f_{CP} = 10MHz, One bit toggling f_{in} = 5 MHz, 50% Duty cycle, For nonswitching inputs $V_{IN} = V_{CC}$ or GND	For switching inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	4,5,6		4.0	mA
			For switching inputs V_{IN} = 3.4 V or GND			4,5,6		6.0	
		Outputs open, 3/ $\overline{OE} = \overline{EN}$ = GND, $\overline{CLR} = V_{CC}$, f_{CP} = 10MHz, Eight bits toggling f_{IN} = 2.5 MHz, 50% Duty cycle, For nonswitching inputs $V_{IN} = V_{CC}$ or GND	For switching inputs $V_{IN} = V_{CC}$ or GND			4,5,6		7.8	
			For switching inputs V_{IN} = 3.4 V or GND			4,5,6		16.8	
Low level ground bounce noise	V_{OLP} 7/ 12/	V_{IH} = 3.0 V, V_{IL} = 0.0 V, T_A = +25 °C, See figure 4		All	5.0 V	4		1450	mV
Low level ground bounce noise	V_{OLV} 7/ 12/			All	5.0 V	4		-1100	mV
High level V_{CC} bounce noise	V_{OHP} 7/ 12/			All	5.0 V	4		600	mV
High level V_{CC} bounce noise	V_{OHV} 7/ 12/			All	5.0 V	4		-550	mV
Functional test	13/	V_{IL} = 0.8 V, V_{IH} = 2.0 V, Verify output V_O, See 4.4.1d		All	4.5 V	7,8	L	H	
		V_{IL} = 0.8 V, V_{IH} = 2.0 V, Verify output V_O, See 4.4.1d		All	5.5 V	7,8	L	H	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 2/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type	V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
Propagation delay time, clock to output, CP to Yn 3003	t_{PHL}, t_{PLH} 14/	R_L = 500Ω, See figure 5	C_L = 50 pF minimum	01,02	4.5 V	9,10,11	1.5	11.5	ns
			C_L = 300 pF minimum4/				1.5	20.0	
			C_L = 50 pF minimum	03,04			1.5	8.5	
			C_L = 300 pF minimum4/				1.5	16.0	
			C_L = 50 pF minimum	05,06			1.5	7.0	
			C_L = 300 pF minimum4/				1.5	13.5	
Propagation delay time, clear to output, CLR to Yn 3003	t_{PHL} 14/	C_L = 50 pF minimum, R_L = 500Ω, See figure 5		01,02	4.5 V	9,10,11	1.5	15.0	ns
				03,04			1.5	9.5	
				05,06			1.5	8.5	
Propagation delay time, output enable, OEn to Yn 3003	t_{PZL}, t_{PZH} 14/	R_L = 500Ω, See figure 5	C_L = 50 pF minimum	01,02	4.5 V	9,10,11	1.5	13.0	ns
			C_L = 300 pF minimum4/				1.5	25.0	
			C_L = 50 pF minimum	03,04			1.5	9.0	
			C_L = 300 pF minimum4/				1.5	16.0	
			C_L = 50 pF minimum	05,06			1.5	8.0	
			C_L = 300 pF minimum4/				1.5	13.5	
Propagation delay time, output disable, OEn to Yn 3003	t_{PLZ}, t_{PHZ} 14/	R_L = 500Ω, See figure 5	C_L = 5 pF minimum 4/	01,02	4.5 V	9,10,11	1.5	8.0	ns
			C_L = 50 pF minimum				1.5	9.0	
			C_L = 5 pF minimum 4/	03,04			1.5	7.0	
			C_L = 50 pF minimum				1.5	8.0	
			C_L = 5 pF minimum 4/	05,06			1.5	6.0	
			C_L = 50 pF minimum				1.5	6.5	
Set-up time, data high and low to clock, Dn to CP	t_s 14/	C_L = 50 pF minimum, R_L = 500Ω, See figure 5		01,02	4.5 V	9,10,11	4.0		ns
				03,04			3.0		
				05,06			3.0		
Hold time, data high and low from clock, Dn from CP	t_h 14/	C_L = 50 pF minimum, R_L = 500Ω, See figure 5		01,02	4.5 V	9,10,11	2.0		ns
				03,04			1.5		
				05,06			1.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 2/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
Clock pulse width, CP high and low	t_w 14/	C_L = 50 pF minimum, R_L = 500Ω, See figure 5	01,02	4.5 V	9,10,11	7.0		ns
			03,04			6.0		
			05,06			6.0		
Set-up time, clock enable high and low to clock, EN to CP	t_s 14/	C_L = 50 pF minimum, R_L = 500Ω, See figure 5	01,02	4.5 V	9,10,11	4.0		ns
			03,04			3.0		
			05,06			3.0		
Hold time, clock enable high and low from clock, EN from CP	t_h 14/	C_L = 50 pF minimum, R_L = 500Ω, See figure 5	01,02	4.5 V	9,10,11	2.0		ns
			03,04			0.0		
			05,06			0.0		
Clear pulse width low, CLR low	t_w 14/	C_L = 50 pF minimum, R_L = 500Ω, See figure 5	01,02	4.5 V	9,10,11	7.0		ns
			03,04			6.0		
			05,06			6.0		
Recovery time, clear to clock, CLR to CP	t_{rec} 14/	C_L = 50 pF minimum, R_L = 500Ω, See figure 5	01,02	4.5 V	9,10,11	7.0		ns
			03,04			6.0		
			05,06			6.0		

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ For negative and positive voltage and current values: The sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I at $4.5\ V \le V_{CC} \le 5.5\ V$.

4/ This parameter is guaranteed, if not tested, to the limits specified in table I.

5/ Three-state output conditions are required.

6/ This test may be performed using V_{IH} = 3.0 V. When V_{IH} = 3.0 V is used, the test is guaranteed for V_{IH} = 2.0 V.

7/ This test is required only for Group A testing, see 4.4.1 herein.

8/ Not more than one output should be shorted at a time. The duration of the short circuit test should not exceed one second.

9/ I_{CCD} may be verified by the following equation:

$$I_{CCD} = \frac{I_{CCT} - I_{CC} - D_H N_T \Delta I_{CC}}{f_{CP}/2 + f_i N_i}$$

where I_{CCT}, I_{CC} (I_{CCL} or I_{CCH} in table I), and ΔI_{CC} shall be the measured values of these parameters, for the device under test, when tested as described in table I, herein. The values for D_H, N_T, f_{CP}, f_i, N_i shall be as listed in the test conditions column for I_{CCT} in table I, herein.

10/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1$ V (alternate method). Classes B, S, Q, and V shall use the preferred method. When the test is performed using the alternate test method: the maximum limit is equal to the number of inputs at a high TTL input level times 2.0 mA; and the preferred method and limits are guaranteed.

11/ I_{CCT} is calculated as follows:
$I_{CCT} = I_{CC} + D_H N_T \Delta I_{CC} + I_{CCD}(f_{CP}/2 + f_i N_i)$

where
I_{CC} = Quiescent supply current (any I_{CCL} or I_{CCH})
D_H = Duty cycle for TTL inputs at 3.4 V
N_T = Number of TTL inputs at 3.4 V
ΔI_{CC} = Quiescent supply current delta, TTL inputs at 3.4 V
I_{CCD} = Dynamic power supply current caused by an input transition pair (HLH or LHL)
f_{CP} = Clock frequency for registered devices (f_{CP} = 0 for nonregistered devices)
f_i = Input frequency
N_i = Number of inputs at f_i

12/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500 Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than .25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

For device types 02, 04, and 06, limits will be added when these device types become available from an approved source of supply.

13/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 1.5 V, L < 1.5 V.

14/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum propagation delay time limits for V_{CC} = 4.5 V and 5.5 V are guaranteed if not tested to the limits specified in table I, herein. For ac tests, all paths must be tested.

Device types	01,02,03,04,05,06	
Case outlines	R and S	2
Terminal number	Terminal symbol	
1	$\overline{OE1}$	NC
2	OE2	$\overline{OE1}$
3	D0	$\overline{OE2}$
4	D1	D0
5	D2	D1
6	D3	D2
7	D4	D3
8	D5	NC
9	D6	D4
10	D7	D5
11	CLR	D6
12	GND	D7
13	CP	CLR
14	EN	GND
15	Y7	NC
16	Y6	CP
17	Y5	EN
18	Y4	Y7
19	Y3	Y6
20	Y2	Y5
21	Y1	Y4
22	Y0	NC
23	$\overline{OE3}$	Y3
24	V_{CC}	Y2
25	---	Y1
26	---	Y0
27	---	$\overline{OE3}$
28	---	V_{CC}

Pin descriptions	
Terminal symbol	Description
Dn (n = 0 to 7)	D flip-flop data inputs.
$\overline{OEn}$ (n= 0 to 2)	Three-state output enable control inputs.
CP	Clock (timing) input for the register. Enters data into the register on low-to high transition.
$\overline{CLR}$	Asynchronous clear control input.
$\overline{EN}$	Synchronous clock enable control input.
Yn (n = 0 to 7)	Register three-state outputs (noninverting).

FIGURE 1. Terminal connections.

All device types							
Function	Inputs					Outputs	
						Internal	External
	$\overline{OEn}$ 1/	$\overline{CLR}$	$\overline{EN}$	CP	Dn	$\overline{Qn}$	Yn
High impedance	H	H	L	↑	L	H	Z
	H	H	L	↑	H	L	Z
Clear	H	L	X	X	X	H	Z
	L	L	X	X	X	H	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	↑	L	H	Z
	H	H	L	↑	H	L	Z
	L	H	L	↑	L	H	L
	L	H	L	↑	H	L	H

H = High voltage level
Z = High impedance
L = Low voltage level

↑ = Low-to-high transition.
NC = No change
X = Don't care

1/ $\overline{OEn}$ = H means one or more of the following inputs are at a high voltage level: OE1, OE2, or OE3. OEn = L means all of these inputs are at a low voltage level.

FIGURE 2. Truth table.

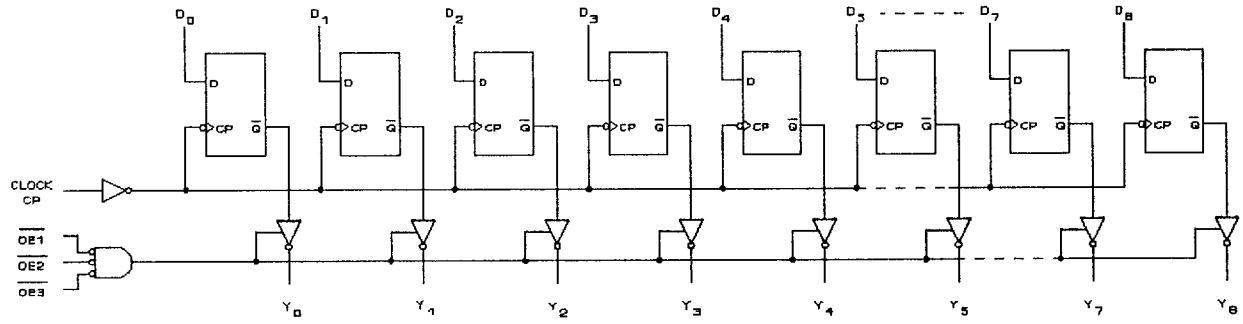
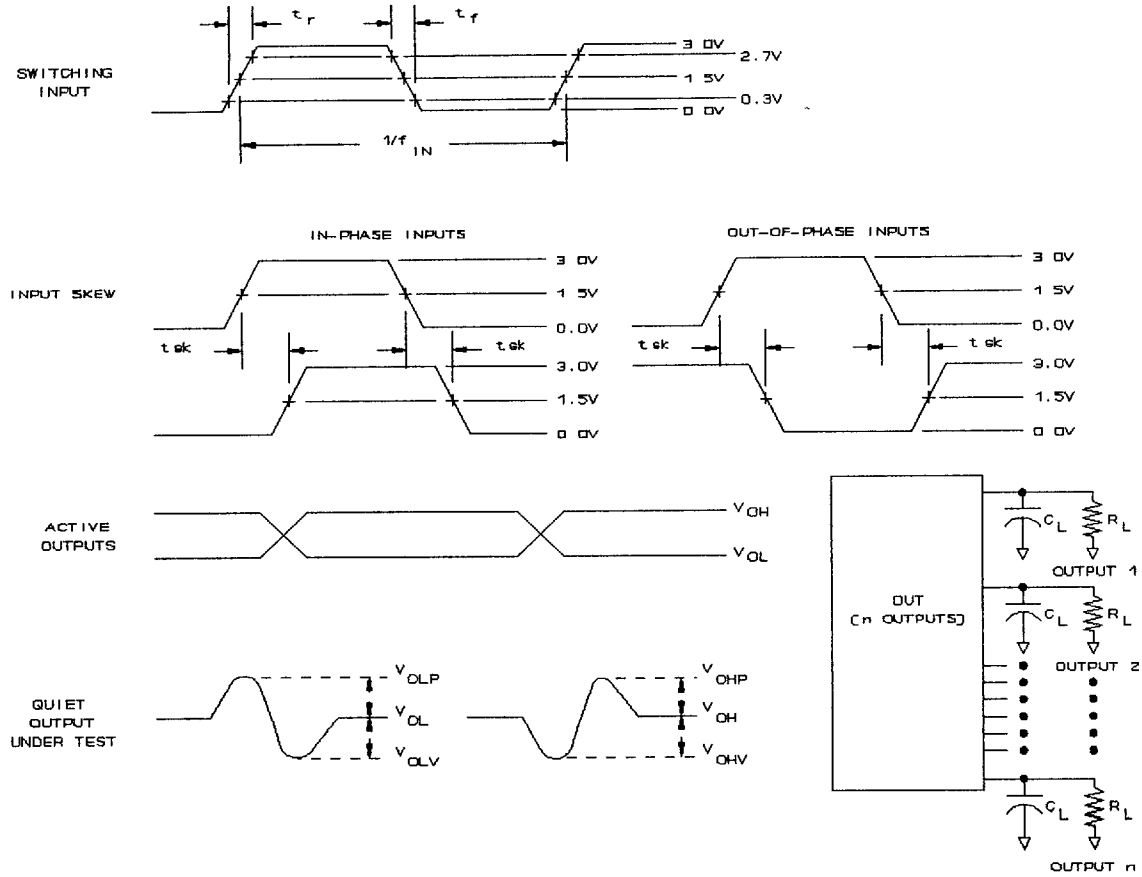


FIGURE 3. Logic diagram.



NOTES:

C_L = 47 pF -0 percent, +20 percent chip capacitor plus ≥ 3 pF of equivalent capacitance from the test jig and probe.

R_L = 450 Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.

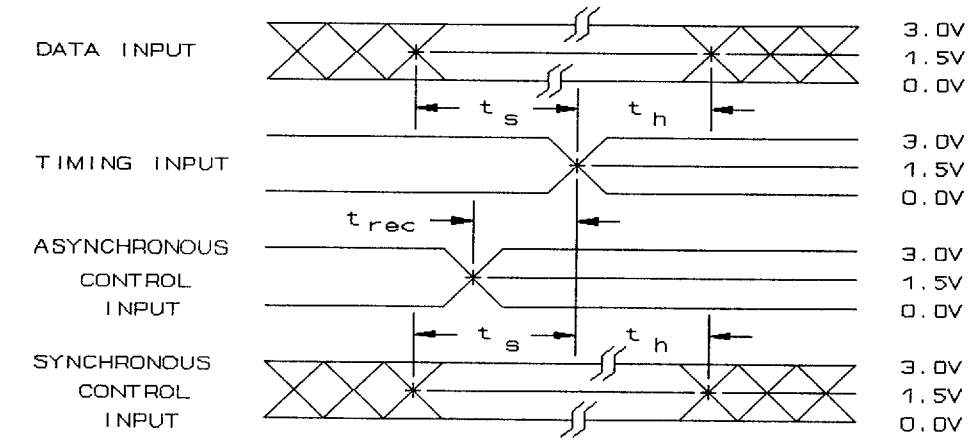
Input signal to the device under test:

V_{IN} = 0.0 V to 3.0 V; duty cycle = 50 percent; f_{IN} ≥ 1 MHz.

t_r, t_f = 3 ns ±1.0 ns. For input signal generators incapable of maintaining this values of t_r and t_f, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns;

Skew between any two switching inputs signals (t_{sk}): ≤ 250 ps.

FIGURE 4. Ground bounce load circuit and waveforms.



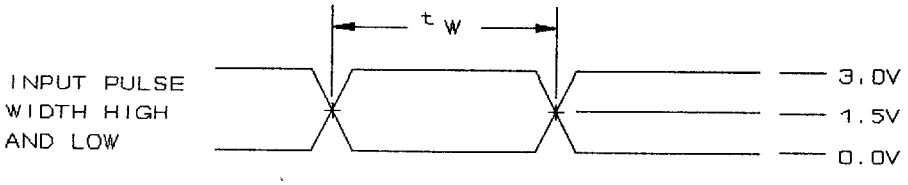
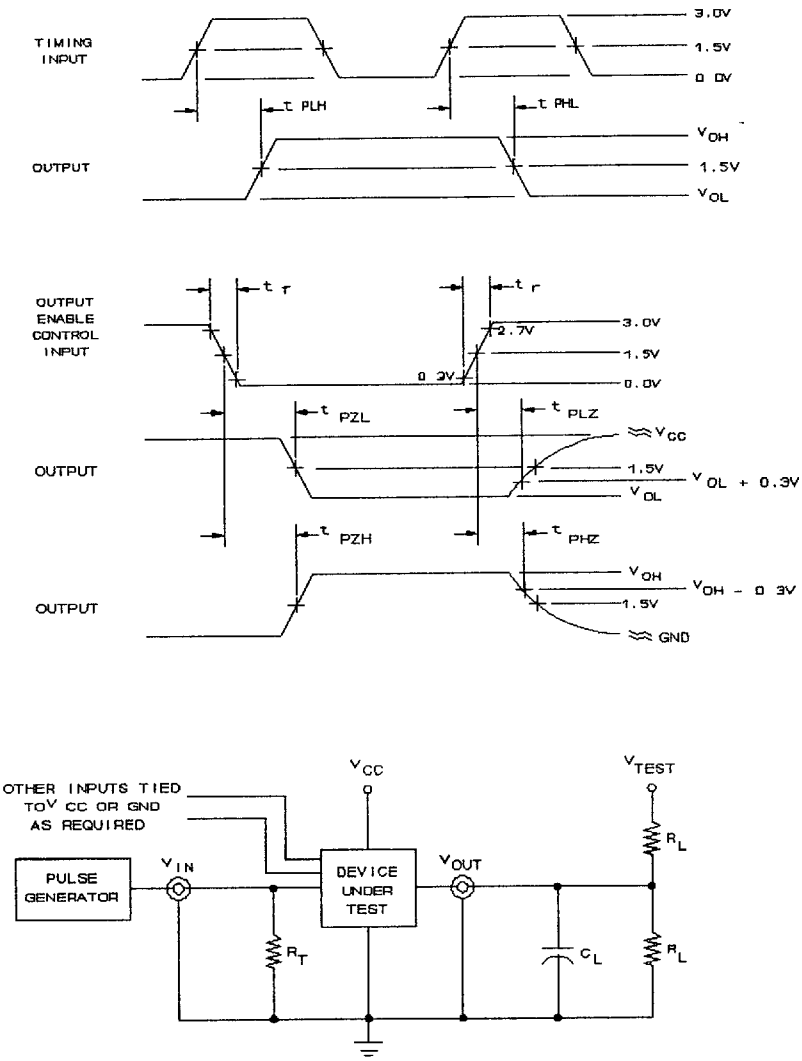


FIGURE 5. Switching waveforms and test circuit - Continued.



NOTES:
When measuring t_{PLZ} and t_{PZL} : V test = 7.0 V
When measuring t_{PHZ}, t_{PZH}, t_{PLH} and t_{PHL} : V test = open
The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.

C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance)
R_L = 500Ω or equivalent
R_T = 50Ω or equivalent
Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; duty cycle = 50 percent;
t_r ≤ 2.5 ns; t_f ≤ 2.5 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V, and 2.7 V to 0.3 V, respectively.
Timing parameters shall be tested at a minimum input frequency of 1 MHz.
The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device class B, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device class S, sampling and inspection procedures shall be in accordance with MIL-M-38510, and methods 5005 and 5007 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. The following additional criteria shall apply.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

(3) For device class M, unless otherwise noted, the requirements for device class B in method 1015 of MIL-STD-883 shall be followed.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1	1	1	1
Final electrical parameters (see 4.2)	1/ 1,2,3, 4,5,6,7,8, 9,10,11	1/ 1,2,3, 4,5,6,7,8, 9,10,11	2/ 1,2,3, 4,5,6,7,8, 9,10,11	1/ 1,2,3, 4,5,6,7,8, 9,10,11	2/ 1,2,3, 4,5,6,7,8, 9,10,11
Group A test requirements (see 4.4)	1,2,3,4, 5,6,7,8,9, 10,11	1,2,3,4, 5,6,7,8,9, 10,11	1,2,3,4, 5,6,7,8,9, 10,11	1,2,3,4, 5,6,7,8, 9,10,11	1,2,3,4, 5,6,7,8,9, 10,11
Group B end-point electrical parameters (see 4.4)			1,2,3,4,7, 8,9,10,11		1,2,3,4,7, 8,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4, 5,6	1,2,3,4, 5,6		1,2,3,4, 5,6	
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1,4,7,9	1,4,7,9	1,4,7,9	1,4,7,9	1,4,7,9

1/ PDA applies to subgroups 1 and 4 (i.e., I_{CCT} only).
2/ PDA applies to subgroups 1, 4 and 7.

4.3.3 Electrostatic discharge sensitivity qualification inspection . Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested to limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested to limits established for the worst case package. The 5 devices to be tested shall be the worst case device type supplied to this drawing. All other device types shall be guaranteed, if not tested, to the limits established for the worst case device type. The package type and device type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DESC-EC data that shall include, all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DESC-EC of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DESC-EC data from testing on both fixtures, that shall include, all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test."

c. C_{IN} and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{OUT}, test all applicable pins on five devices with zero failures.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. Class S steady-state life (accelerated) shall be conducted using test condition D of method 1005 of MIL-STD-883. For device class S steady-state life tests, the test circuit shall be submitted to and approved by the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-M-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as specified in table I at T_A = +25°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331, and as follows:

GND - - - - - - - - - - - - - - Ground zero voltage potential.
I_{CC} - - - - - - - - - - - - - - Quiescent supply current.
I_{IL} - - - - - - - - - - - - - - Input current low.
I_{IH} - - - - - - - - - - - - - - Input current high.
T_C - - - - - - - - - - - - - - Case temperature.
T_A - - - - - - - - - - - - - - Ambient temperature.
V_{CC} - - - - - - - - - - - - - - Positive supply voltage.
C_{IN} - - - - - - - - - - - - - - Input terminal-to-GND capacitance.
V_{IC-} - - - - - - - - - - - - - - Negative input clamp voltage.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.