REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20			

PMIC N/A	PREPARED BY Greg A. Pitz	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444
STANDARDIZED MILITARY DRAWING	CHECKED BY Ray Monnin	MICROCIRCUITS, DIGITAL, BIPOLAR, INTERRUPT HANDLER, MONOLITHIC SILICON
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	APPROVED BY	SIZE A / CAGE CODE 67268 / 5962-88666
AMSC N/A	DRAWING APPROVAL DATE 10 JUNE 1988	SHEET 1 OF 20
	REVISION LEVEL	

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

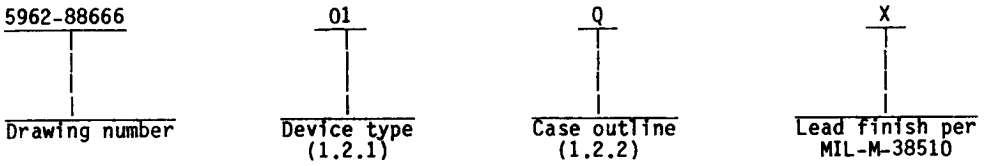
5962-E933

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	68155	Interrupt handler

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage	-0.5 V dc to +5.5 V dc
Voltage applied to output in off-state	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.2 W
Lead temperature (soldering, 5 seconds)	300°C
Junction temperature (T_J)	175°C
Thermal resistance, junction to case (θ_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage range:	
(V_{CC})	4.5 V dc to 5.5 V dc
(V_{BB})	1.35 V dc to 1.65 V dc
High level input voltage (V_{IH})	2.0 V to V_{CC}
Low level input voltage (V_{IL})	0.8 V dc maximum
Low level output current	8.0 mA
High level output current	-3.0 µA
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Supply voltage	V_{CC}			4.5	5.5	V
Supply voltage	V_{BB}			1.35	1.65	V
V_{CC} supply current	I_{CC}	V_{CC} = 5.5 V	1,2,3		100	mA
V_{BB} supply current	I_{BB}	V_{BB} = 1.65 V	1,2,3		200	mA
Input low current	I_{IL}	V_{IL} = 0.4 V, V_{CC} = 5.5 V, V_{BB} = 1.65 V	1,2,3		-20	µA
Input high current	I_{IH}	V_{IH} = 2.7 V, V_{CC} = 5.5 V, V_{BB} = 1.65 V	1,2,3		20	µA
Short circuit output current except LDTACKN (O.C.)	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0 V 2/	1,2,3	-15	-100	mA
Output low voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = 4.5 V, V_{BB} = 1.35 V	1,2,3		0.6	V
Output high voltage except LDTACKN (O.C.)	V_{OH}	I_{OH} = -3 mA, V_{CC} = 4.5 V, V_{BB} = 1.35 V	1,2,3	2.5		V
Input leakage current	I_{II}	V_{CC} = 5.5 V, V_I = 5.5 V	1,2,3		100	µA
Open collector leakage LDTACKN	I_{CEX}	V_{CC} = 4.5 V, V_O = 4.5 V	1,2,3		100	µA
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IC} = -10 mA	1,2,3		-1.5	V
Input low voltage	V_{IL}		1,2,3		0.8	V
Input high voltage	V_{IH}		1,2,3	2.0		V
Functional tests		See 4.3.1c	7,8			

See footnotes at end of table I.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
R/WN to CSDSN low set-up time	t_{RWS}	Register read, see figure 3	9,10,11	5		ns
IACKDSN high to CSDSN low set-up time	t_{IAKS}		9,10,11	42		ns
A1-A3 valid to CSDSN low set-up time	t_{ADRS}		9,10,11	29		ns
CSDSN low to DO-D7 set-up time	t_{DTV}		9,10,11		164	ns
CSDSN low to LDTACKN low read access time	t_{ACCR}		9,10,11	CLK +33	2CLK +175	ns
CSDSN high to R/WN high hold time	t_{RWH}		9,10,11	16		ns
CSDSN high to A1-A3 valid hold time	t_{ADRH}		9,10,11	6		ns
CSDSN high to DO-D7 valid hold time	t_{DTH}		9,10,11	34	104	ns
CSDSN high to DO-D7 three state 3/	t_{TST}		9,10,11	34	104	ns
CSDSN high to LDTACKN high time	t_{ACK}		9,10,11	15	56	ns
CSDSN high time	t_{CSH}		9,10,11	42		ns
LDTACKN low to CSDSN high	t_{DTCS}		9,10,11	18		ns
R/WN low to CSDSN low set-up time	t_{RWS2}	Register write, see figure 4	9,10,11	5		ns

See footnotes at end of table I.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
IACKDSN high to CSDSN low set-up time	t_{IAKS}	Register write, see figure 4	9,10,11	42		ns
A1-A3 valid to CSDSN low set-up time	t_{ADRS}		9,10,11	29		ns
D0-D7 valid to CSDSN set-up time	t_{DS}		9,10,11	0		ns
CSDSN low to LDTACKN low write access time	t_{ACCW}		9,10,11	CLK +33	2CLK +175	ns
CSDSN high to R/WN low hold time	t_{RWH2}		9,10,11	16		ns
CSDSN high to A1-A3 valid hold time	t_{ADRH}		9,10,11	6		ns
CSDSN high to D0-D7 valid hold time	t_{DH}		9,10,11	0		ns
CSDSN high to LDTACKN high time	t_{ACK}		9,10,11	15	56	ns
CSDSN high time	t_{CSH}		9,10,11	42		ns
LDTACKN low to CSDSN high time	t_{DTCS}		9,10,11	18		ns
CSDSN high to IACKDSN low set-up time	t_{CSS}	Vector mode, see figure 5	9,10,11	42		ns
IACKDSN low to LIACKN low propagation time	t_{PDL}		9,10,11	CLK +33	2CLK +175	ns
IACKDSN low to D0-D7 vector valid	t_{DAV}		9,10,11		189	ns

See footnotes at end of table I.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
IACKDSN low to LDTACKN low (vector access time)	t_{ACCV}	Vector mode, see figure 5	9,10,11	CLK +33	2CLK +175	ns
IACKDSN high time	t_{IKH}		9,10,11	42		ns
IACKDSN high to DO-D7 valid hold time	t_{DAH}		9,10,11	34	104	ns
IACKDSN high to DO-D7 three state 4/	t_{TRST}		9,10,11	34	104	ns
IACKDSN high to LDTACKN high	t_{IKDT}		9,10,11	15	56	ns
IACKDSN high to LDTACKN high propagation delay	t_{PDH}		9,10,11	15	56	ns
LDTACKN low to IACKDSN high time	t_{DTIK}		9,10,11	18		ns
A1-A3 valid to IACKDSN low set-up time	t_{ADRS}		9,10,11	29		ns
IACKDSN high to A1-A3 valid hold time	t_{ADH}		9,10,11	6		ns
CSDSN high to IACKDSN low set-up time	t_{CSS}	See figure 6	9,10,11	42		ns
IACKDSN low to LIACKN low propagation time delay	t_{PDL}		9,10,11	CLK +33	2CLK +175	ns
IACKDSN high time	t_{IKH}		9,10,11	42		ns
IACKDSN high to LIACKN high propagation delay	t_{PDH}		9,10,11	15	56	ns

See footnotes at end of table I.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
A1-A3 valid to IACKDSN low set-up time	t_{ADS}	See figure 6	9,10,11	29		ns
IACKDSN high to A1-A3 valid hold time	t_{ADH}		9,10,11	6		ns
CSDSN high IACKDSN low set-up time	t_{CSS}	Bus interrupt acknowledge, see figure 7	9,10,11	42		ns
IACKDSN low to BIACKN low propagation delay	t_{PDL2}		9,10,11	CLK +33	2CLK +175	ns
IACKDSN high time	t_{IKH}		9,10,11	42		ns
IACKDSN high to BIACKN high propagation delay	t_{PDH2}		9,10,11	15	56	ns
A1-A3 valid to IACKDSN low set-up time	t_{ADS}		9,10,11	29		ns
IACKDSN high to A1-A3 hold time	t_{ADH}		9,10,11	6		ns
RESETN low time	t_{RST}	See figure 8	9,10,11	31		ns
Clock period	t_{CKPD}	Clock timing, see figure 9	9,10,11	100		ns
Clock high	t_{CKH}		9,10,11	45		ns
Clock low	t_{CKL}		9,10,11	35		ns
CSDSN low to CLK high set-up time	t_{CSSU}		9,10,11	45		ns

1/ All voltages measurements are reference to ground (GND). For testing, all inputs swing between 0.4 V and 2.4 V with a transition time of ≤ 3 ns maximum and output voltages are checked at 1.5 V.
2/ At anytime, no more than one output should be connected to ground.
3/ t_{TST} is always greater than or equal to t_{DTH}.
4/ t_{TRST} is always greater than or equal to t_{DAH}.

Case Q	
Terminal Number	Terminal Symbol
1	V_{BB}
2	IRQ3N
3	IRQ4N
4	IRQ5N
5	IRQ6N
6	IRQ7N
7	D0
8	D1
9	D2
10	D3
11	D4
12	D5
13	D6
14	D7
15	LDTACKN
16	IACKDSN
17	LIACKN
18	A1
19	A2
20	GND

Case Q (con't)	
Terminal Number	Terminal Symbol
21	V_{BB}
22	A3
23	IPL0N
24	IPL1N
25	IPL2N
26	BIACKN
27	LRQ1N
28	LRQ2N
29	LRQ3N
30	LRQ4N
31	V_{CC}
32	LRQ5N
33	LRQ6N
34	RESETN
35	R/WN
36	NMIN
37	CLK
38	CSDSN
39	IRQ1N
40	IRQ2N

FIGURE 1. Terminal connections.

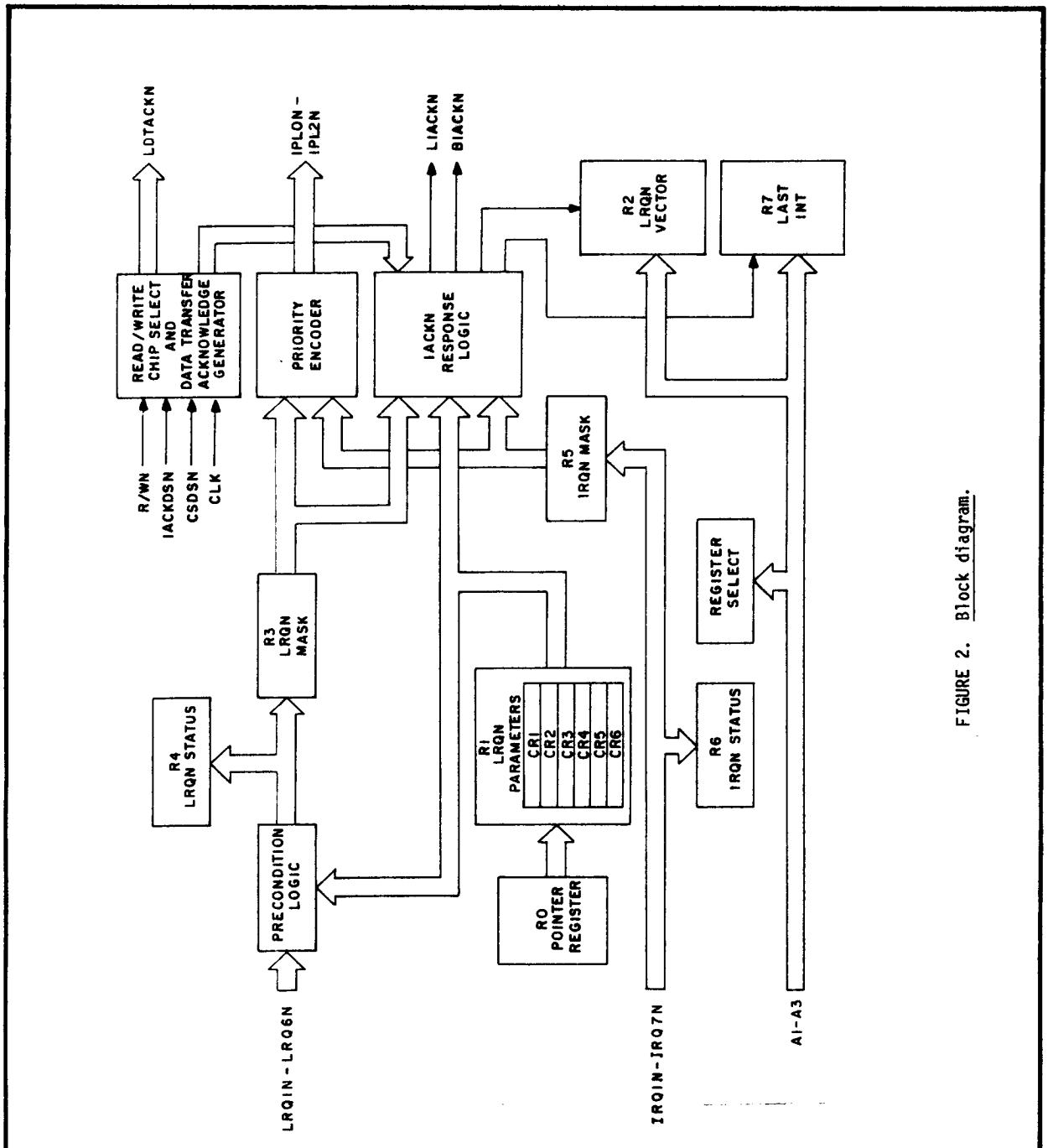


FIGURE 2. Block diagram.

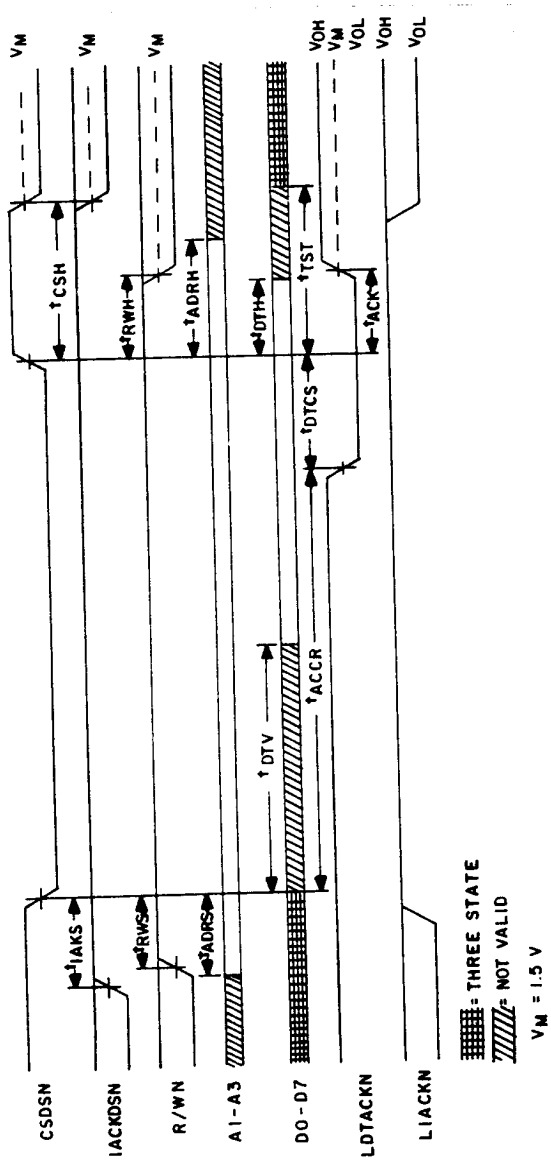


FIGURE 3. Register read.

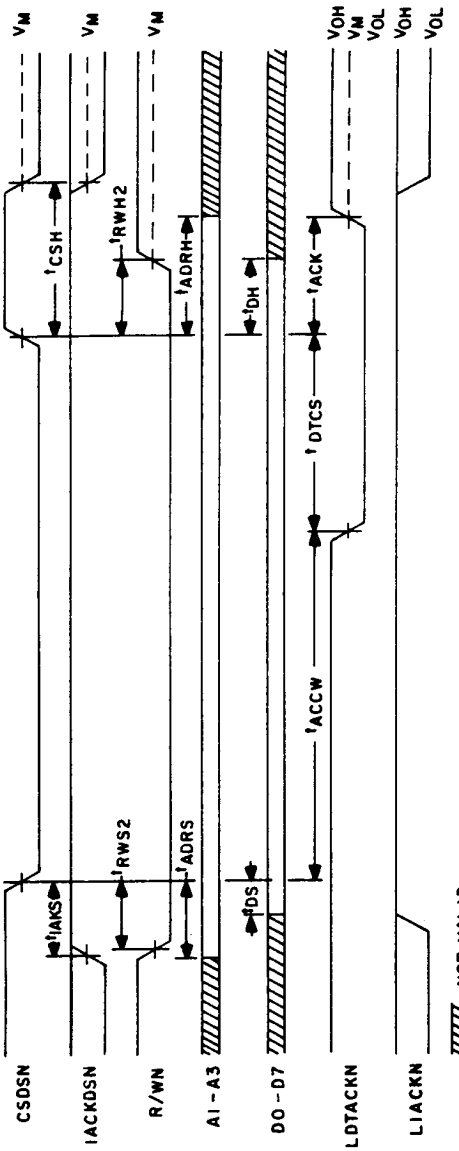


FIGURE 4. Register write.

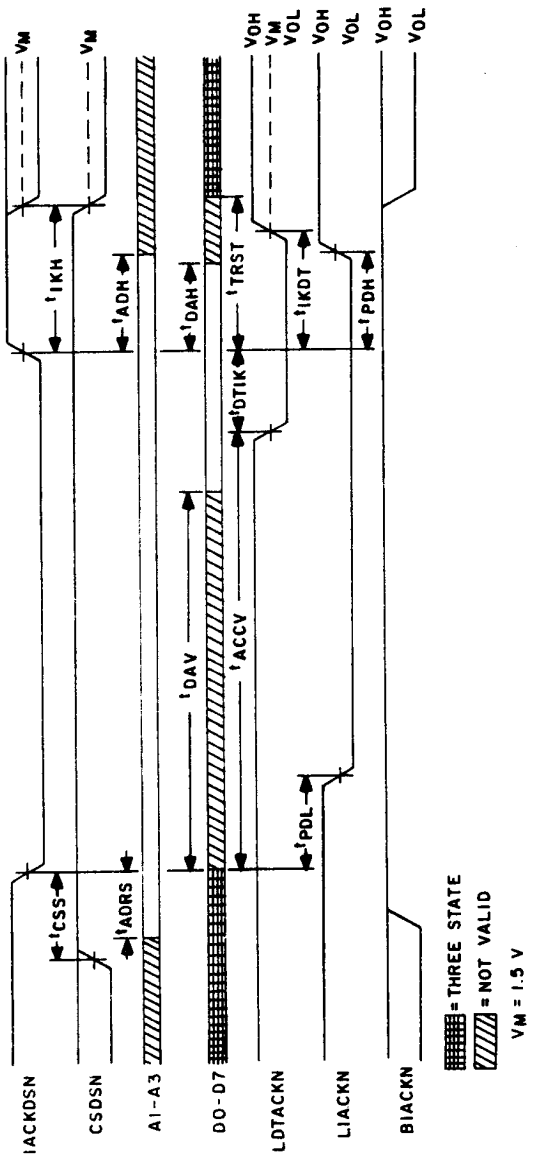


FIGURE 5. Local interrupt acknowledge (Vector mode).

☆U.S. GOVERNMENT PRINTING OFFICE: 1987 - 748-129-60913

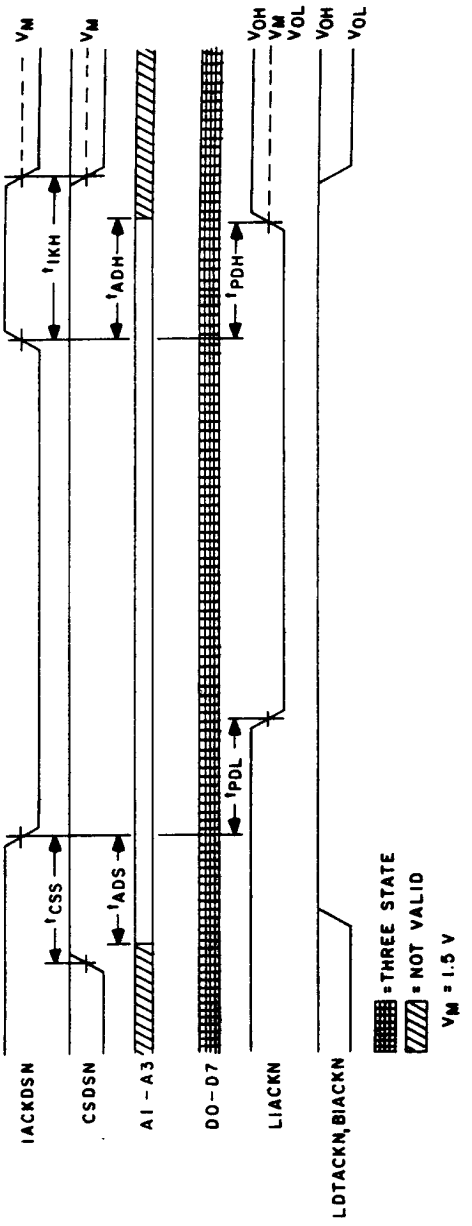


FIGURE 6. Local interrupt acknowledge (Vector mode).

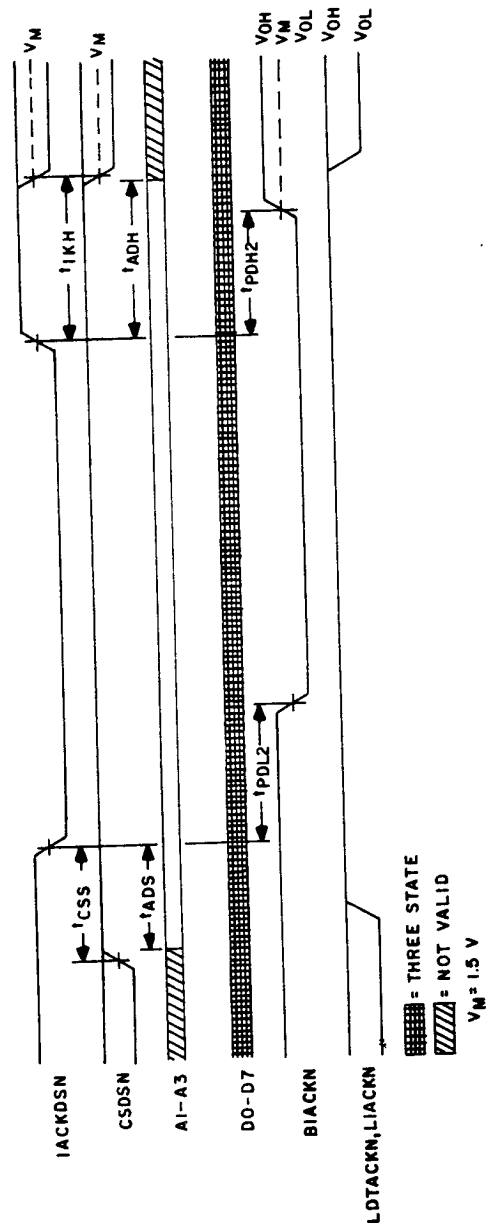


FIGURE 7. Bus interrupt acknowledge.

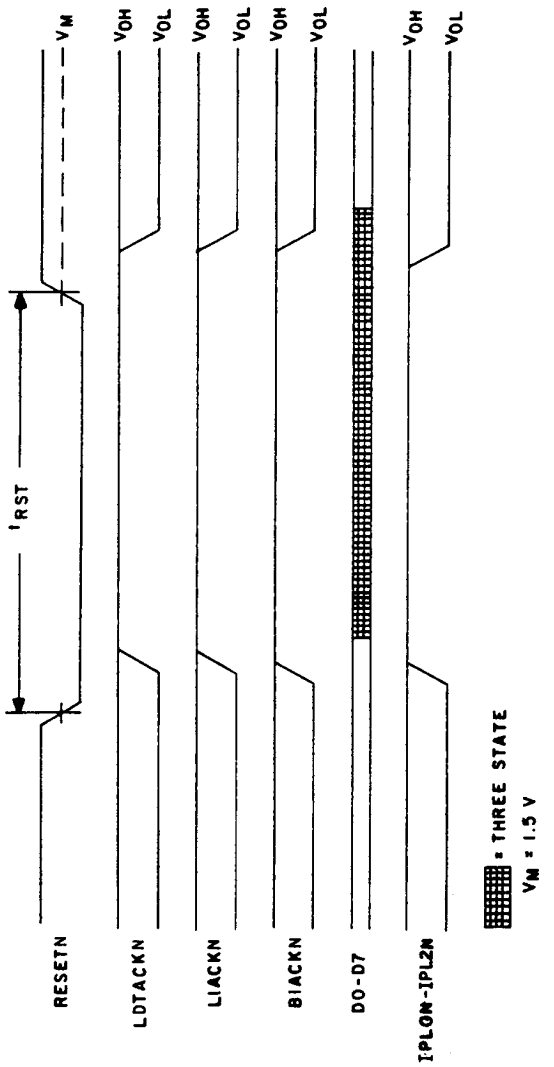


FIGURE 8. Reset.

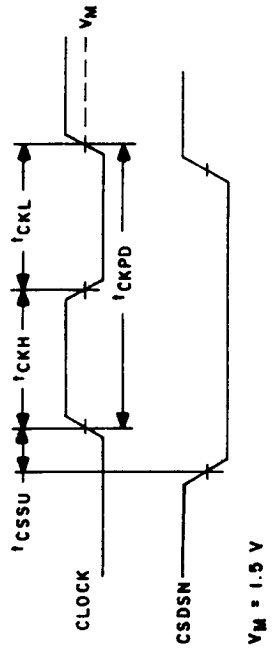


FIGURE 9. Clock.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 functional testing shall include verification of the functionality of the device. These tests form a part of the vendor's test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I) 1/, 2/
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

1/ (*) PDA applies to subgroup 1.
2/ Any subgroup at the same temperature may be combined using a multifunction tester.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Pin descriptions.

Mnemonic	Pin No.	Type	Name and function
VBB	1,21	I	Supply Voltage: Supply voltage for internal gates.
IRQ1N-IRQ7N	39,40, 2-6	I	Bus Interrupt Request: Active low inputs for bus generated interrupts.
D0-D7	7-14	I/O	Bus Data: Three-state local data bus.
LDTACKN	15	0	Local Data Transfer Acknowledge: Active low, open collector output, indicates that valid data is available on the local data bus during interrupt acknowledge cycle or data transfer cycle.
IACKDSN	16	I	Interrupt Acknowledge: Active low interrupt acknowledge input from the local master. This signal must be qualified by the local master's data strobe prior to input.
LIACKN	17	0	Local Interrupt Acknowledge: Active low interrupt acknowledge totem pole output to the local interrupting devices.
A1-A3	18,19,22	I	Address Lines: Address inputs from local master.
GND	20	I	Ground
IPL0N-IPL2N	23-25	0	Interrupt Priority Level: Active low totem pole outputs to the local master.The priority level of the interrupt request is encoded on these outputs.
BIACKN	26	0	Bus Interrupt Acknowledge: Active low interrupt acknowledge totem-pole outputs to the system bus.
LRQ1N-LRQ6N	27-30,32, 33	I	Local Interrupt Request: User can define the active state of these outputs.
V_{CC}	31	I	Supply Voltage: +5V power supply.
RESETN	34	I	Reset: Active low input reset.
R/WN	35	I	Read/Write: This signal specifies the data transfer cycle to be either read or write.
NMIN	36	I	Non-Maskable Interrupt: Active low highest priority interrupt.
CLK	37	I	Clock: Clock input (typically CPU clock).
CSDSN	38	I	Chip Select: Active low chip select input for register I/O. This input must be qualified by the local master's data strobe prior to input.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-88666012X	18324	68155/BQA	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Signetics Corporation 4130 South Market Court Sacramento, CA 95834

011238