DATA SHEET

MOS INTEGRATED CIRCUIT

μPD784044(A), 784046(A)

16-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD784046(A) is a model in the μPD784046 subseries within the 78K/IV series. A stricter quality assurance program applies μPD784046(A) compared to the μPD784046 (standard model). (In terms of NEC's quality grading, this is a "special" grade product.)

The μPD784046(A) is provided with many peripheral hardware functions such as ROM, RAM, I/O port, 10-bit resolution A/D converter, timer, serial interface, and interrupt functions, in addition to a high-speed, high-performance CPU.

The μPD784046(A) is under development.

Moreover, a flash memory model, μPD78F4046^{Note}, that can operate on the same supply voltage as the mask ROM model, and many development tools are under development.

Note Use for functional evaluation only.

The functions are described in detail in the following User's Manuals. Be sure to read these manuals when designing your system.

μPD784046 Subseries User's Manual - Hardware : U11515E
78K/IV Series User's Manual - Instruction : U10905E

FEATURES

- Higher reliability compared to the μPD784044 and 784046
- Minimum instruction execution time : 160 ns (with 12.5-MHz internal clock) ··· μPD784044(A), 784046(A)
  200 ns (with 10-MHz internal clock) ··· μPD784044(A1), (A2), 784046(A1), (A2)
- I/O port : 65 lines
- Timer : 16-bit timer/counter × 2 units
  16-bit timer × 3 units
- A/D converter : 10-bit resolution × 16 channels
- Serial interface
  UART/IOE (3-wire serial I/O) : 2 channels
- Watchdog timer : 1 channel
- Standby function
  HALT/STOP/IDLE mode
- Supply voltage : V_{DD} = 4.5 to 5.5 V

APPLICATION FIELDS

Automotive appliances, etc.

In this document, in addition to the μPD784044(A) and μPD784046(A), the μPD784044(A1), 784044(A2) 784046(A1), and 784046(A2) are also explained. However, unless otherwise specified, the μPD784046(A) is treated as the representative model throughout this document.

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ORDERING INFORMATION

Part Number	Package	Internal ROM (bytes)	Internal RAM (bytes)
μPD784044GC(A)-×××-3B9	80-pin plastic QFP (14 × 14 mm)	32 K	1024
μPD784044GC(A1)-×××-3B9	80-pin plastic QFP (14 × 14 mm)	32 K	1024
μPD784044GC(A2)-×××-3B9	80-pin plastic QFP (14 × 14 mm)	32 K	1024
μPD784046GC(A)-×××-3B9 Note	80-pin plastic QFP (14 × 14 mm)	64 K	2048
μPD784046GC(A1)-×××-3B9 Note	80-pin plastic QFP (14 × 14 mm)	64 K	2048
μPD784046GC(A2)-×××-3B9 Note	80-pin plastic QFP (14 × 14 mm)	64 K	2048

Note Under development

Remark ××× indicates ROM code suffix.

QUALITY GRADE

Special

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Differences between μPD784046 and μPD784046(A)

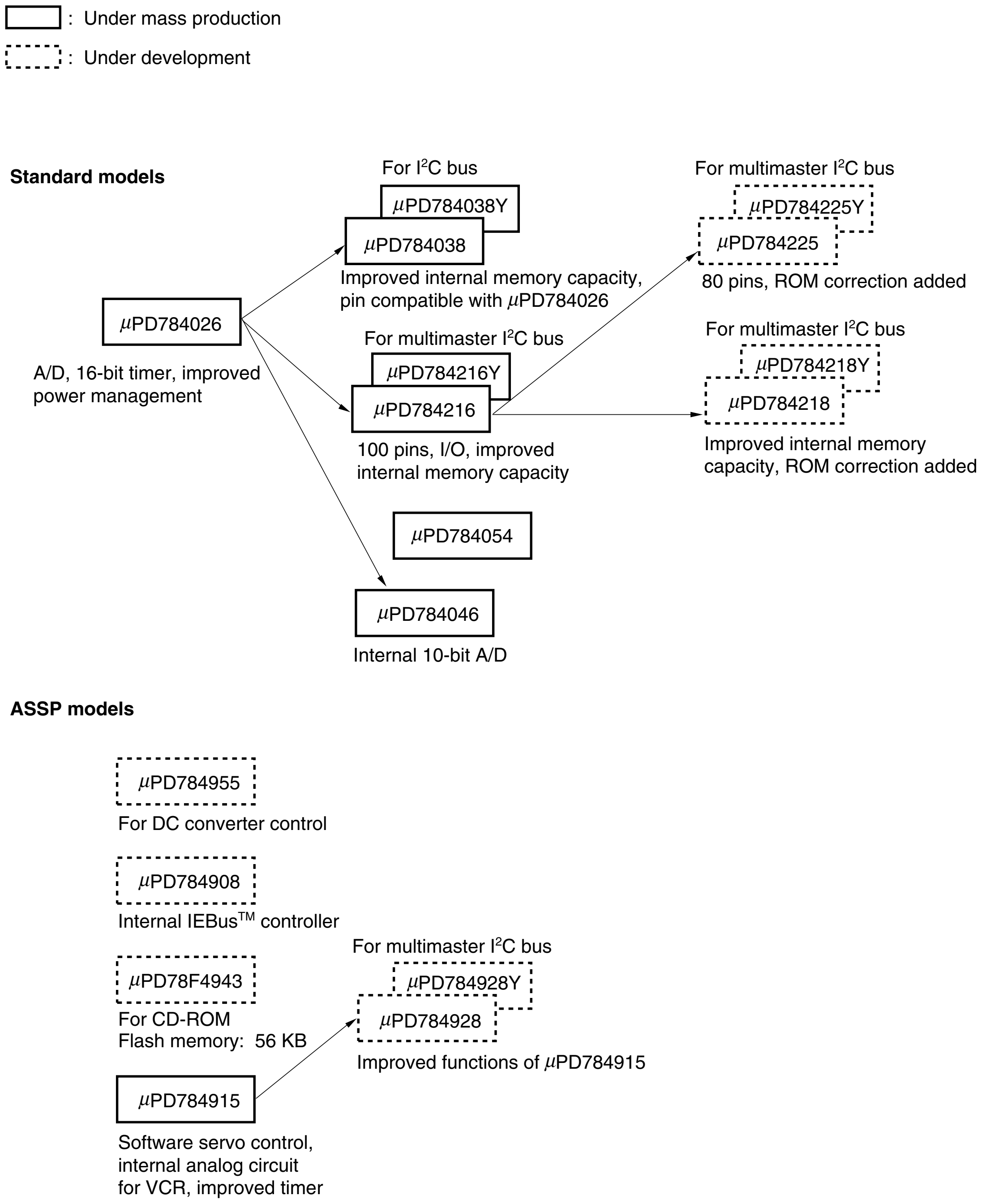
Item \ Part Number	μPD784044, 784046, 78F4046	μPD784044(A), 784046(A)
Quality grade	Standard	Special
Operating ambient temperature (T_A)	–10 to +70 ˚C	–40 to +85 ˚C
Operating frequency	8 to 32 MHz	8 to 25 MHz
Minimum instruction execution time	125 ns (with 16-MHz internal clock)	160 ns (with 12.5-MHz internal clock)
DC characteristics	V_{DD} supply current differs.	
AC characteristics	Bus timing and serial operation differ.	
A/D converter characteristics	Conversion time and sampling time differ.	

Differences between μPD784046(A), 784046(A1) and 784046(A2)

Item \ Part Number	μPD784046(A)	μPD784046(A1)	μPD784046(A2)
Operating ambient temperature (T_A)	–40 to +85 ˚C	–40 to +110 ˚C	–40 to +125 ˚C
Operating frequency	8 to 25 MHz	8 to 20 MHz	
Minimum instruction execution time	160 ns (with 12.5-MHz internal clock)	200 ns (with 10-MHz internal clock)	
DC characteristics	Analog pin input leakage current, V_{DD} supply current and data retention current differ.		
AC characteristics	Bus timing and serial operation differ.		
A/D converter characteristics	AV_{REF} current and A/D converter data retention current differ.		

Remark The differences between μPD784044(A), 784044(A1) and 784044(A2) is the same as above table.

Product Development of 78K/IV Series



FUNCTION LIST

Item / Product		μPD784044(A)	μPD784046(A)
Number of basic instructions (mnemonics)		113	
General-purpose register		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)	
Minimum instruction execution time		• 160 ns (with internal 12.5-MHz clock): μPD784044(A), 784046(A) • 200 ns (with internal 10-MHz clock) : μPD784044(A1), (A2), 784046(A1), (A2)	
Internal memory	ROM	32K bytes	64 K bytes
	RAM	1024 bytes	2048 bytes
Memory space		1M bytes with program/data combined	
I/O port	Total	65 pins	
	Input	17 pins	
	I/O	48 pins	
Pins with ancillary functions[Note]	Pins with pull-up resistors	29 pins	
Real-time output port		4 bits × 1	
Timer/counter		Timer 0 (16 bits) : Timer register × 1, capture/compare register × 4 Pulse output possible • Toggle output • Set/reset output	
		Timer 1 (16 bits) : Timer register × 1, compare register × 2 Pulse output possible • Toggle output • Set/reset output	
		Timer/counter 2 (16 bits) : Timer register × 1, compare register × 2 Pulse output possible • Toggle output • PWM/PPG output	
		Timer/counter 3 (16 bits) : Timer register × 1, compare register × 2 Pulse output possible • Toggle output • PWM/PPG output	
		Timer 4 (16 bits) : Timer register × 1, compare register × 2 Pulse output possible • Read-time output (4 bits × 1)	
A/D converter		10-bit resolution × 16 channels	
Serial interface		UART/IOE (3-wire serial I/O): 2 channels (with baud rate generator)	
Watchdog timer		1 channel	
Interrupt	Hardware source	27 (internal: 23, external: 8 (internal/external: 4))	
	Software source	BRK instruction, BRKCS instruction, operand error	
	Non-maskable	Internal: 1, external: 1	
	Maskable	Internal: 22, external: 7 (internal/external: 4)	
		• 4 levels of programmable priorities • 3 processing formats: vectored interrupt/macro service/context switching	
Bus sizing		8-bit/16-bit external data bus width selectable	
Standby		HALT/STOP/IDLE mode	
Supply voltage		V_{DD} = 4.5 to 5.5 V	
Package		80-pin plastic QFP (14 × 14 mm)	

Note The pins with ancillary functions are included in the I/O pins.

CONTENTS

1. DIFFERENCES BETWEEN μPD784044(A) AND 784046(A)

The only difference between the μPD784044(A) and μPD784046(A) is the internal memory capacity. The differences are shown in Table 1-1.

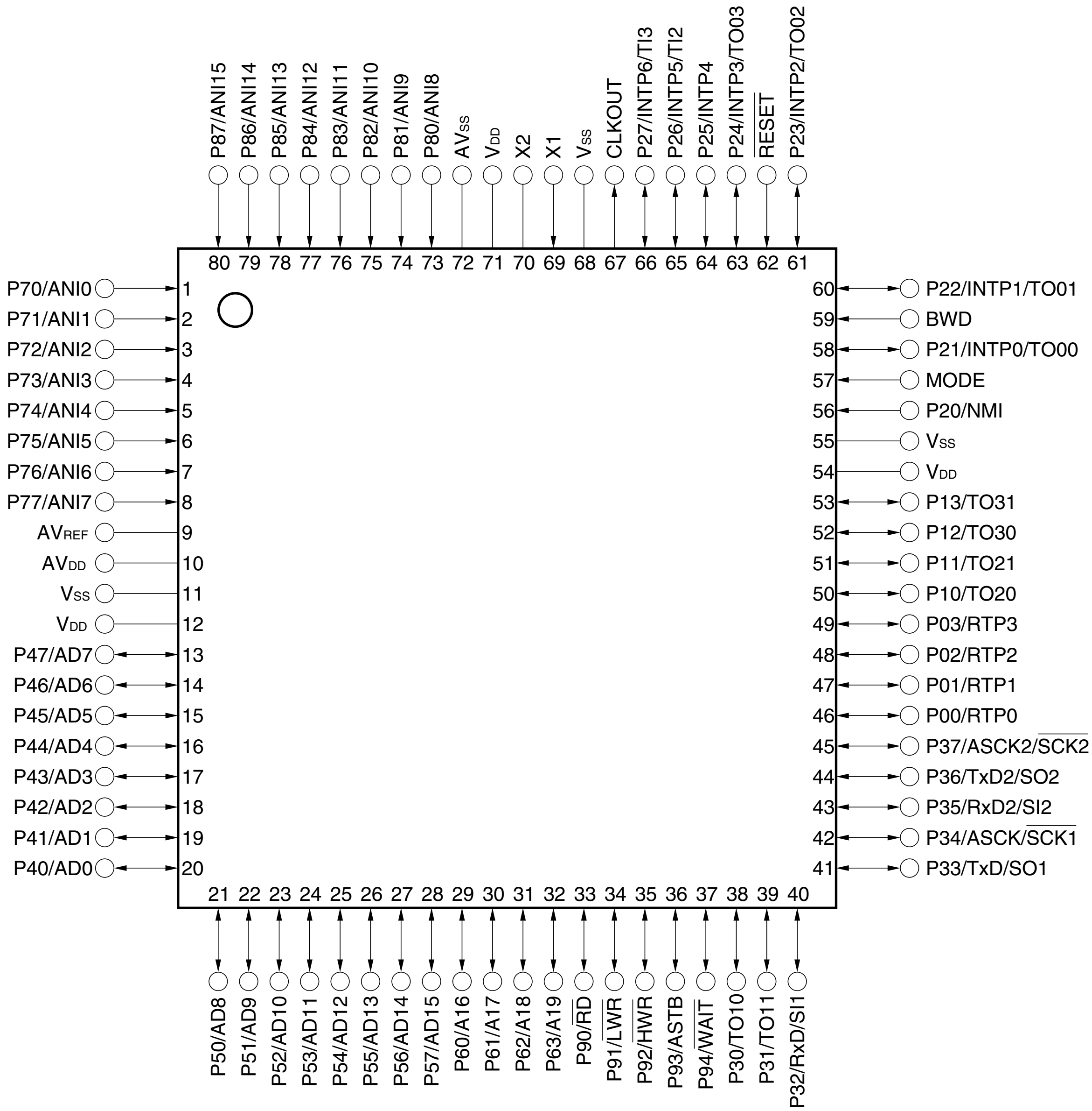
Table 1-1. Differences between μPD784044(A) and 784046(A)

Item \ Part Number	μPD784044(A)	μPD784046(A)
Internal ROM	32K bytes (mask ROM)	64K bytes (mask ROM)
Internal RAM	1024 bytes	2048 bytes

2. PIN CONFIGURATION (Top View)

- **80-pin plastic QFP (14 × 14 mm)**
  μPD784044GC(A)-×××-3B9, 784044GC(A1)-×××-3B9, 784044GC(A2)-×××-3B9
  μPD784046GC(A)-×××-3B9[Note], 784046GC(A1)-×××-3B9[Note], 784046GC(A2)-×××-3B9[Note]

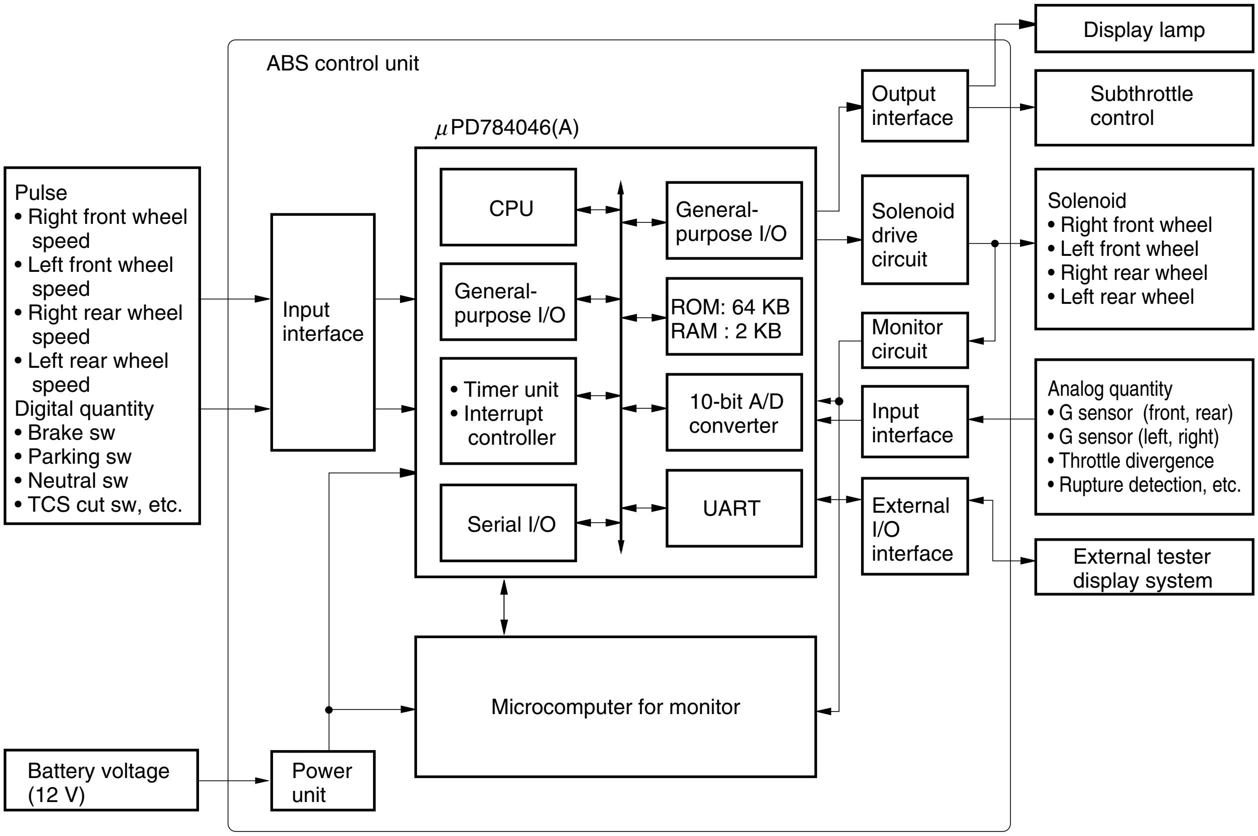
Note Under development



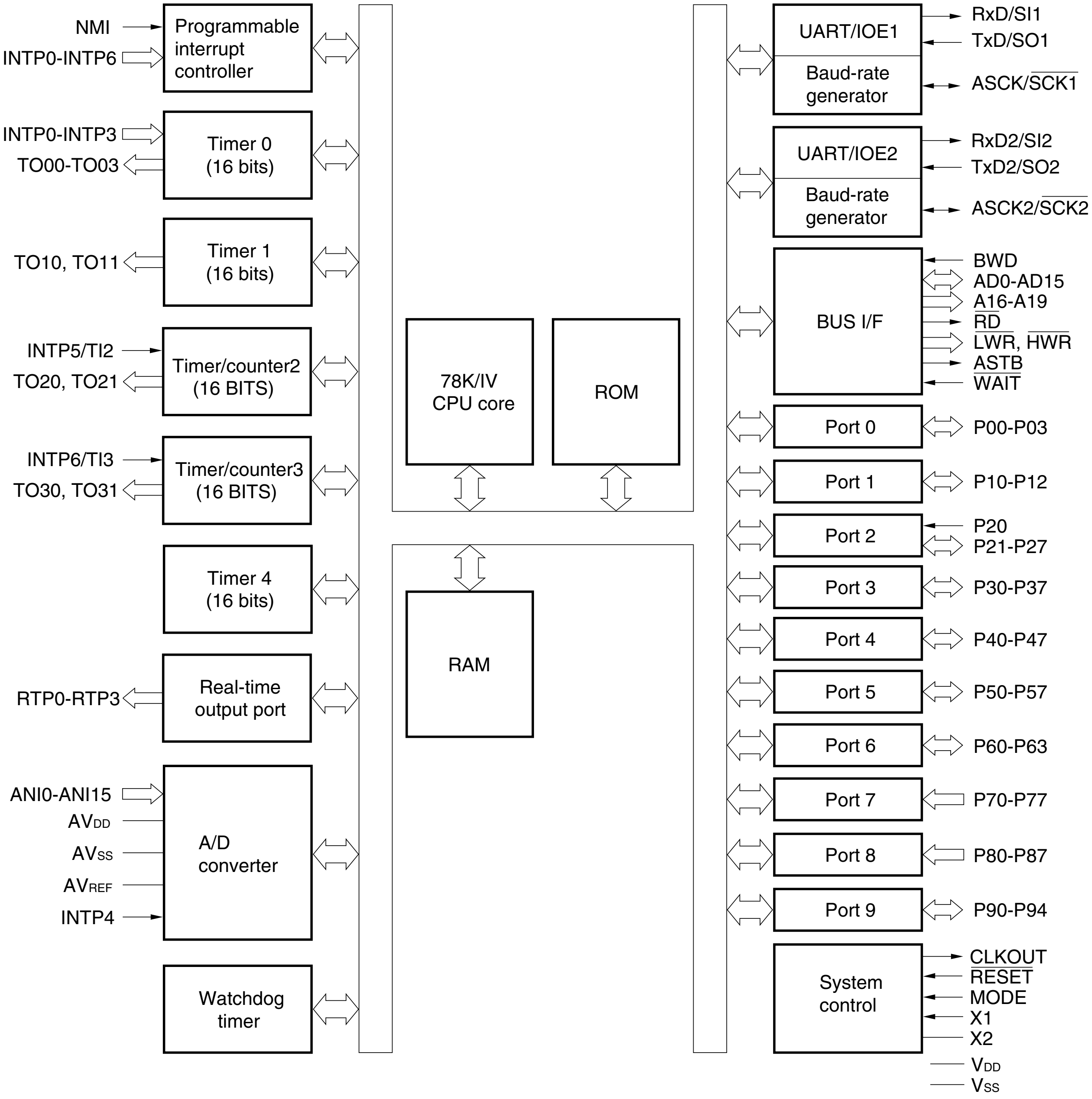
Caution Directly connect the MODE pin to V$_{SS}$.

A16-A19	: Address Bus
AD0-AD15	: Address/Data Bus
ANI0-ANI15	: Analog Input
ASCK, ASCK2	: Asynchronous Serial Clock
ASTB	: Address Strobe
AV_{DD}	: Analog Power Supply
AV_{REF}	: Analog Reference Voltage
AV_{SS}	: Analog Ground
BWD	: Bus Width Definition
CLKOUT	: Clock Out
$\overline{HWR}$	: High Address Write Strobe
INTP0-INTP6	: Interrupt from Peripherals
$\overline{LWR}$	: Low Address Write Strobe
MODE	: Mode
NMI	: Non-maskable Interrupt
P00-P03	: Port0
P10-P13	: Port1
P20-P27	: Port2
P30-P37	: Port3
P40-P47	: Port4
P50-P57	: Port5
P60-P63	: Port6
P70-P77	: Port7
P80-P87	: Port8
P90-P94	: Port9
$\overline{RD}$	: Read Strobe
$\overline{RESET}$	: Reset
RTP0-RTP3	: Real-Time Port
RxD, RxD2	: Receive Data
$\overline{SCK1}$,$\overline{SCK2}$	: Serial Clock
SI1, SI2	: Serial Input
SO1, SO2	: Serial Output
TI2, TI3	: Timer Input
TO00-TO03, TO10, TO11, TO20,TO21,TO30,TO31	: Timer Output
TxD, TxD2	: Transmit Data
V_{DD}	: Power Supply
V_{SS}	: Ground
$\overline{WAIT}$	: Wait
X1, X2	: Crystal

3. SYSTEM CONFIGURATION EXAMPLE (AC SERVO MOTOR CONTROL)



4. BLOCK DIAGRAM



Remark The internal ROM and RAM capacity differs depending on the products.

5. PIN FUNCTIONS

5.1 Port Pins (1/2)

Pin Name	I/O	Shared by:	Function	
P00-P03	I/O	RTP0-RTP3	Port 0 (P0): • 4-bit I/O port • Can be set in input/output mode bit-wise. • Pins in input mode can all be connected to pull-up resistors at once via software.	
P10	I/O	TO20	Port 1 (P1): • 4-bit I/O port • Can be set in input/output mode bit-wise.	
P11		TO21		
P12		TO30		
P13		TO31		
P20	Input	NMI	Port 2 (P2): • 8-bit I/O port	Input only
P21	I/O	INTP0/TO00		Can be set in input/output mode bit-wise.
P22		INTP1/TO01		
P23		INTP2/TO02		
P24		INTP3/TO03		
P25		INTP4		
P26		INTP5/TI2		
P27		INTP6/TI3		
P30	I/O	TO10	Port 3 (P3): • 8-bit I/O port • Can be set in input/output mode bit-wise.	
P31		TO11		
P32		RxD/SI1		
P33		TxD/SO1		
P34		ASCK/$\overline{\text{SCK1}}$		
P35		RxD2/SI2		
P36		TxD2/SO2		
P37		ASCK2/$\overline{\text{SCK2}}$		
P40-P47	I/O	AD0-AD7	Port 4 (P4): • 8-bit I/O port • Can be set in input/output mode bit-wise. • Pins in input mode can all be connected to pull-up resistors at once via software.	
P50-P57	I/O	AD8-AD15	Port 5 (P5): • 8-bit I/O port • Can be set in input/output mode bit-wise. • Pins in input mode can all be connected to pull-up resistors at once via software.	
P60-P63	I/O	A16-A19	Port 6 (P6): • 4-bit I/O port • Can be set in input/output mode bit-wise. • Pins in input mode can all be connected to pull-up resistors at once via software.	

5.1 Port Pins (2/2)

Pin Name	I/O	Shared by:	Function
P70-P77	Input	ANI0-ANI7	Port 7 (P7): • 8-bit input port
P80-P87	Input	ANI8-ANI15	Port 8 (P8): • 8-bit input port
P90	I/O	$\overline{\text{RD}}$	Port 9 (P9): • 5-bit I/O port • Can be set in input/output mode bit-wise. • Pins in input mode can all be connected to pull-up resistors at once via software.
P91		$\overline{\text{LWR}}$	
P92		$\overline{\text{HWR}}$	
P93		ASTB	
P94		$\overline{\text{WAIT}}$	

5.2 Pins Other Than Port Pins (1/2)

Pin Name	I/O	Shared by:	Function	
RTP0-RTP3	Output	P00-P03	Real-time output	
NMI	Input	P20	Non-maskable interrupt request input	
INTP0		P21/TO00	External interrupt request input	Capture trigger signal of CC00
INTP1		P22/TO01		Capture trigger signal of CC01
INTP2		P23/TO02		Capture trigger signal of CC02
INTP3		P24/TO03		Capture trigger signal of CC03
INTP4		P25		Conversion start trigger input of A/D converter
INTP5		P26/TI2		–
INTP6		P27/TI3		
TO00	Output	P21/INTP0	Timer output from timer/counter	
TO01		P22/INTP1		
TO02		P23/INTP2		
TO03		P24/INTP3		
TO10		P30		
TO11		P31		
TO20		P10		
TO21		P11		
TO30		P12		
TO31		P13		
TI2	Input	P26/INTP5	External count clock input to timer/counter 2	
TI3		P27/INTP6	External count clock input to timer/counter 3	
RxD	Input	P32/SI1	Serial data input (UART0)	
RxD2		P35/SI2	Serial data input (UART2)	
TxD	Output	P33/SO1	Serial data output (UART0)	
TxD2		P36/SO2	Serial data output (UART2)	
ASCK	Input	P34/$\overline{\text{SCK1}}$	Baud rate clock input (UART0)	
ASCK2		P37/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)	
SI1	Input	P32/RxD	Serial data input (3-wire serial I/O1)	
SI2		P35/RxD2	Serial data input (3-wire serial I/O2)	
SO1	Output	P33/TxD	Serial data output (3-wire serial I/O1)	
SO2		P36/TxD2	Serial data output (3-wire serial I/O2)	
$\overline{\text{SCK1}}$	I/O	P34/ASCK	Serial clock input/output (3-wire serial I/O1)	
$\overline{\text{SCK2}}$		P37/ASCK2	Serial clock input/output (3-wire serial I/O2)	
AD0-AD7	I/O	P40-P47	Lower multiplexed address/data bus when external memory is connected	
AD8-AD15^{Note}	I/O	P50-P57	• When 8-bit bus is specified Higher address bus when external memory is connected • When external 16-bit bus is specified Higher multiplexed address/data bus when external memory is connected	
A16-A19^{Note}	Output	P60-P63	Higher address bus when external memory is connected	
$\overline{\text{RD}}$	Output	P90	Read strobe to external memory	

Note The number of pins used as address bus pins differs depending on the external address space (refer to **9. LOCAL BUS INTERFACE**).

5.2 Pins Other Than Port Pins (2/2)

Pin Name	I/O	Shared by:	Function
$\overline{\text{LWR}}$	Output	P91	• When external 8-bit bus is specified Write strobe to external memory • When external 16-bit bus is specified Write strobe to external memory located at lower position
$\overline{\text{HWR}}$		P92	Write strobe to external memory located at higher position when external 16-bit bus is specified
ASTB	Output	P93	Timing signal output to externally latch address information output from AD0 through AD15 pins to access external memory
$\overline{\text{WAIT}}$	Input	P94	Inserts wait.
BWD	Input	–	Sets bus width.
MODE	Input	–	Directly connect this pin to V_{SS} (this pin specifies test mode of IC).
CLKOUT	Output	–	Clock output. Outputs low level during IDLE mode and STOP mode. Otherwise, always outputs f_{XX} (oscillation frequency).
X1	Input	–	Connect crystal for system clock oscillation (clock can be also input to X1).
X2	–	–	
$\overline{\text{RESET}}$	Input	–	Chip reset
ANI0-ANI7	Input	P70-P77	Analog voltage input for A/D converter
ANI8-ANI15		P80-P87	
AV_{REF}	–	–	Reference voltage for A/D converter
AV_{DD}		–	Positive power supply for A/D converter
AV_{SS}		–	GND for A/D converter
V_{DD}		–	Positive power supply
V_{SS}		–	GND

5.3 I/O Circuits of Pins and Processing of Unused Pins

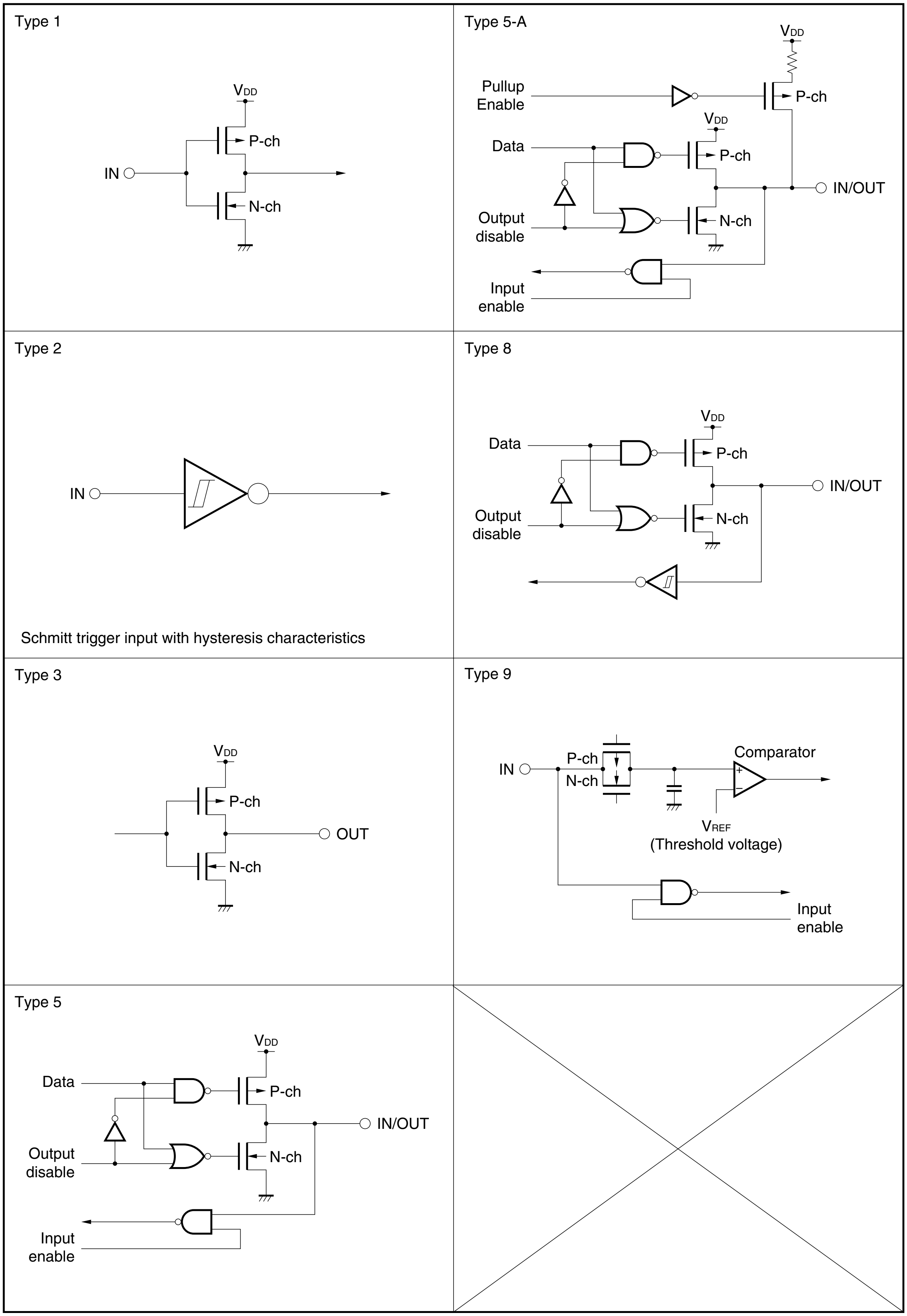
Table 5-1 shows the I/O circuit type of each pin and recommended processing of the unused pins.
For the I/O circuit type, refer to **Figure 5-1**.

Table 5-1. I/O Circuit Type of Each Pin and Recommended Processing of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/RTP0-P03/RTP3	5-A	I/O	Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave unconnected.
P10-P12	5		
P11/TO21			
P12/TO30			
P13/TO31			
P20/NMI	2	Input	Connect to V_{SS}.
P21/INTP0/TO00	8	I/O	Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave unconnected.
P22/INTP1/TO01			
P23/INTP2/TO02			
P24/INTP3/TO03			
P25/INTP4			
P26/INTP5/TI2			
P27/INTP6/TI3			
P30/TO10	5		
P31/TO11			
P32/RxD/SI1			
P33/TxD/SO1			
P34/ASCK/$\overline{\text{SCK1}}$	8		
P35/RxD2/SI2	5		
P36/TxD2/SO2			
P37/ASCK2/$\overline{\text{SCK2}}$	8		
P40/AD0-P47/AD7	5-A		
P50/AD8-P57/AD15			
P60/A16-P63/A19			
P70/ANI0-P77/ANI7	9	Input	Connect to V_{SS}.
P80/ANI8-P87/ANI15			
P90/$\overline{\text{RD}}$	5-A	I/O	Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave unconnected.
P91/$\overline{\text{LWR}}$			
P92/$\overline{\text{HWR}}$			
P93/ASTB			
P94/$\overline{\text{WAIT}}$			
MODE	1	Input	Directly connect to V_{SS}.
$\overline{\text{RESET}}$	2		–
CLKOUT	3	Output	Leave unconnected.
AV_{REF}	–	–	Connect to V_{SS}.
AV_{SS}			
AV_{DD}			Connect to V_{DD}.

Remark The circuit type numbers are serial in the 78K series but are not always so with some models (because some models are not provided with particular circuits).

Figure 5-1. I/O Circuits of Pins



Schmitt trigger input with hysteresis characteristics

6. CPU ARCHITECTURE

6.1 Memory Space

A 1M-byte memory space can be accessed. The mapping of the internal data area (special function registers and internal RAM) can be selected by using the LOCATION instruction. The LOCATION instruction must be always executed after the reset signal has been deasserted, and must not be used more than once.

(1) When LOCATION 0 instruction is executed

- **Internal memory**
  The internal data area and internal ROM area are as follows:

Product Name	Internal Data Area	Internal ROM Area
μPD784044(A)	0FB00H-0FFFFH	00000H-07FFFH
μPD784046(A)	0F700H-0FFFFH	00000H-0F5FFH

Caution 0F600H to 0FFFFH of the on-chip ROM (00000H to 0FFFFH) of the μPD784046(A) cannot be used as ROM in execution of the LOCATION 0 instruction (refer to Figure 6-2).

- **External memory**
  The external memory is accessed in the external memory expansion mode.

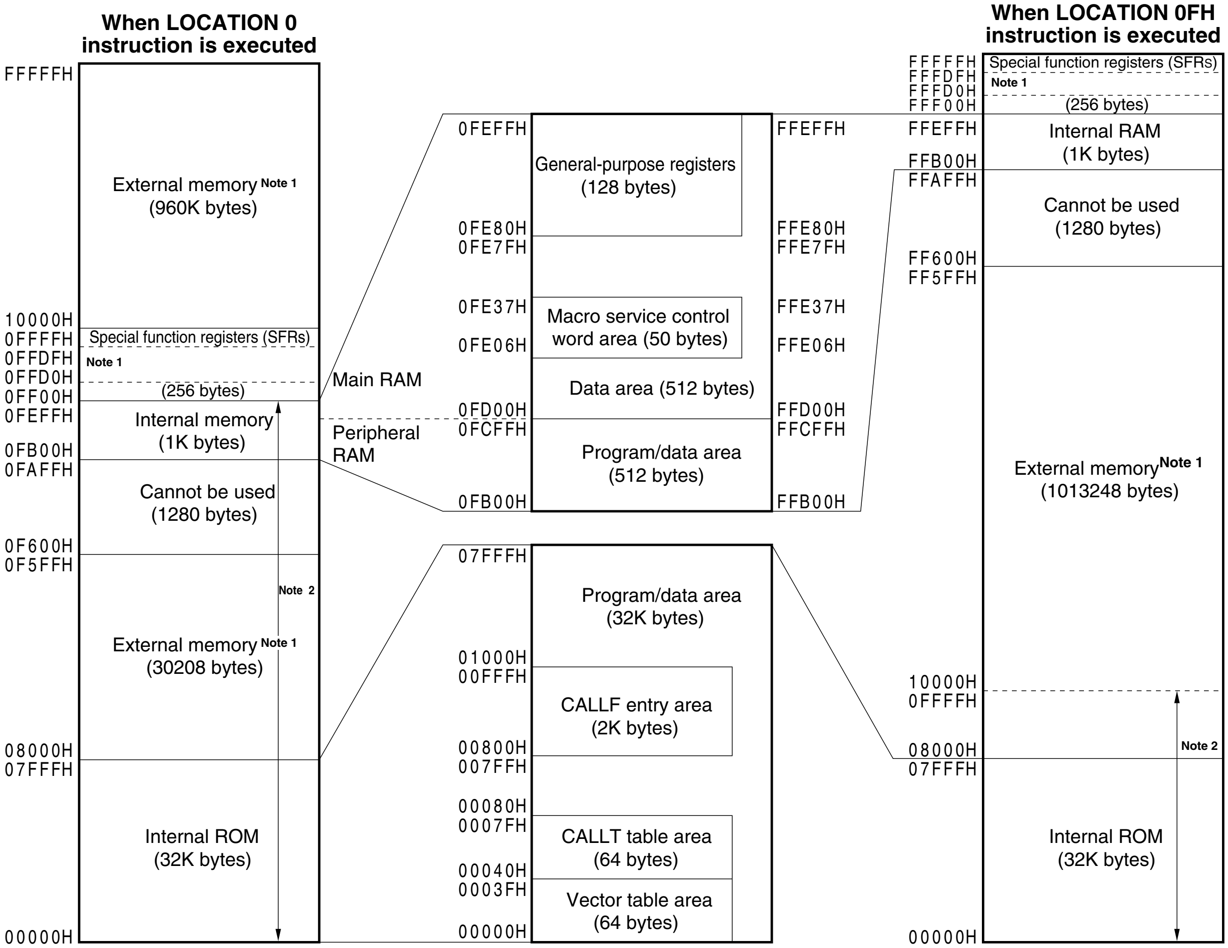
(2) When LOCATION 0FH instruction is executed

- **Internal memory**
  The internal data area and internal ROM area are as follows:

Product Name	Internal Data Area	Internal ROM Area
μPD784044(A)	FFB00H-FFFFFH	00000H-07FFFH
μPD784046(A)	FF700H-FFFFFH	00000H-0FFFFH

- **External memory**
  The external memory is accessed in the external memory expansion mode.

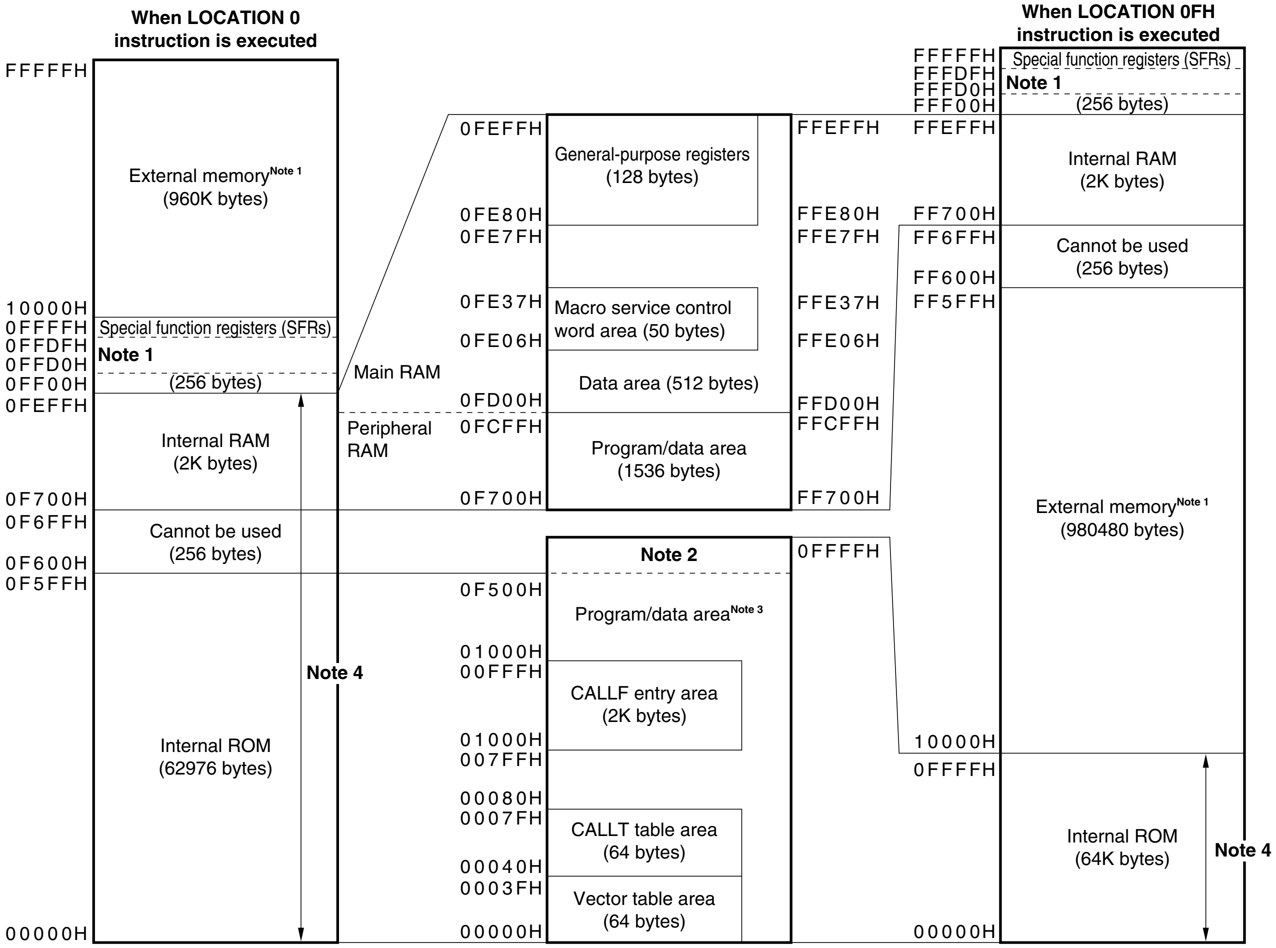
Figure 6-1. μPD784044(A) Memory Map



Notes 1. Accessed in the external memory expansion mode.

2. Base area or entry area by reset or interrupt. The internal RAM is not reset.

Figure 6-2. μPD784046(A) Memory Map



Notes 1. Accessed in the external memory expansion mode.

2. 2560 bytes in this area can be used as inernal ROM only when the LOCATION 0FH instruction is executed.

3. When the LOCATION 0 instruction is executed: 62976 bytes
When the LOCATION 0FH instruction is executed: 65536 bytes

4. Base area or entry area by reset or interrupt. The internal RAM is not reset.

6.2 CPU Registers

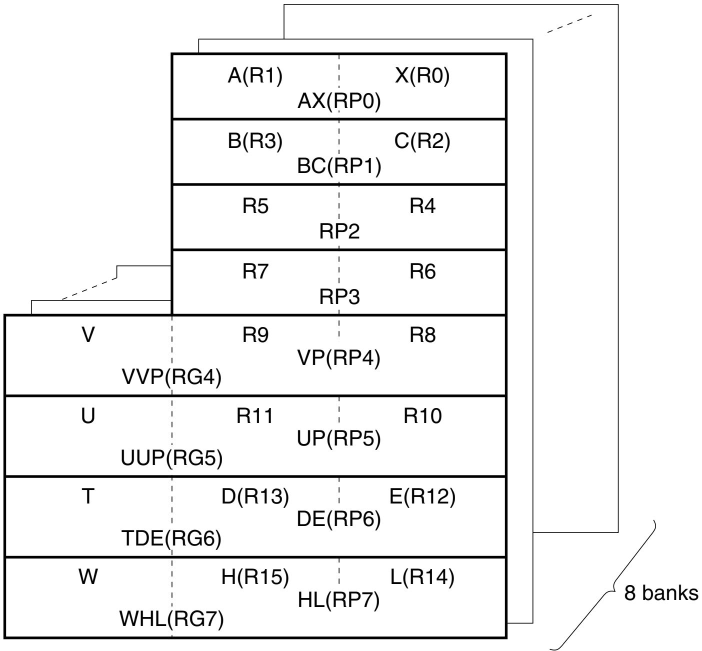
6.2.1 General-purpose registers

Sixteen 8-bit general-purpose registers are provided. Two 8-bit general-purpose registers can be used in pairs as a 16-bit general-purpose register. Of the 16-bit registers, four can be used with an 8-bit register for address expansion as 24-bit address specification registers.

Eight banks of register sets are available which can be selected by software or context switching function.

The general-purpose registers except the V, U, T, and W registers for address expansion are mapped to the internal RAM.

Figure 6-3. General-Purpose Register Format



( ): absolute name

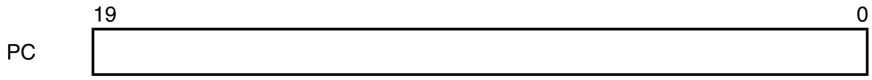
Caution **R4, R5, R6, R7, RP2, and RP3 can be used as X, A, C, B, AX, and BC registers, respectively, by setting the RSS bit of the PSW to 1. However, use this function only when using a 78K/III series program.**

6.2.2 Control registers

(1) Program counter (PC)

This is a 20-bit program counter. Its contents are automatically updated as the program is executed.

Figure 6-4. Program Counter (PC) Format



(2) Program status word (PSW)

This register retains the status of the CPU and its contents are automatically updated as the program is executed.

Figure 6-5. Program Status Word (PSW) Format

PSW								
	15	14	13	12	11	10	9	8
PSWH	UF	RBS2	RBS1	RBS0	—	—	—	—
	7	6	5	4	3	2	1	0
PSWL	S	Z	RSS[Note]	AC	IE	P/V	0	CY

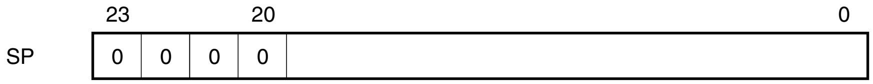
Note This flag is provided so that the μPD784046(A) maintains compatibility with the 78K/III series. Be sure to clear this flag to 0 when using 78K/III series software.

(3) Stack pointer (SP)

This is a 24-bit pointer that holds the first address of the stack.

Be sure to write 0 to the high-order 4 bits of this pointer.

Figure 6-6. Stack Pointer (SP) Format



6.2.3 Special function registers (SFRs)

The special function registers are registers to which special functions are assigned, and include the mode registers and control registers of the internal peripheral hardware. These registers are mapped to a 256-byte space of addresses 0FF00H through 0FFFFH^{Note}.

Note When the LOCATION 0 instruction is executed. FFF00H through FFFFFH when the LOCATION 0FH instruction is executed.

Caution Do not access an address in this area to which no SFR is allocated. If an address to which no SFR is allocated is accessed by mistake, the μPD784046(A) may be deadlocked. The deadlock status can be cleared only by inputting the reset signal.

Table 6-1 lists the special function registers. The meanings of the symbols in this table are as follows:

- Symbol .... Symbol indicating an SFR. These symbols are reserved for an NEC's assembler (RA78K4). With a C compiler (CC78K4), they can be used as sfr variables by using the #pragma sfr directive.
- R/W .... Indicates whether the corresponding SFR can be read/written.
  R/W : Read/write
  R : Read only
  W : Write only
- Bit units for manipulation .... Indicates bit units in which the corresponding SFR can be manipulated.
  SFRs that can be manipulated in 16-bit units can be written as operand sfrp. Specify the even addresses of these SFRs when specifying an address.
  SFRs that can be manipulated bit-wise can be written in bit manipulation instructions.
- On reset .... Indicates the status of each register when the $\overline{\text{RESET}}$ signal is input.

Table 6-1. Special Function Register List (1/5)

Address[Note 1]	Special Function Register (SFR) Name	Symbol	R/W	Bit units for manipulation			On reset
				1 bit	8 bits	16 bits	
0FF00H	Port 0	P0	R/W	○	○	–	Undefined
0FF01H	Port 1	P1		○	○	–	
0FF02H	Port 2	P2	Note 2	○	○	–	
0FF03H	Port 3	P3	R/W	○	○	–	
0FF04H	Port 4	P4		○	○	–	
0FF05H	Port 5	P5		○	○	–	
0FF06H	Port 6	P6		○	○	–	
0FF07H	Port 7	P7	R	○	○	–	
0FF08H	Port 8	P8		○	○	–	
0FF09H	Port 9	P9	R/W	○	○	–	
0FF0EH	Port 0 buffer register	P0L		○	○	–	
0FF10H	Timer register 0	TM0	R	–	–	○	0000H
0FF11H							
0FF12H	Capture/compare register 00	CC00	R/W	–	–	○	Undefined
0FF13H							
0FF14H	Capture/compare register 01	CC01		–	–	○	
0FF15H							
0FF16H	Capture/compare register 02	CC02		–	–	○	
0FF17H							
0FF18H	Capture/compare register 03	CC03		–	–	○	
0FF19H							
0FF1AH	Timer register 1	TM1	R	–	–	○	0000H
0FF1BH							
0FF1CH	Compare register 10	CM10	R/W	–	–	○	Undefined
0FF1DH							
0FF1EH	Compare register 11	CM11		–	–	○	
0FF1FH							
0FF20H	Port 0 mode register	PM0		○	○	–	FFH
0FF21H	Port 1 mode register	PM1		○	○	–	
0FF22H	Port 2 mode register	PM2[Note 3]		○	○	–	
0FF23H	Port 3 mode register	PM3		○	○	–	
0FF24H	Port 4 mode register	PM4		○	○	–	
0FF25H	Port 5 mode register	PM5		○	○	–	
0FF26H	Port 6 mode register	PM6		○	○	–	
0FF29H	Port 9 mode register	PM9		○	○	–	
0FF2EH	Real-time output port control register	RTPC		○	○	–	00H
0FF2FH	Port read control register	PRDC		○	○	–	

Notes 1. When the LOCATION 0 instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

2. Bit 0 of P2 can only be read. Bit 1 can be read/written.

3. Bit 0 of PM2 is fixed to “1” by hardware.

Table 6-1. Special Function Register List (2/5)

Address[Note 1]	Special Function Register (SFR) Name	Symbol	R/W	Bit units for manipulation			On reset
				1 bit	8 bits	16 bits	
0FF30H	Timer unit mode register 0	TUM0	R/W	○	○	–	00H
0FF31H	Timer mode control register	TMC		○	○	–	
0FF32H	Timer output control register 0	TOC0		○	○	–	
0FF33H	Timer output control register 1	TOC1		○	○	–	
0FF34H	Timer unit mode register 2	TUM2		○	○	–	
0FF35H	Timer mode control register 2	TMC2		○	○	–	
0FF36H	Timer output control register 2	TOC2		○	○	–	
0FF37H	Timer mode control register 4	TMC4		○	○	–	
0FF38H	Prescaler mode register	PRM		–	○	–	
0FF39H	Prescaler mode register 2	PRM2		–	○	–	
0FF3AH	Prescaler mode register 4	PRM4		–	○	–	
0FF3BH	Noise protection control register	NPC		○	○	–	
0FF3CH	External interrupt mode register 0	INTM0		○	○	–	
0FF3DH	External interrupt mode register 1	INTM1		○	○	–	
0FF3EH	Interrupt valid edge flag register 1	IEF1		○	○	–	Undefined
0FF3FH	Interrupt valid edge flag register 2	IEF2		○	○	–	
0FF41H	Port 1 mode control register	PMC1		○	○	–	00H
0FF42H	Port 2 mode control register	PMC2[Note 2]		○	○	–	
0FF43H	Port 3 mode control register	PMC3		○	○	–	
0FF49H	Port 9 mode control register	PMC9		○	○	–	
0FF4EH	Pull-up resistor option register L	PUOL		○	○	–	
0FF4FH	Pull-up resistor option register H	PUOH		○	○	–	
0FF50H	Timer register 2	TM2	R	–	–	○	0000H
0FF51H							
0FF52H	Compare register 20	CM20	R/W	–	–	○	Undefined
0FF53H							
0FF54H	Compare register 21	CM21		–	–	○	
0FF55H							
0FF56H	Timer register 3	TM3	R	–	–	○	0000H
0FF57H							
0FF58H	Compare register 30	CM30	R/W	–	–	○	Undefined
0FF59H							
0FF5AH	Compare register 31	CM31		–	–	○	
0FF5BH							
0FF60H	Timer register 4	TM4	R	–	–	○	0000H
0FF61H							

Notes 1. When the LOCATION 0 instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

2. Bits 0, and 5 through 7 of PMC2 are fixed to “0” by hardware.

Table 6-1. Special Function Register List (3/5)

Address[Note]	Special Function Register (SFR) Name	Symbol	R/W	Bit units for manipulation			On reset
				1 bit	8 bits	16 bits	
0FF62H	Compare register 40	CM40	R/W	–	–	○	Undefined
0FF63H							
0FF64H	Compare register 41	CM41		–	–	○	
0FF65H							
0FF6EH	A/D converter mode register	ADM		○	○	–	00H
0FF70H	A/D conversion result register 0	ADCR0	R	–	–	○	Undefined
0FF71H							
0FF71H	A/D conversion result register 0H	ADCR0H		–	○	–	
0FF72H	A/D conversion result register 1	ADCR1		–	–	○	
0FF73H							
0FF73H	A/D conversion result register 1H	ADCR1H		–	○	–	
0FF74H	A/D conversion result register 2	ADCR2		–	–	○	
0FF75H							
0FF75H	A/D conversion result register 2H	ADCR2H		–	○	–	
0FF76H	A/D conversion result register 3	ADCR3		–	–	○	
0FF77H							
0FF77H	A/D conversion result register 3H	ADCR3H		–	○	–	
0FF78H	A/D conversion result register 4	ADCR4		–	–	○	
0FF79H							
0FF79H	A/D conversion result register 4H	ADCR4H		–	○	–	
0FF7AH	A/D conversion result register 5	ADCR5		–	–	○	Undefined
0FF7BH							
0FF7BH	A/D conversion result register 5H	ADCR5H		–	○	–	
0FF7CH	A/D conversion result register 6	ADCR6		–	–	○	
0FF7DH							
0FF7DH	A/D conversion result register 6H	ADCR6H		–	○	–	
0FF7EH	A/D conversion result register 7	ADCR7		–	–	○	
0FF7FH							
0FF7FH	A/D conversion result register 7H	ADCR7H		–	○	–	
0FF84H	Clocked serial interface mode register 1	CSIM1	R/W	○	○	–	00H
0FF85H	Clocked serial interface mode register 2	CSIM2		○	○	–	
0FF88H	Asynchronous serial interface mode register	ASIM		○	○	–	
0FF89H	Asynchronous serial interface mode register 2	ASIM2		○	○	–	
0FF8AH	Asynchronous serial interface status register	ASIS	R	○	○	–	
0FF8BH	Asynchronous serial interface status register 2	ASIS2		○	○	–	

Note When the LOCATION 0 instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

Table 6-1. Special Function Register List (4/5)

Address[Note 1]	Special Function Register (SFR) Name	Symbol	R/W	Bit units for manipulation			On reset
				1 bit	8 bits	16 bits	
0FF8CH	Serial receive buffer: UART0	RXB	R	–	○	–	Undefined
	Serial transmit shift register: UART0	TXS	W	–	○	–	
	Serial shift register: IOE1	SIO1	R/W	–	○	–	
0FF8DH	Serial receive buffer: UART2	RXB2	R	–	○	–	
	Serial transmit shift register: UART2	TXS2	W	–	○	–	
	Serial shift register: IOE2	SIO2	R/W	–	○	–	
0FF90H	Baud rate generator control register	BRGC		–	○	–	00H
0FF91H	Baud rate generator control register 2	BRGC2		–	○	–	
0FFA8H	In-service priority register	ISPR	R	○	○	–	
0FFAAH	Interrupt mode control register	IMC	R/W	○	○	–	80H
0FFACH	Interrupt mask register 0L	MK0L		○	○	–	FFH
0FFACH	Interrupt mask register 0	MK0		–	–	○	FFFFH
0FFADH							
0FFADH	Interrupt mask register 0H	MK0H		○	○	–	FFH
0FFAEH	Interrupt mask register 1L	MK1L		○	○	–	
0FFAEH	Interrupt mask register 1	MK1		–	–	○	FFFFH
0FFAFH							
0FFAFH	Interrupt mask register 1H	MK1H		○	○	–	FFH
0FFC0H	Standby control register[Note 2]	STBC		–	○	–	30H
0FFC2H	Watchdog timer mode register[Note 2]	WDM		–	○	–	00H
0FFC4H	Memory expansion mode register	MM		○	○	–	20H
0FFC7H	Programmable wait control register 1	PWC1		–	○	–	AAH
0FFC8H	Programmable wait control register 2	PWC2		–	–	○	AAAAH
0FFC9H							
0FFCAH	Bus width specification register	BW		–	–	○	**Note 3**
0FFCBH							
0FFCFH	Oscillation stabilization time specification register	OSTS		–	○	–	00H
0FFD0H- 0FFDFH	External SFR area	–		○	○	–	Undefined
0FFE0H	Interrupt control register (INTOV0)	OVIC0		○	○	–	43H
0FFE1H	Interrupt control register (INTOV1)	OVIC1		○	○	–	
0FFE2H	Interrupt control register (INTOV4)	OVIC4		○	○	–	
0FFE3H	Interrupt control register (INTP0)	PIC0		○	○	–	
0FFE4H	Interrupt control register (INTP1)	PIC1		○	○	–	
0FFE5H	Interrupt control register (INTP2)	PIC2		○	○	–	

Notes 1. When the LOCATION 0 instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

2. These registers can be written only by using dedicated instructions MOV STBC, #byte and MOV WDM, #byte, and cannot be written by any other instructions.

3. The value of this register on reset differs depending on the setting of the BWD pin.

BWD = 0: 0000H
BWD = 1: 00FFH

Table 6-1. Special Function Register List (5/5)

Address[Note]	Special Function Register (SFR) Name	Symbol	R/W	Bit units for manipulation			On reset
				1 bit	8 bits	16 bits	
0FFE6H	Interrupt control register (INTP3)	PIC3	R/W	○	○	–	43H
0FFE7H	Interrupt control register (INTP4)	PIC4		○	○	–	
0FFE8H	Interrupt control register (INTP5)	PIC5		○	○	–	
0FFE9H	Interrupt control register (INTP6)	PIC6		○	○	–	
0FFEAH	Interrupt control register (INTCM10)	CMIC10		○	○	–	
0FFEBH	Interrupt control register (INTCM11)	CMIC11		○	○	–	
0FFECH	Interrupt control register (INTCM20)	CMIC20		○	○	–	
0FFEDH	Interrupt control register (INTCM21)	CMIC21		○	○	–	
0FFEEH	Interrupt control register (INTCM30)	CMIC30		○	○	–	
0FFEFH	Interrupt control register (INTCM31)	CMIC31		○	○	–	
0FFF0H	Interrupt control register (INTCM40)	CMIC40		○	○	–	
0FFF1H	Interrupt control register (INTCM41)	CMIC41		○	○	–	
0FFF2H	Interrupt control register (INTSER)	SERIC		○	○	–	
0FFF3H	Interrupt control register (INTSR)	SRIC		○	○	–	
	Interrupt control register (INTCSI1)	CSIIC1		○	○	–	
0FFF4H	Interrupt control register (INTST)	STIC		○	○	–	
0FFF5H	Interrupt control register (INTSER2)	SERIC2		○	○	–	
0FFF6H	Interrupt control register (INTSR2)	SRIC2		○	○	–	
	Interrupt control register (INTCSI2)	CSIIC2		○	○	–	
0FFF7H	Interrupt control register (INTST2)	STIC2		○	○	–	
0FFF8H	Interrupt control register (INTAD)	ADIC		○	○	–	

Note When the LOCATION 0 instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

7. PERIPHERAL HARDWARE FUNCTIONS

7.1 Ports

The μPD784046(A) has the ports shown in Figure 7-1. These ports can be used for various control operations. The function of each port is shown in Table 7-1. Ports 0, 4 through 6, and 9 can be connected to an internal pull-up resistor via software when they are set in the input mode.

Figure 7-1. Port Configuration

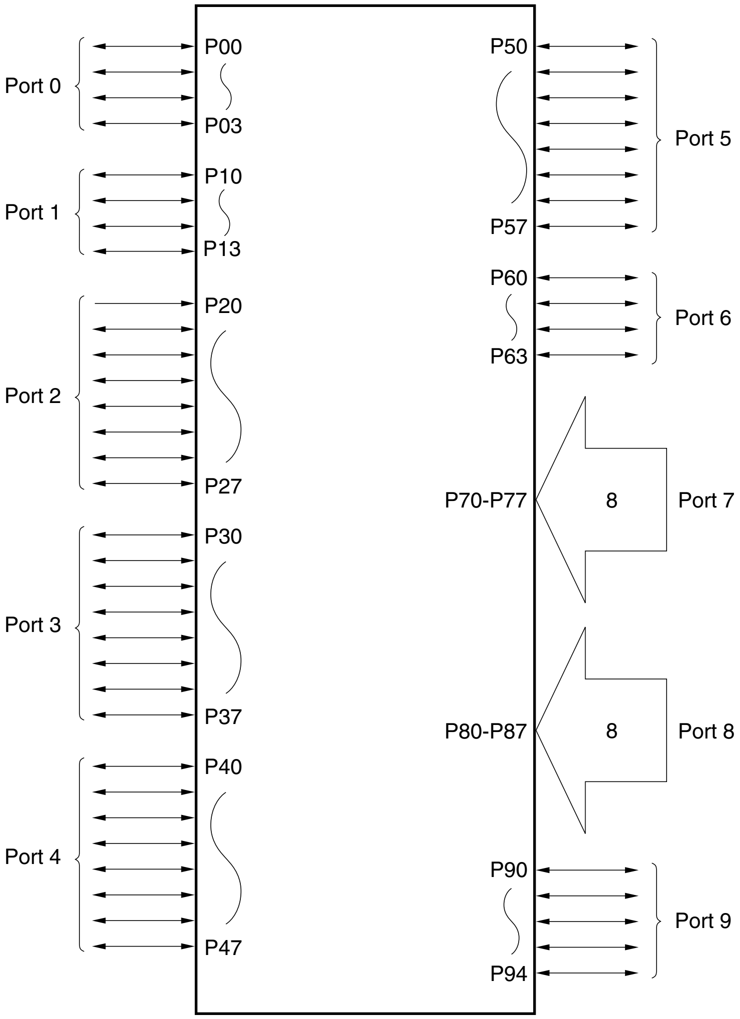


Table 7-1. Port Function

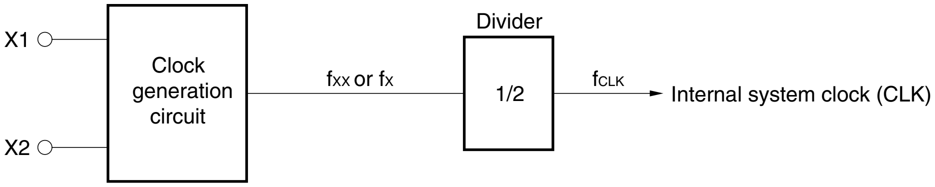
Port Name	Pin Name	Function	Specification of Pull-Up Resistor by Software
Port 0	P00-P03	Can be set in input or output mode bit-wise.	All pins in input mode
Port 1	P10-P13		–
Port 2	P20-P27	Can be set in input or output mode bit-wise (however, P20 is input-only).	
Port 3	P30-P37	Can be set in input or output mode bit-wise.	
Port 4	P40-P47		All pins in input mode
Port 5	P50-P57		
Port 6	P60-P63		
Port 7	P70-P77	Input port	–
Port 8	P80-P87		
Port 9	P90-P94	Can be set in input or output mode bit-wise.	All pins in input mode

7.2 Clock Generation Circuit

The clock generation circuit generates and controls the internal system clock (CLK) to be supplied to the CPU.

Figure 7-2 shows the configuration of this circuit.

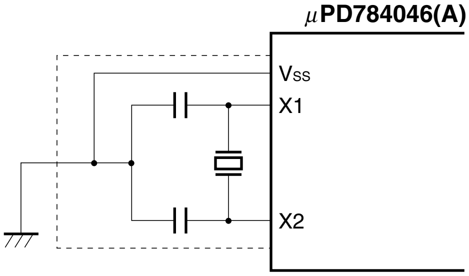
Figure 7-2. Block Diagram of Clock Generation Circuit



Remark f_{XX} : crystal/ceramic oscillation frequency
f_X : external clock frequency
f_{CLK} : internal system clock frequency

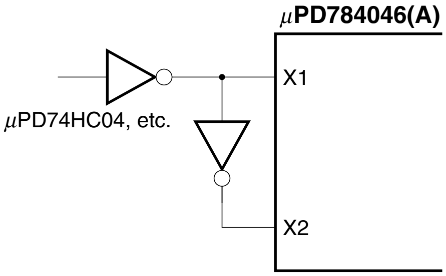
Figure 7-3. Example of Using Oscillation Circuit

(1) Crystal/ceramic oscillation

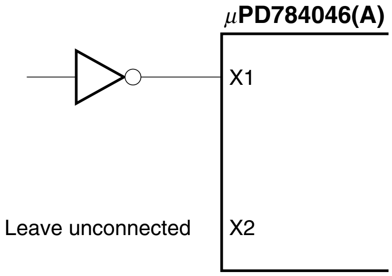


(2) External clock input

(a) EXTC bit of OSTS = 1



(b) EXTC bit of OSTS = 0



Caution When using the clock oscillation circuit, wire the portion enclosed by the dotted line in the above figure as follows to avoid adverse effects of wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

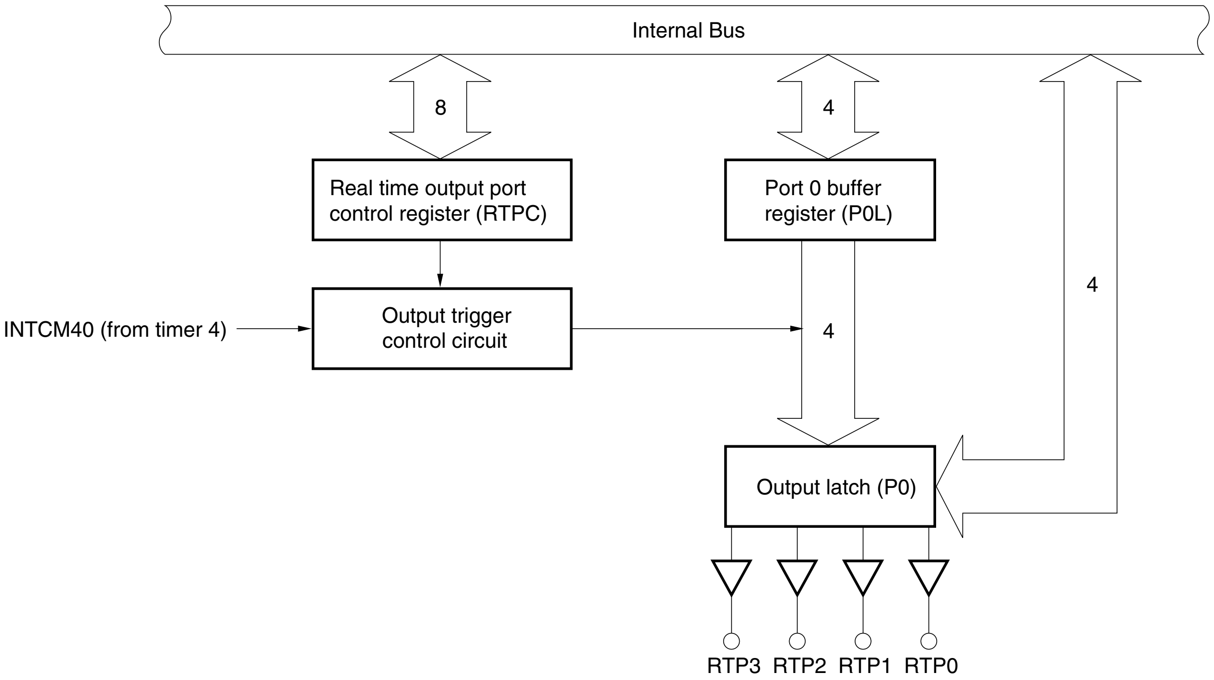
7.3 Real-Time Output Port

The real-time output port outputs the data stored in the buffer in synchronization with a match interrupt of timer 4. This allows jitter-less pulse output to be obtained.

Therefore, it is best suited to applications that output patterns at given intervals (such as stepping motor open loop control,etc.).

As shown in Figure 7-4, port 0 and the port 0 buffer register form the core of configuration.

Figure 7-4. Block Diagram of Real-Time Output Port



7.4 Timer/Counter

The μPD784046(A) contains two 16-bit timer/counter units and three 16-bit timer units.

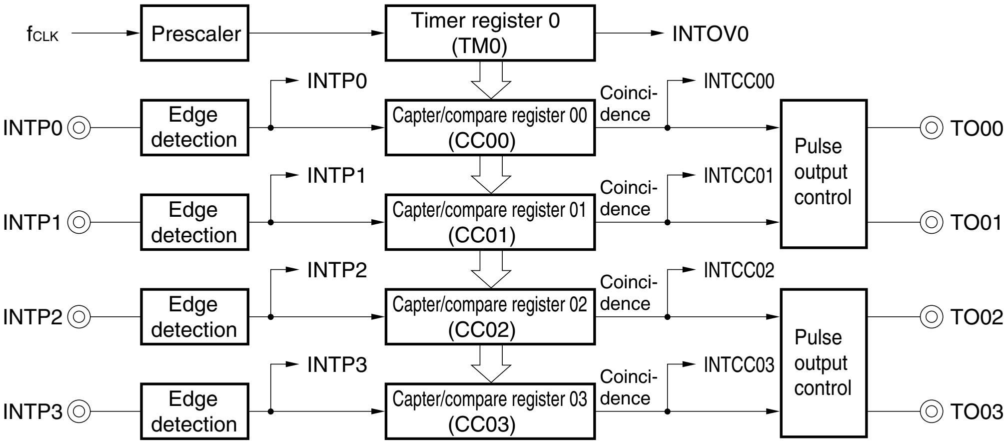
These units support a total of 15 interrupt requests, which enable them to function as 15-channel timers.

Table 7-2. Timer/Counter Function

Item \ Name			Timer 0	Timer 1	Timer/ Counter2	Timer/ Counter 3	Timer 4
Operating mode	Interval timer		4ch	2ch	2ch	2ch	2ch
	External event counter		–	–	○	○	–
Function	Timer output		4ch	2ch	2ch	2ch	–
		Toggle output	○	○	○	○	–
		Set/reset output	○	○	–	–	–
		PWM/PPG output	–	–	○	○	–
	Real-time output		–	–	–	–	○
	Overflow interrupt		○	○	–	–	○
	Number of interrupt requests		5	3	2	2	3

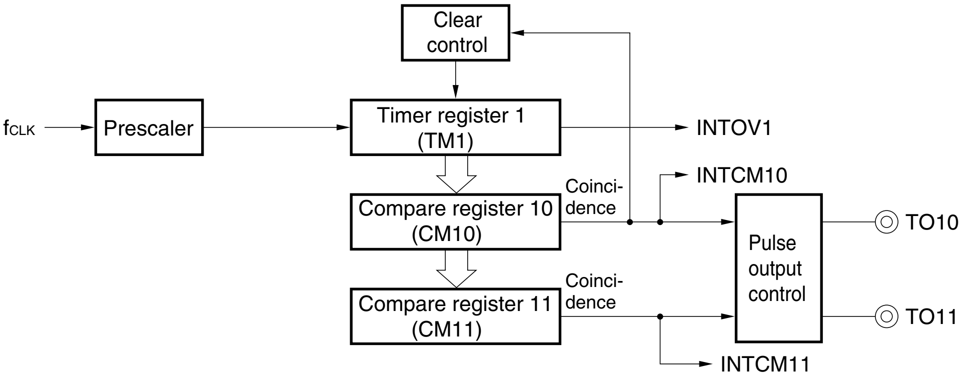
Figure 7-5. Block Diagram of Timer/Counter (1/2)

Timer 0



Prescaler: fCLK/4, fCLK/8, fCLK/16, fCLK/32, fCLK/64

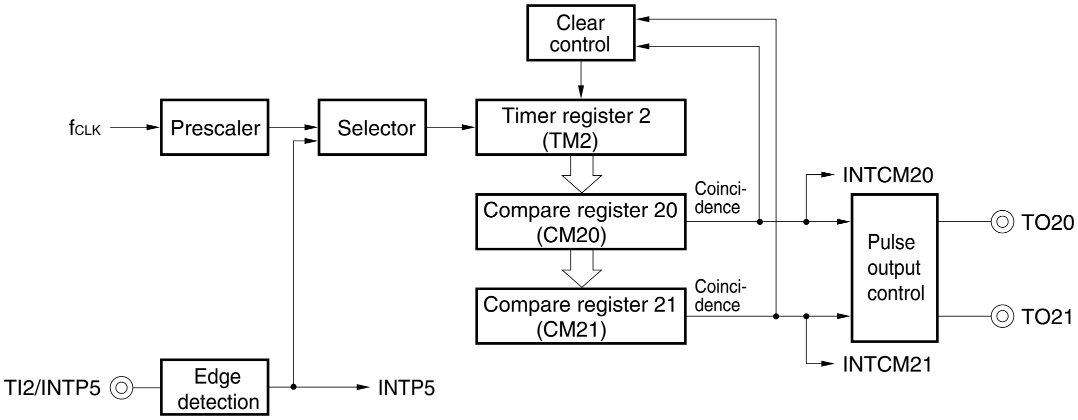
Timer 1



Prescaler: fCLK/8, fCLK/16, fCLK/32, fCLK/64, fCLK/128

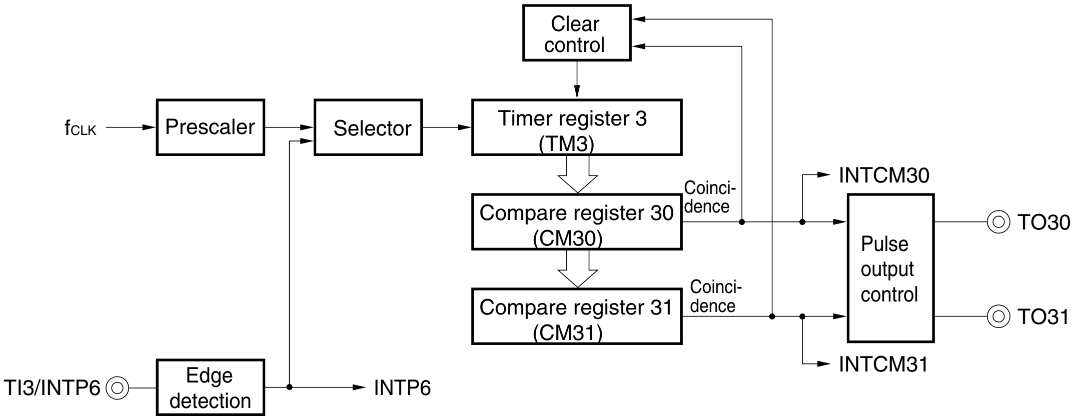
Figure 7-5. Block Diagram of Timer/Counter (2/2)

Timer/counter 2



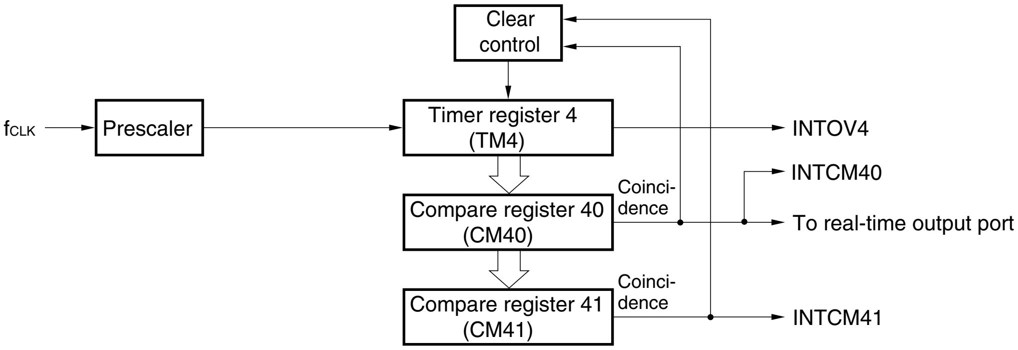
Prescaler: $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/16$, $f_{CLK}/32$, $f_{CLK}/64$

Timer/counter 3



Prescaler: $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/16$, $f_{CLK}/32$, $f_{CLK}/64$

Timer 4



Prescaler: $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/16$, $f_{CLK}/32$, $f_{CLK}/64$

7.5 A/D Converter

The μPD784046(A) has an analog-to-digital (A/D) converter with 16 multiplexed analog input pins (ANI0 through ANI15).

This converter is of successive approximation type. The result of conversion is stored to and retained in 10-bit A/D conversion result registers (ADCR0-ADCR7). Therefore, high-speed, high-accuracy conversion can be performed (conversion time: about 13.5 μs: f_{CLK} = 12.5 MHz).

The A/D conversion operation can be started in the following modes:

- Hardware start : Conversion is started by trigger input (INTP4).
- Software start : Conversion is started by setting a bit of the A/D converter mode register (ADM).

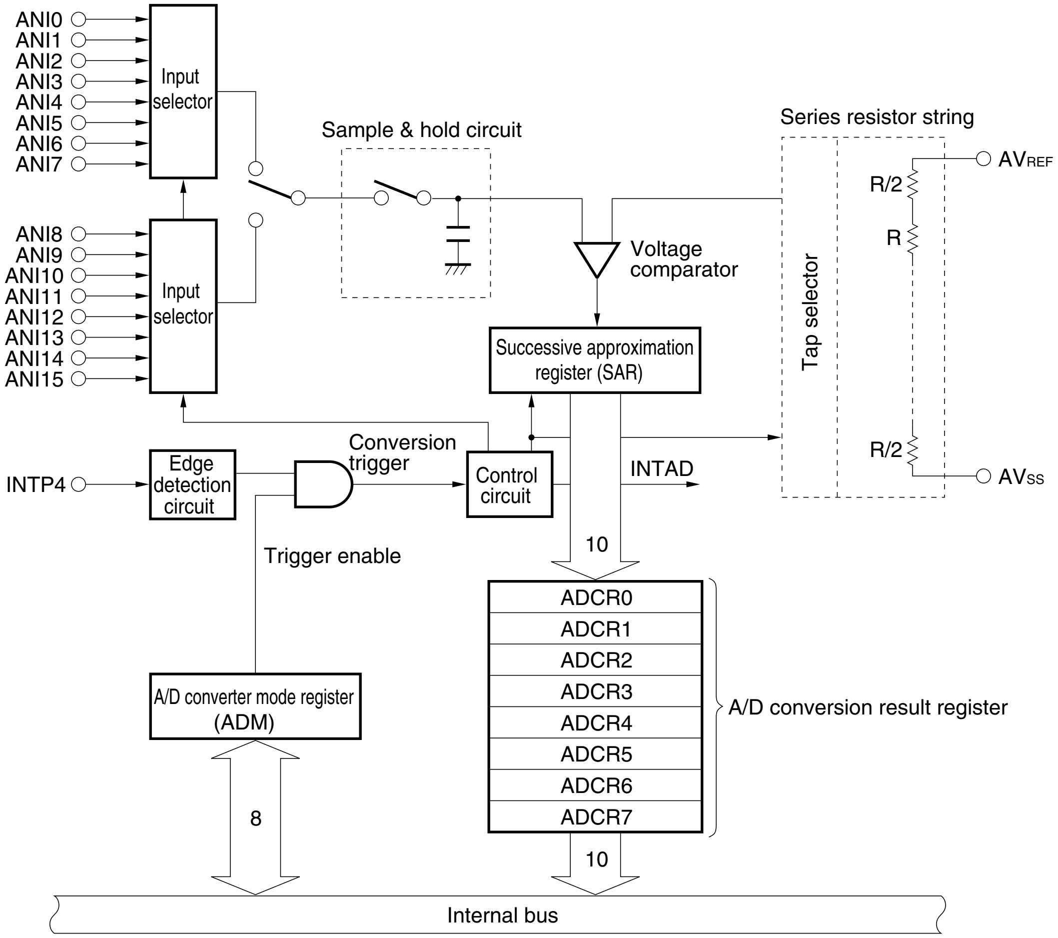
The A/D converter operates in the following modes:

- Scan mode : Sequentially selects two or more analog input pins to obtain data to be converted from all the pins.
- Select mode : Selects only one analog input pin to obtain successive conversion values.

The above modes and stopping the conversion are specified by ADM.

When the result of conversion is transferred to ADCRn (n = 0-7), interrupt request INTAD is generated. By using this interrupt request and by using macro service, the converted value can be successively transferred to memory.

Figure 7-6. Block Diagram of A/D Converter



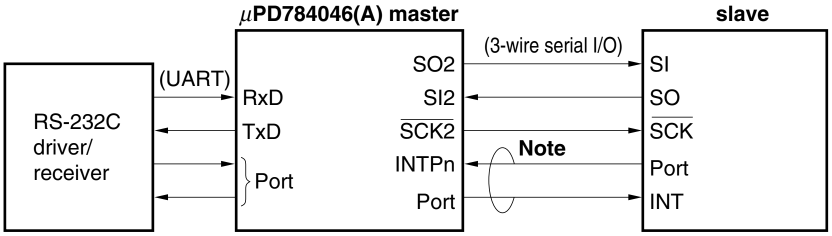
7.6 Serial Interface

The μPD784046(A) is provided with two independent serial interface channels.

- Asynchronous serial interface (UART)/3-wire serial I/O (IOE) × 2

By using these serial interface channels, communication with an external device and local communication within a system can be performed at the same time (refer to **Figure 7-7**).

Figure 7-7. Example of Serial Interface



Note Handshake line

7.6.1 Asynchronous serial interface/3-wire serial I/O (UART/IOE)

Two serial interface channels from which asynchronous serial interface mode and three-wire serial I/O mode can be selected are provided.

(1) Asynchronous serial interface mode

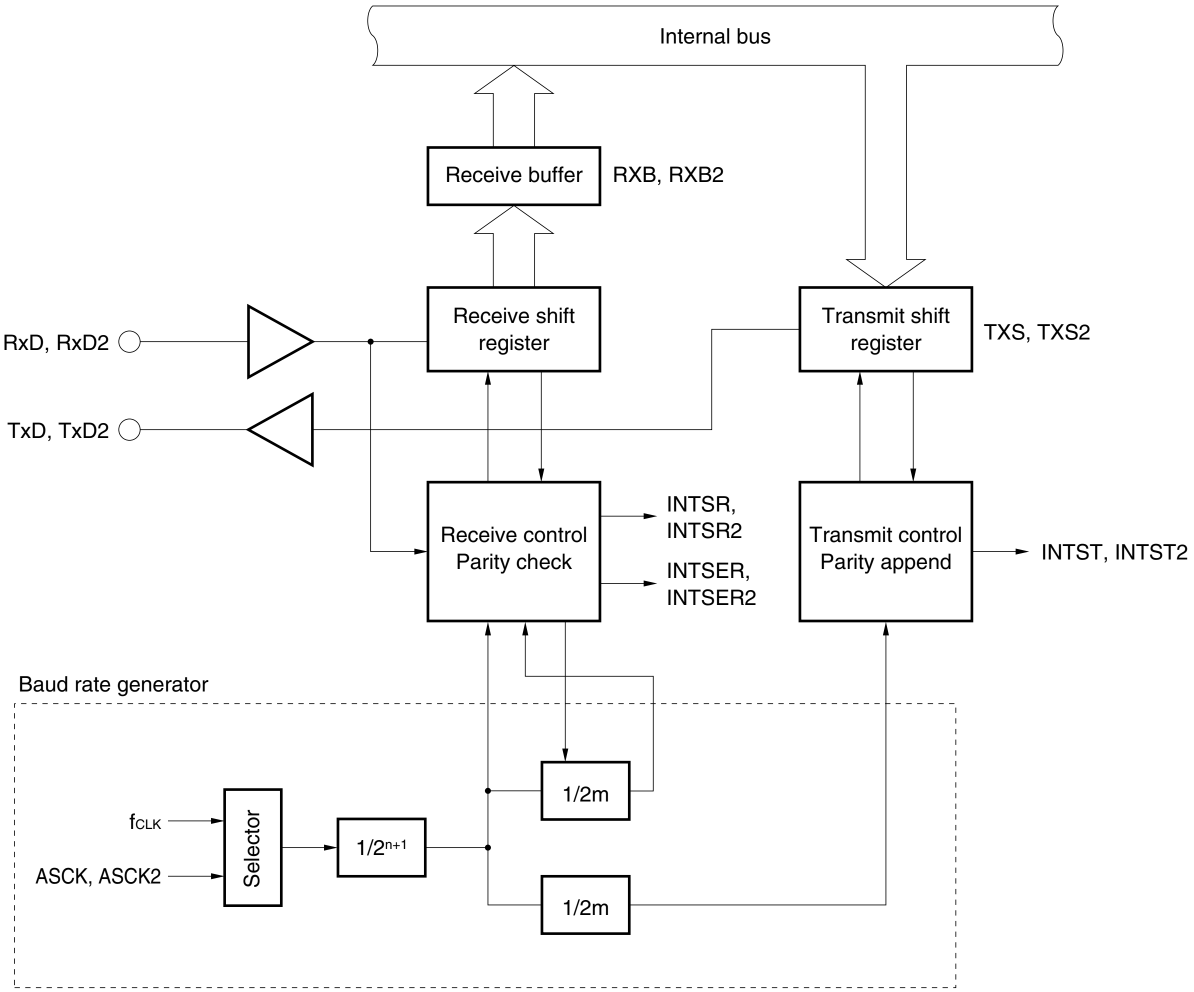
In this mode, 1-byte data following a start bit is transferred or received.

The internal baud rate generator allows communication in a wide range of baud rates.

The clock input to the ASCK pin can also be divided to define a baud rate.

The baud rate generator can also set a baud rate conforming to the MIDI standard (31.25 kbps).

Figure 7-8. Block Diagram in Asynchronous Serial Interface Mode



Remark f_{CLK}: internal system clock

n = 0 to 11

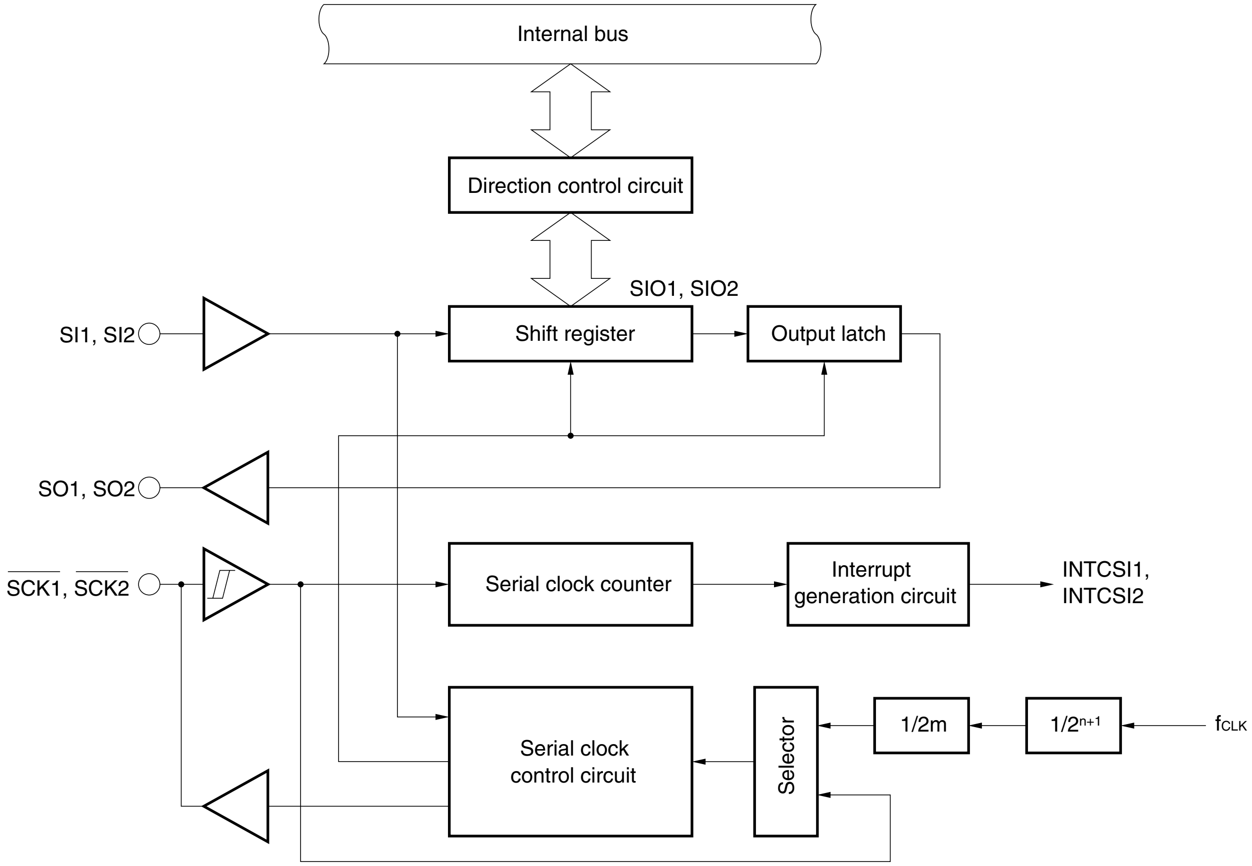
m = 16 to 30

(2) 3-wire serial I/O mode

This mode is to start transmission when the master device makes a serial clock active and to communicate 1-byte data in synchronization with this clock.

The interface in this mode communicates with devices that have conventional clocked serial interface. Basically, communication is performed by using three lines: serial clock ($\overline{\text{SCK}}$) and two serial data (SI and SO) lines. To connect two or more devices, a handshake line is necessary.

Figure 7-9. Block Diagram in 3-Wire Serial I/O Mode



Remark f_{CLK}: internal system clock

$n = 0$ to 11

$m = 1$, 16 to 30

7.7 Edge Detection Circuit

The interrupt input pins (NMI and INTP0 through INTP6) input not only interrupt requests but also trigger signals of the internal hardware. Because all the interrupts and internal hardware operate by detecting specific edges of the input signals, a function to detect edges is provided. In addition, a noise rejection function is also provided to prevent detection of a wrong edge due to noise.

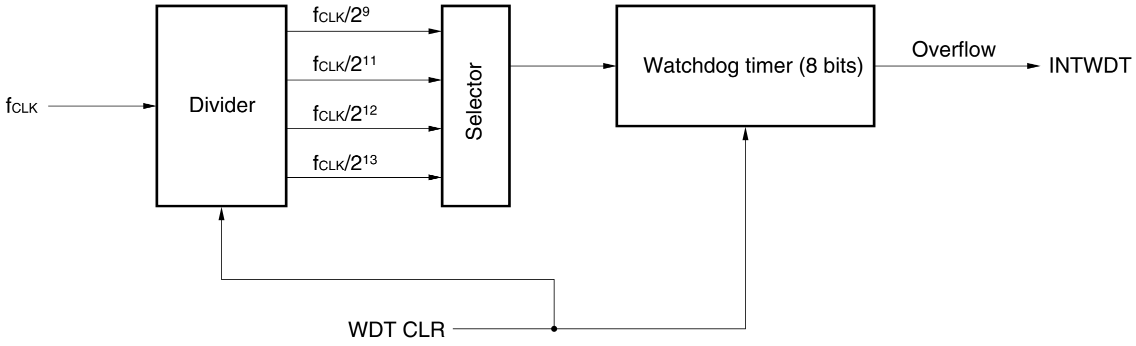
Pin	Detectable Edge	Noise Rejected by:
NMI	Either rising or falling edge	Analog delay
INTP0-INTP6	Either rising or falling edge, or both edges	Clock sampling[Note]

Note A sampling clock can be selected.

7.8 Watchdog Timer

A watchdog timer is provided to detect a hang-up of the CPU. This watchdog timer generates a non-maskable interrupt unless it is cleared by software within a specified interval time. Once the watchdog timer has been enable to operate, its operation cannot be stopped by software. Moreover, it can be specified whether the interrupt by the watchdog timer or the interrupt from the NMI pin takes precedence.

Figure 7-10. Block Diagram of Watchdog Timer



8. INTERRUPT FUNCTION

The three types of interrupt processing shown in Table 8-1 can be selected.

Table 8-1. Interrupt Request Processing

Processing Mode	Processed by:	Processing	Contents of PC and PSW
Vectored interrupt	Software	Branches to and executes processing routine (any processing contents).	Saves and restores to/from stack.
Context switching		Automatically selects register bank, and branches to and executes processing routine (any processing contents).	Saves or restores to/from fixed area in register bank.
Macro service	Firmware	Executes data transfer between memory and I/O (any processing contents).	Retained

8.1 Interrupt Source

As interrupt sources, twenty-seven sources listed in Table 8-2, BRK instruction execution, and operand error are available.

Four priority levels of interrupt processing can be selected, so that nesting during interrupt processing and the levels of interrupt requests that are generated at the same time can be controlled. However, nesting always advances with macro service (i.e., nesting is not kept pending).

The default priority is the priority (fixed) of the processing for the interrupt requests that have occurred at the same time and have the same priority level (refer to **Table 8-2**).

Table 8-2. Interrupt Sources

Type	Default Priority	Source		Internal/ External	Macro Service
		Name	Trigger		
Software	–	BRK instruction	Execution of instruction	–	–
		BRKCS instruction			
		Operand error	If result of exclusive OR of operands byte and $\overline{\text{byte}}$ is not FFH when MOV STBC, #byte, MOV WDM, #byte, or LOCATION instruction is executed		
Non-maskable	–	NMI	Detection of pin input edge	External	
		INTWDT	Overflow of watchdog timer	Internal	
Maskable	0 (highest)	INTOV0	Overflow of timer 0		○
	1	INTOV1	Overflow of timer 1		
	2	INTOV4	Overflow of timer 4		
	3	INTP0	Detection of pin input edge (CC00 capture trigger)	External	
		INTCC00	Generation of TM0-CC00 coincidence signal	Internal	
	4	INTP1	Detection of pin input edge (CC01 capture trigger)	External	
		INTCC01	Generation of TM0-CC01 coincidence signal	Internal	
	5	INTP2	Detection of pin input edge (CC02 capture trigger)	External	
		INTCC02	Generation of TM0-CC02 coincidence signal	Internal	
	6	INTP3	Detection of pin input edge (CC03 capture trigger)	External	
		INTCC03	Generation of TM0-CC03 coincidence signal	Internal	
	7	INTP4	Detection of pin input edge (A/D converter conversion start trigger)	External	
	8	INTP5	Detection of pin input edge (TM2 event counter input)		
	9	INTP6	Detection of pin input edge (TM3 event counter input)		
	10	INTCM10	Generation of TM1-CM10 coincidence signal	Internal	
	11	INTCM11	Generation of TM1-CM11 coincidence signal		
	12	INTCM20	Generation of TM2-CM20 coincidence signal		
	13	INTCM21	Generation of TM2-CM21 coincidence signal		
	14	INTCM30	Generation of TM3-CM30 coincidence signal		
	15	INTCM31	Generation of TM3-CM31 coincidence signal		
	16	INTCM40	Generation of TM4-CM40 coincidence signal		
	17	INTCM41	Generation of TM4-CM41 coincidence signal		
	18	INTSER	Occurrence of UART0 reception error		
	19	INTSR	End of UART0 reception		
		INTCSI1	End of 3-wire serial I/O1 transfer		
	20	INTST	End of UART0 transfer		
	21	INTSER2	Occurrence of UART2 reception error		
	22	INTSR2	End of UART2 reception		
		INTCSI2	End of 3-wire serial I/O2 transfer		
	23	INTST2	End of UART2 transfer		
	24 (lowest)	INTAD	End of A/D converter conversion (transfer to ADCR)		

8.2 Vectored Interrupt

Execution branches to a processing routine by using the memory contents of the vector table address corresponding to an interrupt source as the branch destination address.

The following operations are performed so that the CPU processes the interrupt:

- On branch : Saves status of CPU (contents of PC and PSW) to stack
- On returning : Restores status of CPU from stack

Execution is returned from the processing routine to the main routine by the RETI instruction.

The branch destination address must be in a range of 0 to FFFFH.

Table 8-3. Vector Table Address

Interrupt Source	Vector Table Address	Interrupt Source	Vector Table Address
BRK instruction	003EH	INTCM10	001AH
Operand error	003CH	INTCM11	001CH
NMI	0002H	INTCM20	001EH
INTWDT	0004H	INTCM21	0020H
INTOV0	0006H	INTCM30	0022H
INTOV1	0008H	INTCM31	0024H
INTOV4	000AH	INTCM40	0026H
INTP0	000CH	INTCM41	0028H
INTCC00		INTSER	002AH
INTP1	000EH	INTSR	002CH
INTCC01		INTCSI1	
INTP2	0010H	INTST	002EH
INTCC02		INTSER2	0030H
INTP3	0012H	INTSR2	0032H
INTCC03		INTCSI2	
INTP4	0014H	INTST2	0034H
INTP5	0016H	INTAD	0036H
INTP6	0018H		

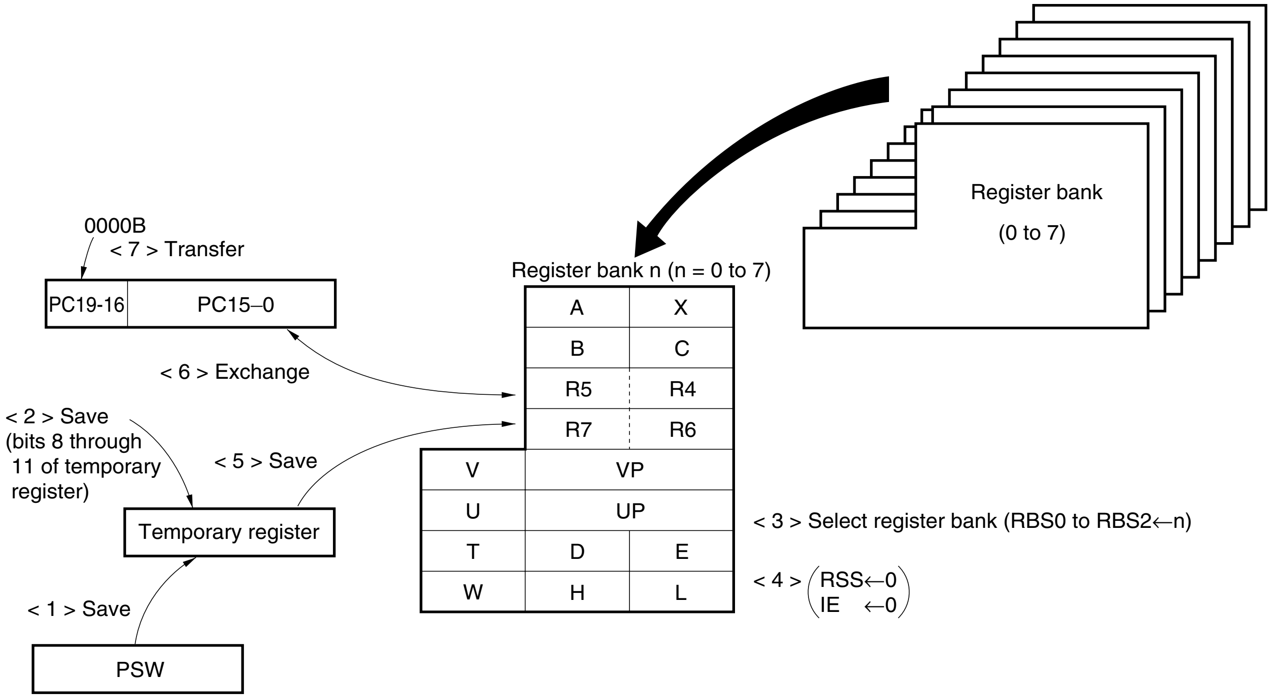
8.3 Context Switching

A specific register bank is selected by hardware when an interrupt request is generated or when the BRKCS instruction is executed.

Execution branches to the vector address stored in advance to the selected register bank, and the current contents of the program counter (PC) and program status word (PSW) are stacked to the register bank.

The branch destination address must be in a range of 0 to FFFFH.

Figure 8-1. Context Switching Operation When Interrupt Request Is Generated

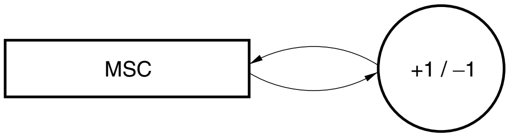


8.4 Macro Service

The μPD784046(A) has a total of seven types of macro service. Each macro service is outlined below.

(1) Counter mode: EVTCNT

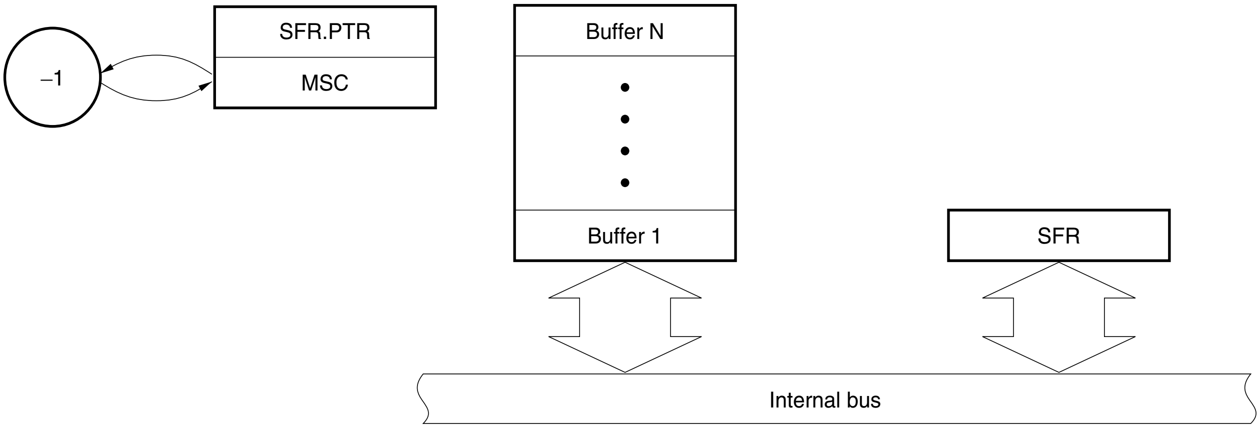
- **Operation** (a) Increments or decrements an 8-bit macro service counter (MSC).
  (b) A vectored interrupt request is generated when the value of MSC reaches 0.



- **Application example:** Event counter, measurement of number of times of capture

(2) Block transfer mode: BLKTRS

- **Operation** (a) Transfers block data between the buffer and an SFR specified by the SFR pointer (SFR.PTR).
  (b) The transfer source and destination can be an SFR or buffer. The length of the data to be transferred can be byte or word.
  (c) The number of times data is to be transferred (block size) is specified by MSC.
  (d) MSC is auto-decremented (–1) each time the macro service has been executed.
  (e) When the value of MSC has reached 0, a vectored interrupt request is generated.

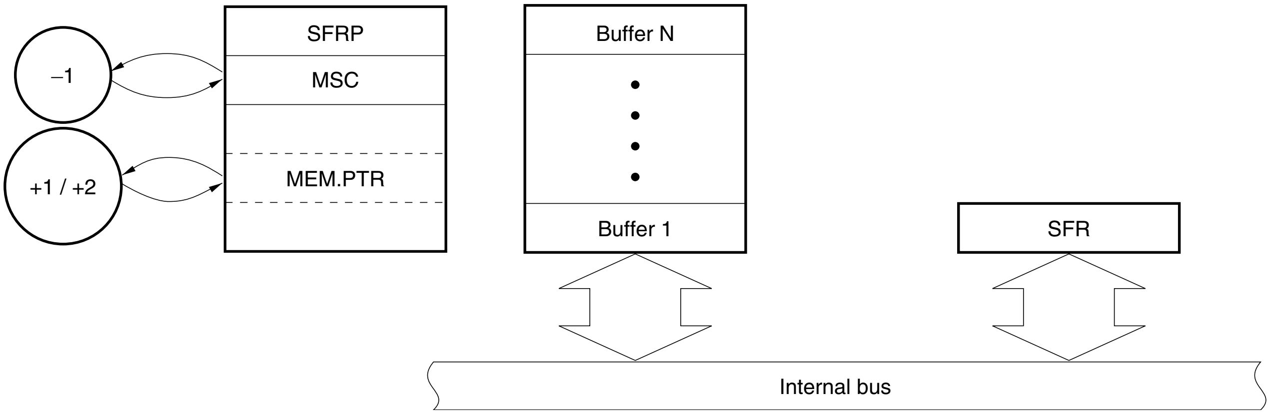


- **Application example:** Data transfer/reception of serial interface

(3) Block transfer mode (with memory pointer): BLKTRS-P

- **Operation** This is the block transfer mode in (2) with a memory pointer (MEM.PTR) appended. The appended buffer area of MEMP can be freely set on the memory space.

Remark MEM.PTR is auto-incremented (+1: byte data transfer/+2: word data transfer) each time the macro service has been executed.

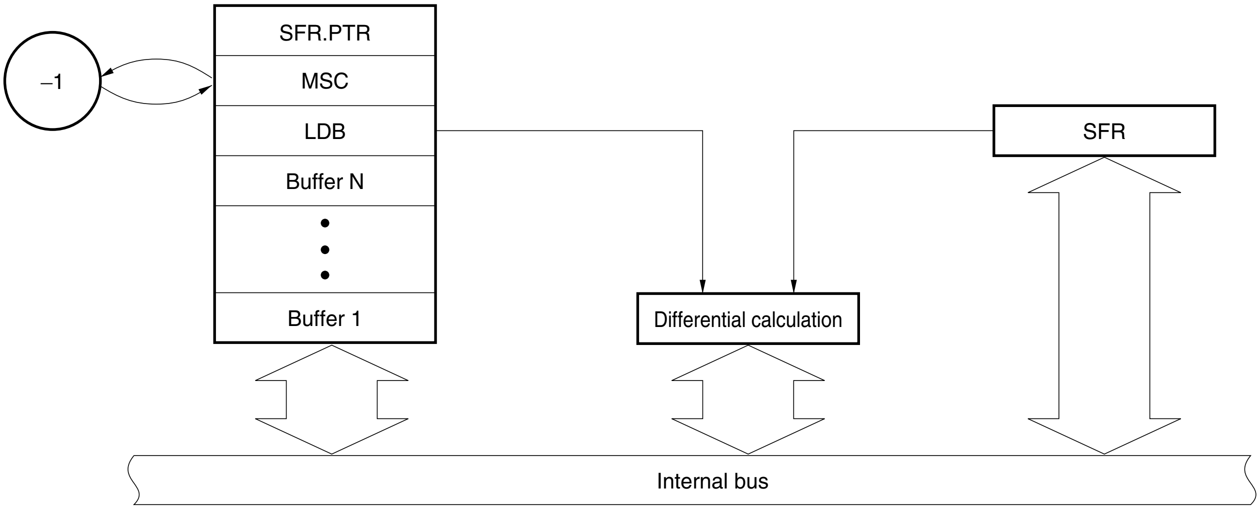


- **Application example:** Same as (2)

(4) Data differential mode: DTADIF

- **Operation** (a) Calculates the difference between the contents of the SFR specified by SFR pointer (SFR.PTR) (current value) and the contents of the SFR loaded to the last data buffer (LDB).
  (b) Stores the result of the calculation to a predetermined buffer area.
  (c) Stores the contents of the current value of SFR to LDB.
  (d) The number of times the data is to be transferred (block size) is specified by MSC. The value of MSC is auto-decremented (–1) each time the macro service has been executed.
  (e) When the value of MSC has reached 0, a vectored interrupt request is generated.

Remark The differential calculation can be performed only an SFR of 16-bit configuration.



- **Application example:** Measurement of period and pulse width by capture register of timer 0

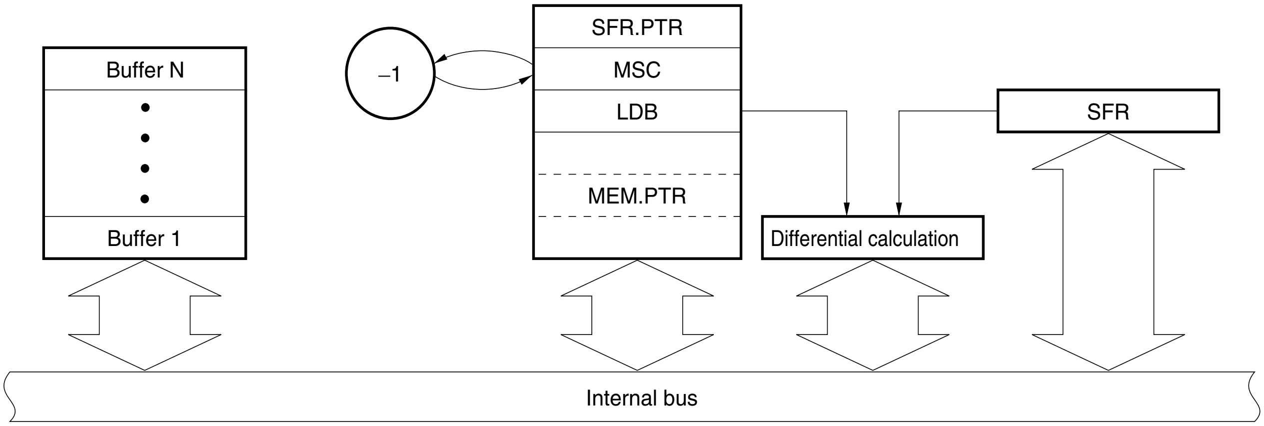
(5) Data differential mode (with memory pointer): DTADIF-P

- **Operation** This is the data differential mode in (4) with a memory pointer (MEM.PTR) appended. The appended MEM.PTR can set a buffer area to which the differential data is to be stored on the memory space freely.

Remarks 1. The differential calculation can be performed only an SFR of 16-bit configuration.

2. The buffer is specified by the result of an operation between MEM.PTR and MSC[Note]. The value of MEM.PTR is not updated after the data has been transferred.

Note MEM.PTR – (MSC × 2) + 2



- **Application example:** Same as (4)

(6) CPU monitoring mode0: SFLF0

- Operation (a) Checks the internal operation of the CPU.
  (b) When the blocks are operating normally, the value given by subtracting 10 from the initial value is transferred to the SFR specified by the SFR pointer (SFR.PTR).
- **Application example:** Used for self checking of the CPU during normal operation.

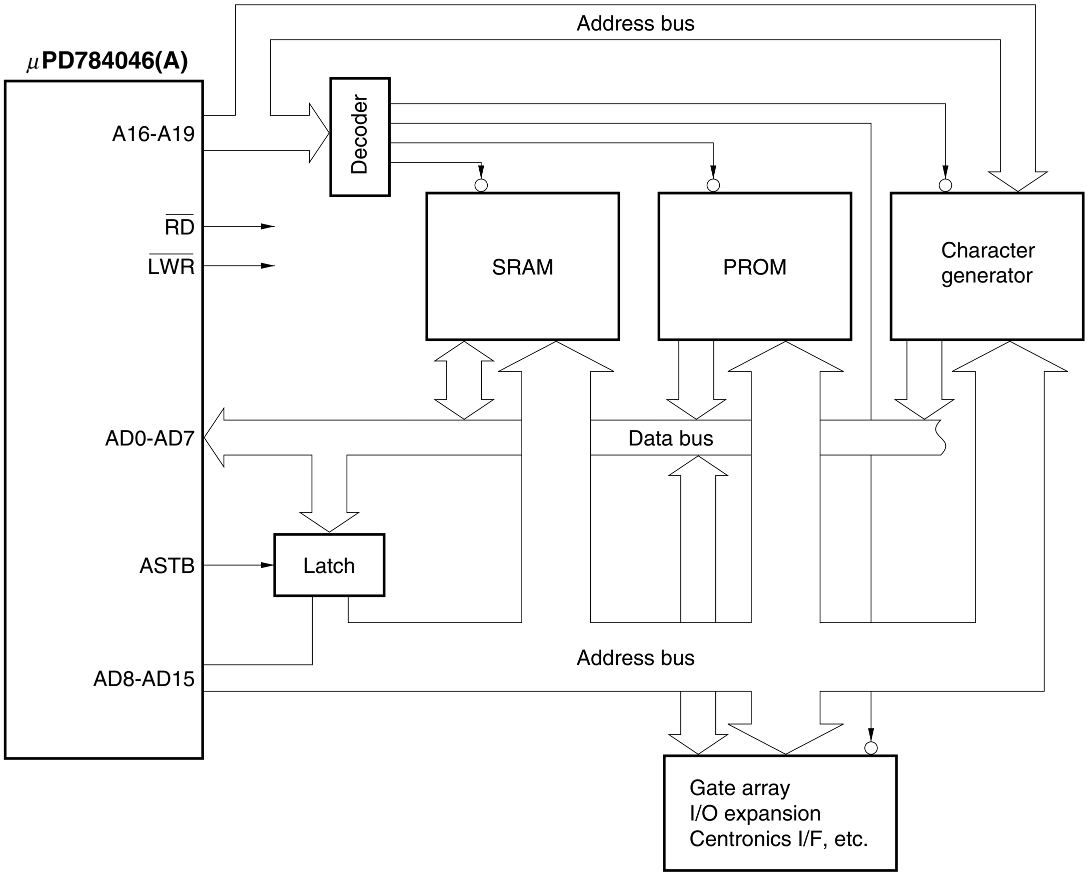
(7) CPU monitoring mode1: SELF1

- Operation (a) Checks the internal operation of the CPU.
  (b) When the blocks are operating normally, the value given by subtracting 8 from the initial value is transferred to the SFR specified by the SFR pointer (SFR.PTR).
- **Application example:** Used for self checking of the CPU during normal operation.

9. LOCAL BUS INTERFACE

The μPD784046(A) can be connected to an external memory or I/O (memory mapped I/O), supporting a 1M-byte memory space (refer to **Figure 9-1**).

Figure 9-1. Example of Local Bus Interface (with external 8-bit bus specified)



9.1 Memory Expansion

The external program memory or data memory can be expanded from 256 bytes up to 1M bytes in seven steps.

When an external device is connected, the address/data bus and read/write strobe signals are controlled by using ports 4 through 6 and P90 through P93 pins. The functions of these ports and pins are set by the memory expansion mode register (MM).

Table 9-1. Setting of Pin Function

Memory Expansion Mode Register	Pin Function			
	Port 4	Port 5	Port 6	
MM0-MM3	P40-P47	P50-P57	P60-P63	P90-P93
Port mode	General-purpose port			
External memory expansion mode	AD0-AD7	AD8 to AD15 are set stepwise. Rest of pins can be used as general-purpose port pins.	A16 through A19 are set stepwise. Rest of pins can be used as general-purpose port pins.	P90 : $\overline{\text{RD}}$ P91 : $\overline{\text{LWR}}$ P92 : $\overline{\text{HWR}}$ P93 : ASTB

Remark AD8 through AD15 are used as address bus.

The number of pins of ports 5 and 6 that are used as address bus pins can be changed according to the size of the external memory connected (external address space), so that the external memory can be expanded stepwise. The pins not used as address bus pins can be used as general-purpose I/O port pins (refer to **Table 9-2**). The external address space can be set in seven steps by MM.

Table 9-2. Operations of Ports 5 and 6 (in external memory expansion mode)

Port 5								Port 6				External address space
P50	P51	P52	P53	P54	P55	P56	P57	P60	P61	P62	P63	
General-purpose port												256 bytes or less[Note]
AD8	AD9											1K bytes or less[Note]
		AD10	AD11									4K bytes or less[Note]
				AD12	AD13							16K bytes or less[Note]
						AD14	AD15					64K bytes or less
								A16	A17			256K bytes or less
										A18	A19	1M bytes or less

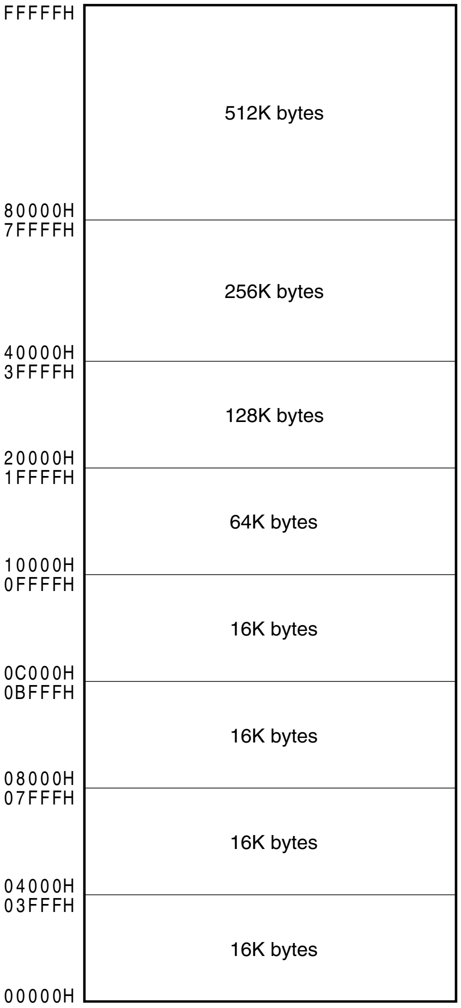
Note When the external 16-bit bus is specified, do not set MM such that the external address space is of this size.

Caution **When the external 16-bit bus is specified, set MM such that all the pins of port 5 (P50 through P57) are used as AD pins (AD8 through AD15).**

9.2 Memory Space

The 1M-byte memory space is divided into the following eight spaces of logical addresses. Each space can be controlled by using the programmable wait function and bus sizing function.

Figure 9-2. Memory Space



9.3 Programmable Wait

A wait state can be inserted to each of the eight memory spaces while the $\overline{\mathrm{RD}}$, $\overline{\mathrm{LWR}}$, and $\overline{\mathrm{HWR}}$ signals are active. Even if memories with different access times are connected, therefore, the overall efficiency of the system is not degraded.

In addition, an address wait function that extends the active period of the ASTB signal is also available to extend the address decode time (this function can be set to all the spaces).

9.4 Bus Sizing Function

The μPD784046(A) can change the external data bus width between 8 and 16 bits when an external device is connected. Even if the memory space is divided by eight, the bus width of each memory space can be specified independently.

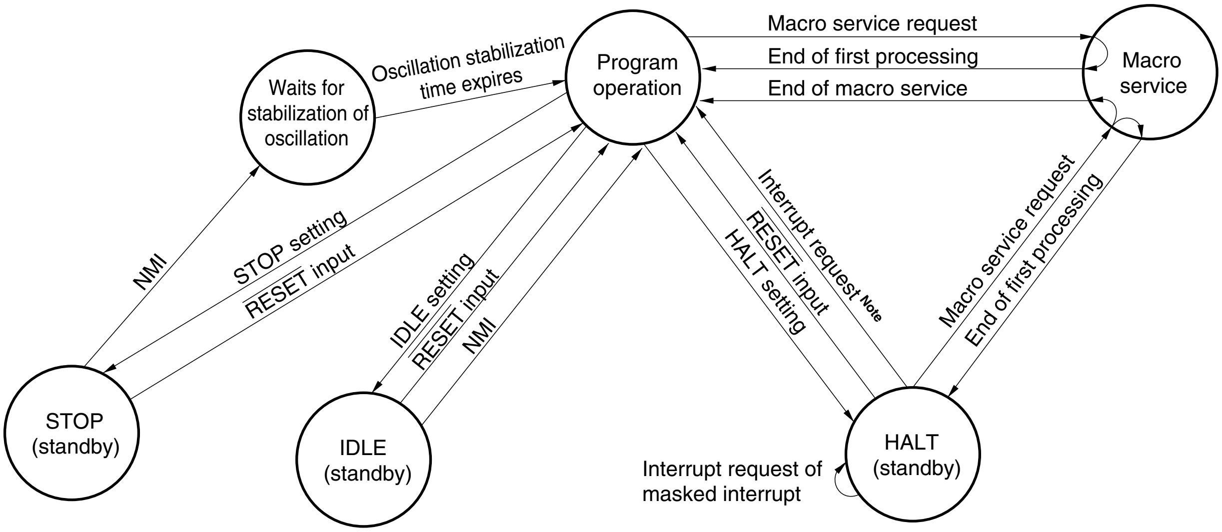
10. STANDBY FUNCTION

The μPD784046(A) has the following standby function modes that reduce the power consumption of the chip.

• HALT mode	: This mode stops the operating clock of the CPU. It can reduce the average power consumption through intermittent operation by combination of a normal operation and this mode.
• IDLE mode	: This mode stops the entire system with the operation of the oscillation circuit continuing. Normal program operation can be restored from this mode with the power consumption close to that in the STOP mode and time equivalent to that in the HALT mode.
• STOP mode	: This mode stops the oscillator and stops all the internal operations of the chip to minimize the power consumption to the level of only leakage current.

These modes are programmable.
Macro service can be started from the HALT mode.

Figure 10-1. Standby Status Transition



Note Only unmasked interrupt request

Remark Only external input of NMI is valid. The watchdog timer cannot be used to release the standby mode (STOP/HALT/IDLE).

11. RESET FUNCTION

When a low level is input to the $\overline{\text{RESET}}$ pin, the internal hardware is initialized (reset status).
When the $\overline{\text{RESET}}$ signal goes high, the following data is set to the program counter (PC).

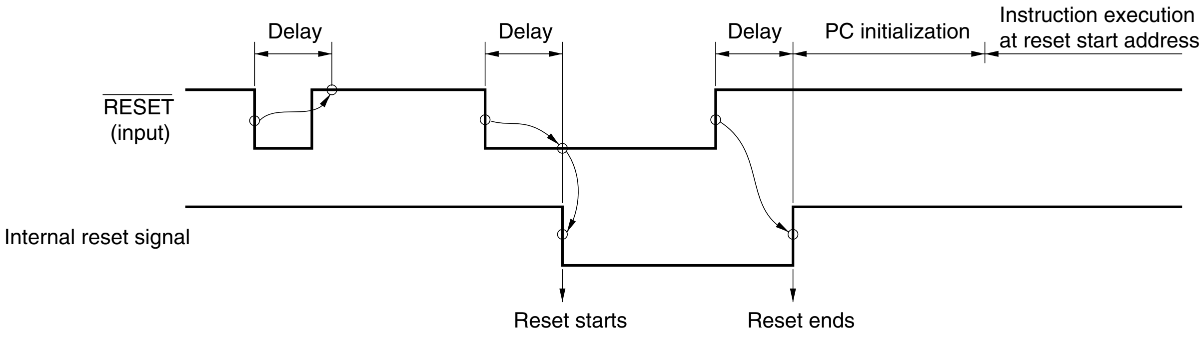
- Lower 8 bits of PC : contents of address 0000H
- Middle 8 bits of PC : contents of address 0001H
- Higher 4 bits of PC : 0

The contents of the PC are assumed as a branch destination address and program execution is started from this address. Therefore, the program can be reset and started from any address.

Set the contents of each register by program as necessary.

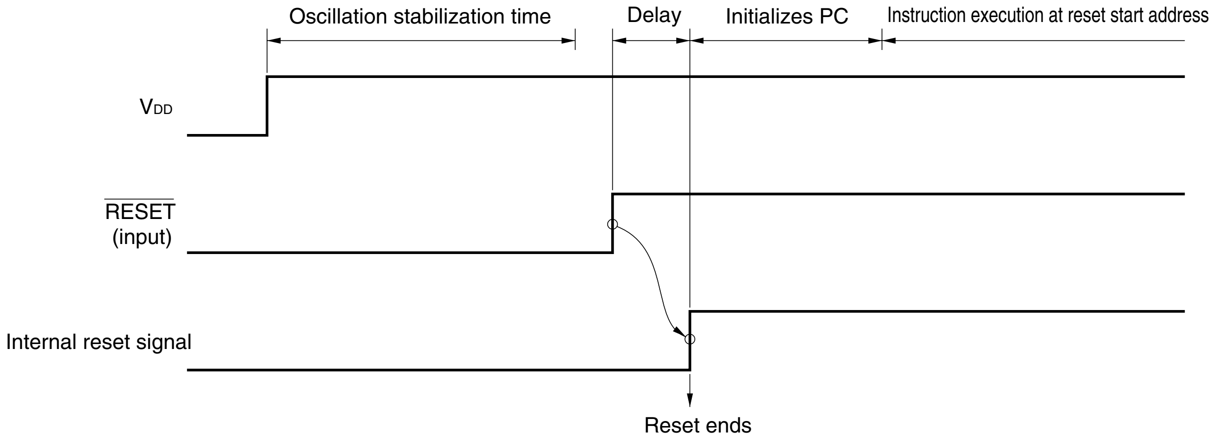
To prevent malfunctioning due to noise, a noise rejection circuit is provided to the $\overline{\text{RESET}}$ input circuit. This noise rejection circuit is a sampling circuit with analog delay.

Figure 11-1. Accepting Reset



Keep the $\overline{\text{RESET}}$ signal active until the oscillation stabilization time (about 40 ms) elapses when executing a reset operation on power application or when releasing the STOP mode by reset.

Figure 11-2. Reset Operation on Power Application



12. INSTRUCTION SET

(1) 8-bit instructions (( ): combination realized by writing A as r)

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP, MOVM, XCHM, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC, CHKL, CHKLA

Table 12-1. Instructions for 8-Bit Addressing

2nd Operand 1st Operand	#byte	A	r r’	saddr saddr’	sfr	!addr16 !!addr24	mem [saddrp] [%saddrg]	r3 PSWL PSWH	[WHL+] [WHL–]	n	None$^{\text{Note 2}}$
A	(MOV) ADD$^{\text{Note 1}}$	(MOV) (XCH) (ADD)$^{\text{Note 1}}$	MOV XCH (ADD)$^{\text{Note 1}}$	(MOV)$^{\text{Note 6}}$ (XCH)$^{\text{Note 6}}$ (ADD)$^{\text{Note 1, 6}}$	MOV (XCH) (ADD)$^{\text{Note 1}}$	(MOV) (XCH) ADD$^{\text{Note 1}}$	MOV XCH ADD$^{\text{Note 1}}$	MOV	(MOV) (XCH) (ADD)$^{\text{Note 1}}$		
r	MOV ADD$^{\text{Note 1}}$	(MOV) (XCH) (ADD)$^{\text{Note 1}}$	MOV XCH ADD$^{\text{Note 1}}$	MOV XCH ADD$^{\text{Note 1}}$	MOV XCH ADD$^{\text{Note 1}}$	MOV XCH				ROR$^{\text{Note 3}}$	MULU DIVUW INC DEC
saddr	MOV ADD$^{\text{Note 1}}$	(MOV)$^{\text{Note 6}}$ (ADD)$^{\text{Note 1}}$	MOV ADD$^{\text{Note 1}}$	MOV XCH ADD$^{\text{Note 1}}$							INC DEC DBNZ
sfr	MOV ADD$^{\text{Note 1}}$	MOV (ADD)$^{\text{Note 1}}$	MOV ADD$^{\text{Note 1}}$								PUSH POP CHKL CHKLA
!addr16 !!addr24	MOV	(MOV) ADD$^{\text{Note 1}}$	MOV								
mem [saddrp] [%saddrg]		MOV ADD$^{\text{Note 1}}$									
mem3											ROR4 ROL4
r3 PSWL PSWH	MOV	MOV									
B, C											DBNZ
STBC, WDM	MOV										
[TDE+] [TDE–]		(MOV) (ADD)$^{\text{Note 1}}$ MOVM$^{\text{Note 4}}$							MOVBK$^{\text{Note 5}}$		

Notes 1. ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as ADD.

2. Either the second operand is not used, or the second operand is not an operand address.

3. ROL, RORC, ROLC, SHR, and SHL are the same as ROR.

4. XCHM, CMPME, CMPMNE, CMPMNC, and CMPMC are the same as MOVM.

5. XCHBK, CMPBKE, CMPBKNE, CMPBKNC, and CMPBKC are the same as MOVBK.

6. If saddr is saddr2 in this combination, some instructions have a short code length.

(2) 16-bit instructions (( ): combination realized by writing AX as rp)

MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

Table 12-2. Instructions for 16-Bit Addressing

2nd Operand 1st Operand	#word	AX	rp rp'	saddrp saddrp'	sfrp	!addr16 !!addr24	mem [saddrp] [%saddrg]	[WHL+]	byte	n	None[Note 2]
AX	(MOVW) ADDW[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	(MOVW)[Note 3] (XCHW)[Note 3] (ADDW)[Note 1, 3]	MOVW (XCHW) (ADDW)[Note 1]	(MOVW) XCHW	MOVW XCHW	(MOVW) (XCHW)			
rp	MOVW ADDW[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW				SHRW SHLW	MULW[Note 4] INCW DECW
saddrp	MOVW ADDW[Note 1]	(MOVW)[Note 3] (ADDW)[Note 1]	MOVW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]							INCW DECW
sfrp	MOVW ADDW[Note 1]	MOVW (ADDW)[Note 1]	MOVW ADDW[Note 1]								PUSH POP
!addr16 !!addr24	MOVW	(MOVW)	MOVW						MOVTBLW		
mem [saddrp] [%saddrg]		MOVW									
PSW											PUSH POP
SP	ADDWG SUBWG										
post											PUSH POP PUSHU POPU
[TDE+]		(MOVW)						SACW			
byte											MACW MACSW

Notes 1. SUBW and CMPW are the same as ADDW.

2. Either the second operand is not used, or the second operand is not an operand address.

3. If saddrp is saddrp2 in this combination, some instructions have a short code length.

4. MULUW and DIVUX are the same as MULW.

(3) 24-bit instructions (( ): combination realized by writing WHL as rg)

MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

Table 12-3. Instructions for 24-Bit Addressing

2nd Operand / 1st Operand	#imm24	WHL	rg rg'	saddrg	!!addr24	mem1	[%saddrg]	SP	None[Note]
WHL	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) ADDG SUBG	(MOVG)	MOVG	MOVG	MOVG	
rg	MOVG ADDG SUBG	(MOVG) (ADDG) (SUBG)	MOVG ADDG SUBG	MOVG	MOVG				INCG DECG PUSH POP
saddrg		(MOVG)	MOVG						
!!addr24		(MOVG)	MOVG						
mem1		MOVG							
[%saddrg]		MOVG							
SP	MOVG	MOVG							INCG DECG

Note Either the second operand is not used, or the second operand is not an operand address.

(4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BCLR, BFSET

Table 12-4. Addressing of Bit Manipulation Instructions

2nd Operand 1st Operand	CY	saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	/saddr.bit /sfr.bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit	None[Note]
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	NOT1 SET1 CLR1
saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	MOV1			NOT1 SET1 CLR1 BF BT BTCLR BFSET

Note Either the second operand is not used, or the second operand is not an operand address.

(5) Call/return/branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Table 12-5. Addressing for Call/Return/Branch Instructions

Operand of instruction address	$addr20	$!addr20	!addr16	!!addr20	rp	rg	[rp]	[rg]	!addr11	[addr5]	RBn	None
Basic instruction	BC[Note] BR	CALL BR	CALL BR RETCS RETCSB	CALL BR	CALL BR	CALL BR	CALL BR	CALL BR	CALLF	CALLT	BRKCS	BRK RET RETI RETB
Compound instruction	BF BT BTCLR BFSET DBNZ											

Note BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH are the same as BC.

(6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT, EI, DI, SWRS

13. ELECTRICAL SPECIFICATIONS

Caution The followings are the specifications for the μPD784044(A), (A1), and (A2). For the μPD784046(A), (A1), and (A2), these are target specifications.

(1) Electrical specifications of μPD784044(A), 784046(A) (1/6)

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.5 to +7.0	V
	AV_{DD}			–0.5 to V_{DD} + 0.5	V
	AV_{SS}			–0.5 to +0.5	V
Input voltage	V_I	**Note 1**		–0.5 to V_{DD} + 0.5 ≤ 7.0	V
Output voltage	V_O			–0.5 to V_{DD} + 0.5	V
Low-level output current	I_{OL}	All output pins		15	mA
		Total of all output pins		150	mA
High-level output current	I_{OH}	All output pins		–10	mA
		Total of all output pins		–100	mA
Analog input voltage	V_{IAN}	**Note 2**	$AV_{DD} > V_{DD}$	–0.5 to V_{DD} + 0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} + 0.5	
A/D converter reference input voltage	AV_{REF}		$AV_{DD} > V_{DD}$	–0.5 to V_{DD} + 0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} + 0.5	
Operating temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Notes 1. Pins other than the pins in **Note 2**.

2. Pins P70/ANI0-P77/ANI7, P80/ANI8-P87/ANI15

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

Recommended Operating Conditions

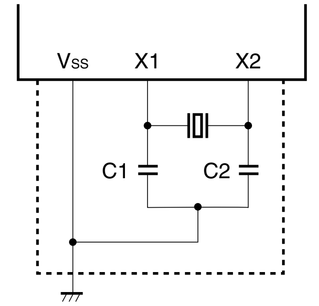
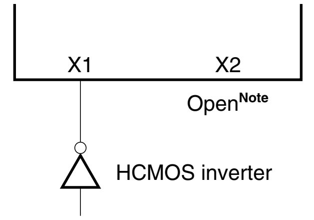
Oscillation Frequency	T_A	V_{DD}
8 MHz ≤ f_{XX} ≤ 25 MHz	–40 to +85 °C	4.5 to 5.5 V

Capacitance (T_A = 25 °C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz 0 V except measured pins			10	pF
Output capacitance	C_O				10	pF
I/O capacitance	C_{IO}				10	pF

(1) Electrical specifications of μPD784044(A), 784046(A) (2/6)

Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Item	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillation frequency (f_{XX})	8	25	MHz
External clock		X1 input frequency (f_X)	8	25	MHz
		X1 input rise, fall time	0	5	ns
		X1 input high-, low-level width	20	105	ns

Note When the EXTC bit of the oscillation stabilization time specification register (OSTS) = 0. Input the reverse phase clock of the pin X1 to the pin X2 when the EXTC bit = 1.

Caution When using a system clock oscillation circuit, wire the portion enclosed by the dotted line in the diagram above as follows to prevent adverse influence from wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines. Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground potential for the capacitor in the oscillation circuit at the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not extract any signal from the oscillation circuit.**

(1) Electrical specifications of μPD784044(A), 784046(A) (3/6)

DC Characteristics (T_A = –40 to +85 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}			0		0.8	V
High-level input voltage	V_{IH1}	**Note 1**		2.2		V_{DD}	V
	V_{IH2}	**Note 2**		0.8 V_{DD}		V_{DD}	
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA				0.45	V
High-level output voltage	V_{OH}	I_{OH} = –400 μA		V_{DD} – 1.0			V
Input leakage current	I_{LI}	**Note 3**	0 V ≤ V_I ≤ V_{DD}			±10	μA
Analog pin input leakage current	I_{LIAN}	**Note 4**	0 V ≤ V_I ≤ AV_{DD}			±1	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operating mode (f_{XX} = 25 MHz)			40	70	mA
	I_{DD2}	HALT mode (f_{XX} = 25 MHz)			25	50	mA
	I_{DD3}	IDLE mode (f_{XX} = 25 MHz)			10	20	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	15	μA
			V_{DDDR} = 5 V ± 10 %		15	50	μA
Pull-up resistor	R_L			15	40	80	kΩ

Notes
1. Pins other than pins in **Note 2**.
2. P20/NMI, P21/INTP0/TO00, P22/INTP1/TO01, P23/INTP2/TO02, P24/INTP3/TO03, P25/INTP4, P26/INTP5/TI2, P27/INTP6/TI3, P34/ASCK/$\overline{\text{SCK1}}$, P37/ASCK2/$\overline{\text{SCK2}}$, X1, X2, $\overline{\text{RESET}}$
3. Input and I/O pins (except X1 and X2, and P70/ANI0-P77/ANI7, P80/ANI8-P87/ANI15 used as analog inputs)
4. Pins P70/ANI0-P77/ANI7, P80/ANI8-P87/ANI15 (pins used as analog input, only during the non-sampling operation)

(1) Electrical specifications of μPD784044(A), 784046(A) (4/6)

AC Characteristics (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Read/write operation

Parameter	Symbol	Expression	MIN.	MAX.	Unit
System clock cycle time	t_{CYK}		80	250	ns
Address setup time (vs. ASTB↓)	t_{SAST}	(0.5 + a) T – 20	20		ns
Address hold time (vs. ASTB↓)	t_{HSTA}	0.5T – 20	20		ns
ASTB high-level width	t_{WSTH}	(0.5 + a) T – 17	23		ns
Address→$\overline{\text{RD}}$↓ delay time	t_{DAR}	(1 + a) T – 15	65		ns
$\overline{\text{RD}}$↓→address float time	t_{FRA}			0	ns
Address→data input time	t_{DAID}	(2.5 + a + n) T – 56		144	ns
$\overline{\text{RD}}$↓→data input time	t_{DRID}	(1.5 + n) T – 48		72	ns
ASTB↓→$\overline{\text{RD}}$↓ delay time	t_{DSTR}	0.5T – 16	24		ns
Data hold time (vs. $\overline{\text{RD}}$↑)	t_{HRID}		0		ns
$\overline{\text{RD}}$↑→address active time	t_{DRA}	0.5T – 14	26		ns
$\overline{\text{RD}}$ low-level width	t_{WRL}	(1.5 + n) T – 30	90		ns
Address→$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓ delay time	t_{DAW}	(1 + a) T – 15	65		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→data output time	t_{DWOD}			15	ns
ASTB↓→$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓ delay time	t_{DSTW}	0.5T – 16	24		ns
Data setup time (vs. $\overline{\text{LWR}}$, $\overline{\text{HWR}}$↑)	t_{SODW}	(1.5 + n) T – 25	95		ns
Data hold time (vs. $\overline{\text{LWR}}$, $\overline{\text{HWR}}$↑)	t_{HWOD}	0.5T – 14	26		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↑→ ASTB↑ delay time	t_{DWST}	1.5T – 15	105		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$ low-level width	t_{WWL}	(1.5 + n) T – 36	84		ns
Address→$\overline{\text{WAIT}}$↓ input time	t_{DAWT}	(2 + a) T – 50		110	ns
ASTB↓→$\overline{\text{WAIT}}$↓ input time	t_{DSTWT}	1.5T – 40		80	ns
ASTB↓→$\overline{\text{WAIT}}$ hold time	t_{HSTWT}	(1.5 + n) T + 5	125		ns
ASTB↓→$\overline{\text{WAIT}}$↑ delay time	t_{DSTWTH}	(1.5 + n) T – 40		160$^{\text{Note}}$	ns
$\overline{\text{RD}}$↓→$\overline{\text{WAIT}}$↓ input time	t_{DRWT}	T – 40		40	ns
$\overline{\text{RD}}$↓→$\overline{\text{WAIT}}$ hold time	t_{HRWT}	(1 + n) T + 5	85		ns
$\overline{\text{RD}}$↓→$\overline{\text{WAIT}}$↑ delay time	t_{DRWTH}	(1 + n) T – 40		120$^{\text{Note}}$	ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→$\overline{\text{WAIT}}$↓ input time	t_{DWWT}	T – 40		40	ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→$\overline{\text{WAIT}}$ hold time	t_{HWWT}	(1 + n) T + 5	85		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→$\overline{\text{WAIT}}$↑ delay time	t_{DWWTH}	(1 + n) T – 40		120$^{\text{Note}}$	ns

Note Specification when an external wait is inserted

Remarks
1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} is internal system clock frequency)
2. a = 1 when an address wait is inserted, otherwise, 0.
3. n indicates the number of the wait cycles by specifying the external wait pins ($\overline{\text{WAIT}}$) or programmable wait control registers 1, 2 (PWC1, PWC2). (n ≥ 0. n ≥ 1 for t_{DSTWTH}, t_{DRWTH}, t_{DWWTH}).
4. Calculate values in the expression column with the system clock cycle time to be used because these values depend on the system clock cycle time (t_{CYK} = T). The values in the above expression column are calculated based on T = 80 ns.

(1) Electrical specifications of μPD784044(A), 784046(A) (5/6)

Serial Operation (T_A = –40 to +85 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ output	BRG	T_{SFT}		ns
		$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ input	External clock	640		ns
Serial clock low-level width	t_{WSKL}	$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ output	BRG	$0.5T_{SFT}–40$		ns
		$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ input	External clock	280		ns
Serial clock high-level width	t_{WSKH}	$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ output	BRG	$0.5T_{SFT}–40$		ns
		$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ input	External clock	280		ns
SI1, SI2 setup time (vs. $\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$↑)	t_{SSSK}			80		ns
SI1, SI2 hold time (vs. $\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$↑)	t_{HSSK}			80		ns
$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$↓→SO1, SO2 output delay time	t_{DSBSK}	R = 1 kΩ, C = 100 pF		0	150	ns

Remarks **1.** T_{SFT} is a value set in software. The minimum value is $t_{CYK} \times 8$.

2. $t_{CYK} = 1/f_{CLK}$ (f_{CLK} is internal system clock frequency)

Other Operations (T_A = –40 to +85 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

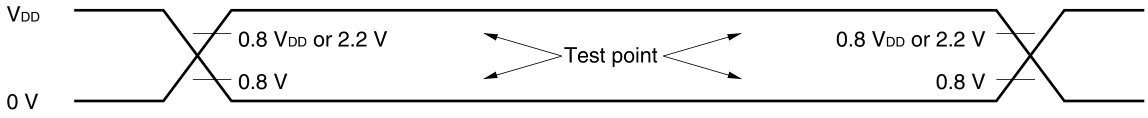
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI high, low-level width	t_{WNIH}, t_{WNIL}		10		μs
INTP0-INTP6 high, low-level width	t_{WITH}, t_{WITL}		4		t_{CYSMP}
TI2, TI3 high, low-level width	t_{WTIH}, t_{WTIL}		4		t_{CYSMP}
$\overline{\text{RESET}}$ high, low-level width	t_{WRSH}, t_{WRSL}		10		μs

Remarks **1.** t_{CYSMP} is a sampling clock set in the noise protection control register (NPC) in software.
When NIn = 0, $t_{CYSMP} = t_{CYK}$
When NIn = 1, $t_{CYSMP} = t_{CYK} \times 4$

2. $t_{CYK} = 1/f_{CLK}$ (f_{CLK} is internal system clock frequency)

3. NIn: Bit n of NPC (n = 0-6)

AC Timing Test Point



(1) Electrical specifications of μPD784044(A), 784046(A) (6/6)

AD Converter Characteristics (T_A = –40 to +85 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{DD} – 0.5 V ≤ AV_{DD} ≤ V_{DD})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				10			bit
Total error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD}				±0.5	%FSR
		3.4 V ≤ AV_{REF} < 4.5 V				±0.7	%FSR
Quantization error						±1/2	LSB
Conversion time	t_{CONV}	80 ns ≤ t_{CYK} ≤ 250 ns		169			t_{CYK}
Sampling time	t_{SAMP}	80 ns ≤ t_{CYK} ≤ 250 ns		20			t_{CYK}
Zero-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±3.5	LSB
		3.4 V ≤ AV_{REF} < 4.5 V			±1.5	±4.5	LSB
Full-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±3.5	LSB
		3.4 V ≤ AV_{REF} < 4.5 V			±1.5	±4.5	LSB
Nonlinearity error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} < 4.5 V			±1.5	±4.5	LSB
Analog input voltage	V_{IAN}			–0.3		AV_{REF}+0.3	V
A/D converter reference input voltage	AV_{REF}			3.4		AV_{DD}	V
AV_{REF} current	AI_{REF}				1.0	3.0	mA
AV_{DD} supply current	AI_{DD}				2.0	6.0	mA
A/D converter data retention current	AI_{DDDR}	STOP mode	AV_{DDDR} = 2.5 V		2	10	μA
			AV_{DDDR} = 5 V ± 10%		10	50	μA

Note The quantization error is excluded.

Remark t_{CYK} = 1/f_{CLK} (f_{CLK} is internal system clock frequency).

(2) Electrical specifications of μPD784044(A1), 784046(A1) (1/6)

Absolute Maximum Ratings (T_A = 25 ˚C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.5 to +7.0	V
	AV_{DD}			–0.5 to V_{DD} + 0.5	V
	AV_{SS}			–0.5 to +0.5	V
Input voltage	V_I	**Note 1**		–0.5 to V_{DD} + 0.5 ≤ 7.0	V
Output voltage	V_O			–0.5 to V_{DD} + 0.5	V
Low-level output current	I_{OL}	All output pins		15	mA
		Total of all output pins		150	mA
High-level output current	I_{OH}	All output pins		–10	mA
		Total of all output pins		–100	mA
Analog input voltage	V_{IAN}	**Note 2**	$AV_{DD} > V_{DD}$	–0.5 to V_{DD} + 0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} + 0.5	
A/D converter reference input voltage	AV_{REF}		$AV_{DD} > V_{DD}$	–0.5 to V_{DD} + 0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} + 0.5	
Operating temperature	T_A			–40 to +110	˚C
Storage temperature	T_{stg}			–65 to +150	˚C

Notes 1. Pins other than the pins in **Note 2**.

2. Pins P70/ANI0-P77/ANI7, P80/ANI8-P87/ANI15

Caution **If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.**

Recommended Operating Conditions

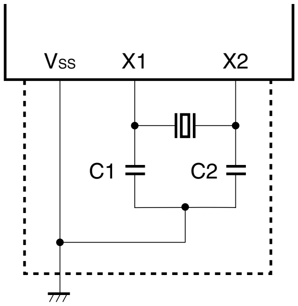
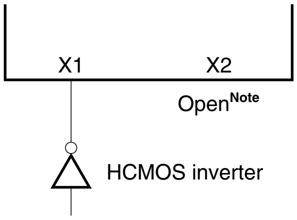
Oscillation Frequency	T_A	V_{DD}
8 MHz ≤ f_{XX} ≤ 20 MHz	–40 to +110 ˚C	4.5 to 5.5 V

Capacitance (T_A = 25 ˚C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz 0 V except measured pins			10	pF
Output capacitance	C_O				10	pF
I/O capacitance	C_{IO}				10	pF

(2) Electrical specifications of μPD784044(A1), 784046(A1) (2/6)

Oscillation Circuit Characteristics (T_A = –40 to +110 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Item	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillation frequency (f_{XX})	8	20	MHz
External clock		X1 input frequency (f_X)	8	20	MHz
		X1 input rise, fall time	0	5	ns
		X1 input high-, low-level width	20	105	ns

Note When the EXTC bit of the oscillation stabilization time specification register (OSTS) = 0. Input the reverse phase clock of the pin X1 to the pin X2 when the EXTC bit = 1.

Caution When using a system clock oscillation circuit, wire the portion enclosed by the dotted line in the diagram above as follows to prevent adverse influence from wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines. Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground potential for the capacitor in the oscillation circuit at the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not extract any signal from the oscillation circuit.**

(2) Electrical specifications of μPD784044(A1), 784046(A1) (3/6)

DC Characteristics (T_A = –40 to +110 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}			0		0.8	V
High-level input voltage	V_{IH1}	**Note 1**		2.2		V_{DD}	V
	V_{IH2}	**Note 2**		0.8 V_{DD}		V_{DD}	
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA				0.45	V
High-level output voltage	V_{OH}	I_{OH} = –400 μA		V_{DD} – 1.0			V
Input leakage current	I_{LI}	**Note 3**	0 V ≤ V_I ≤ V_{DD}			±10	μA
Analog pin input leakage current	I_{LIAN}	**Note 4**	0 V ≤ V_I ≤ AV_{DD}			±2	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operating mode (f_{XX} = 20 MHz)			30	60	mA
	I_{DD2}	HALT mode (f_{XX} = 20 MHz)			15	30	mA
	I_{DD3}	IDLE mode (f_{XX} = 20 MHz)			10	20	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	100	μA
			V_{DDDR} = 5 V ± 10 %		15	1000	μA
Pull-up resistor	R_L			15	40	80	kΩ

Notes 1. Pins other than pins in **Note 2**.

2. P20/NMI, P21/INTP0/TO00, P22/INTP1/TO01, P23/INTP2/TO02, P24/INTP3/TO03, P25/INTP4, P26/INTP5/TI2, P27/INTP6/TI3, P34/ASCK/$\overline{\text{SCK1}}$, P37/ASCK2/$\overline{\text{SCK2}}$, X1, X2, $\overline{\text{RESET}}$

3. Input and I/O pins (except X1 and X2, and P70/ANI0-P77/ANI7, P80/ANI8-P87/ANI15 used as analog inputs)

4. Pins P70/ANI0-P77/ANI7, P80/ANI8-P87/ANI15 (pins used as analog input, only during the non-sampling operation)

(2) Electrical specifications of μPD784044(A1), 784046(A1) (4/6)

AC Characteristics (T_A = –40 to +110 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Read/write operation

Parameter	Symbol	Expression	MIN.	MAX.	Unit
System clock cycle time	t_{CYK}		100	250	ns
Address setup time (vs. ASTB↓)	t_{SAST}	(0.5 + a) T – 20	30		ns
Address hold time (vs. ASTB↓)	t_{HSTA}	0.5T – 20	30		ns
ASTB high-level width	t_{WSTH}	(0.5 + a) T – 17	33		ns
Address→$\overline{\text{RD}}$↓ delay time	t_{DAR}	(1 + a) T – 15	85		ns
$\overline{\text{RD}}$↓→address float time	t_{FRA}			0	ns
Address→data input time	t_{DAID}	(2.5 + a + n) T – 56		194	ns
$\overline{\text{RD}}$↓→data input time	t_{DRID}	(1.5 + n) T – 53		97	ns
ASTB↓→$\overline{\text{RD}}$↓ delay time	t_{DSTR}	0.5T – 16	34		ns
Data hold time (vs. $\overline{\text{RD}}$↑)	t_{HRID}		0		ns
$\overline{\text{RD}}$↑→address active time	t_{DRA}	0.5T – 14	36		ns
$\overline{\text{RD}}$ low-level width	t_{WRL}	(1.5 + n) T – 30	120		ns
Address→$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓ delay time	t_{DAW}	(1 + a) T – 15	85		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→data output time	t_{DWOD}			15	ns
ASTB↓→$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓ delay time	t_{DSTW}	0.5T – 16	34		ns
Data setup time (vs. $\overline{\text{LWR}}$, $\overline{\text{HWR}}$↑)	t_{SODW}	(1.5 + n) T – 25	125		ns
Data hold time (vs. $\overline{\text{LWR}}$, $\overline{\text{HWR}}$↑)	t_{HWOD}	0.5T – 14	36		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↑→ ASTB↑ delay time	t_{DWST}	1.5T – 15	135		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$ low-level width	t_{WWL}	(1.5 + n) T – 36	114		ns
Address→$\overline{\text{WAIT}}$↓ input time	t_{DAWT}	(2 + a) T – 50		150	ns
ASTB↓→$\overline{\text{WAIT}}$↓ input time	t_{DSTWT}	1.5T – 40		110	ns
ASTB↓→$\overline{\text{WAIT}}$ hold time	t_{HSTWT}	(1.5 + n) T + 5	155		ns
ASTB↓→$\overline{\text{WAIT}}$↑ delay time	t_{DSTWTH}	(1.5 + n) T – 40		210**Note**	ns
$\overline{\text{RD}}$↓→$\overline{\text{WAIT}}$↓ input time	t_{DRWT}	T – 40		60	ns
$\overline{\text{RD}}$↓→$\overline{\text{WAIT}}$ hold time	t_{HRWT}	(1 + n) T + 5	105		ns
$\overline{\text{RD}}$↓→$\overline{\text{WAIT}}$↑ delay time	t_{DRWTH}	(1 + n) T – 40		160**Note**	ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→$\overline{\text{WAIT}}$↓ input time	t_{DWWT}	T – 40		60	ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→$\overline{\text{WAIT}}$ hold time	t_{HWWT}	(1 + n) T + 5	105		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→$\overline{\text{WAIT}}$↑ delay time	t_{DWWTH}	(1 + n) T – 40		160**Note**	ns

Note Specification when an external wait is inserted

Remarks
1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} is internal system clock frequency)
2. a = 1 when an address wait is inserted, otherwise, 0.
3. n indicates the number of the wait cycles by specifying the external wait pins ($\overline{\text{WAIT}}$) or programmable wait control registers 1, 2 (PWC1, PWC2). ($n \geq 0$. $n \geq 1$ for t_{DSTWTH}, t_{DRWTH}, t_{DWWTH}).
4. Calculate values in the expression column with the system clock cycle time to be used because these values depend on the system clock cycle time (t_{CYK} = T). The values in the above expression column are calculated based on T = 100 ns.

(2) Electrical specifications of μPD784044(A1), 784046(A1) (5/6)

Serial Operation (T_A = –40 to +110 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ output	BRG	T_{SFT}		ns
		$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ input	External clock	800		ns
Serial clock low-level width	t_{WSKL}	$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ output	BRG	$0.5T_{SFT}$–40		ns
		$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ input	External clock	360		ns
Serial clock high-level width	t_{WSKH}	$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ output	BRG	$0.5T_{SFT}$–40		ns
		$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ input	External clock	360		ns
SI1, SI2 setup time (vs. $\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$↑)	t_{SSSK}			80		ns
SI1, SI2 hold time (vs. $\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$↑)	t_{HSSK}			80		ns
$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$↓→SO1, SO2 output delay time	t_{DSBSK}	R = 1 kΩ, C = 100 pF		0	150	ns

Remarks 1. T_{SFT} is a value set in software. The minimum value is t_{CYK} × 8.

2. $t_{CYK} = 1/f_{CLK}$ (f_{CLK} is internal system clock frequency)

Other Operations (T_A = –40 to +110 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

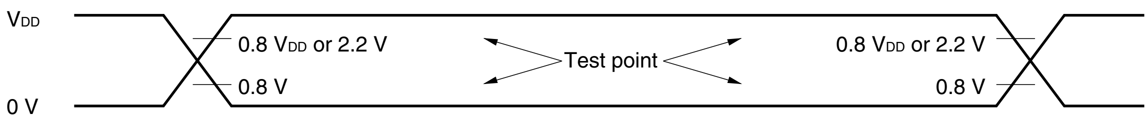
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI high, low-level width	t_{WNIH}, t_{WNIL}		10		μs
INTP0-INTP6 high, low-level width	t_{WITH}, t_{WITL}		4		t_{CYSMP}
TI2, TI3 high, low-level width	t_{WTIH}, t_{WTIL}		4		t_{CYSMP}
$\overline{\text{RESET}}$ high, low-level width	t_{WRSH}, t_{WRSL}		10		μs

Remarks 1. t_{CYSMP} is a sampling clock set in the noise protection control register (NPC) in software.
When NIn = 0, $t_{CYSMP} = t_{CYK}$
When NIn = 1, $t_{CYSMP} = t_{CYK} \times 4$

2. $t_{CYK} = 1/f_{CLK}$ (f_{CLK} is internal system clock frequency)

3. NIn: Bit n of NPC (n = 0-6)

AC Timing Test Point



(2) Electrical specifications of μPD784044(A1), 784046(A1) (6/6)

AD Converter Characteristics (T_A = –40 to +110 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V, $V_{DD} - 0.5\ V \leq AV_{DD} \leq V_{DD}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				10			bit
Total error[Note]		$4.5\ V \leq AV_{REF} \leq AV_{DD}$				±0.5	%FSR
		$3.4\ V \leq AV_{REF} < 4.5\ V$				±0.7	%FSR
Quantization error						±1/2	LSB
Conversion time	t_{CONV}			169			t_{CYK}
Sampling time	t_{SAMP}			20			t_{CYK}
Zero-scale error[Note]		$4.5\ V \leq AV_{REF} \leq AV_{DD}$			±1.5	±3.5	LSB
		$3.4\ V \leq AV_{REF} < 4.5\ V$			±1.5	±4.5	LSB
Full-scale error[Note]		$4.5\ V \leq AV_{REF} \leq AV_{DD}$			±1.5	±3.5	LSB
		$3.4\ V \leq AV_{REF} < 4.5\ V$			±1.5	±4.5	LSB
Nonlinearity error[Note]		$4.5\ V \leq AV_{REF} \leq AV_{DD}$			±1.5	±2.5	LSB
		$3.4\ V \leq AV_{REF} < 4.5\ V$			±1.5	±4.5	LSB
Analog input voltage	V_{IAN}			–0.3		AV_{REF}+0.3	V
A/D converter reference input voltage	AV_{REF}			3.4		AV_{DD}	V
AV_{REF} current	AI_{REF}				3.0	4.0	mA
AV_{DD} supply current	AI_{DD}				2.0	6.0	mA
A/D converter data retention current	AI_{DDDR}	STOP mode	AV_{DDDR} = 2.5 V		2	100	μA
			AV_{DDDR} = 5 V ± 10%		10	1000	μA

Note The quantization error is excluded.

Remark $t_{CYK} = 1/f_{CLK}$ (f_{CLK} is internal system clock frequency).

(3) Electrical specifications of μPD784044(A2), 784046(A2) (1/6)

Absolute Maximum Ratings (T_A = 25 ˚C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.5 to +7.0	V
	AV_{DD}			–0.5 to V_{DD} + 0.5	V
	AV_{SS}			–0.5 to +0.5	V
Input voltage	V_I	**Note 1**		–0.5 to $V_{DD} + 0.5 \le 7.0$	V
Output voltage	V_O			–0.5 to V_{DD} + 0.5	V
Low-level output current	I_{OL}	All output pins		15	mA
		Total of all output pins		150	mA
High-level output current	I_{OH}	All output pins		–10	mA
		Total of all output pins		–100	mA
Analog input voltage	V_{IAN}	**Note 2**	$AV_{DD} > V_{DD}$	–0.5 to V_{DD} + 0.5	V
			$V_{DD} \ge AV_{DD}$	–0.5 to AV_{DD} + 0.5	
A/D converter reference input voltage	AV_{REF}		$AV_{DD} > V_{DD}$	–0.5 to V_{DD} + 0.5	V
			$V_{DD} \ge AV_{DD}$	–0.5 to AV_{DD} + 0.5	
Operating temperature	T_A			–40 to +125	˚C
Storage temperature	T_{stg}			–65 to +150	˚C

Notes 1. Pins other than the pins in **Note 2**.

2. Pins P70/ANI0-P77/ANI7, P80/ANI8-P87/ANI15

Caution **If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.**

Recommended Operating Conditions

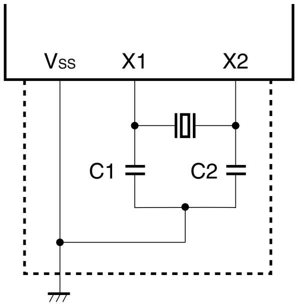
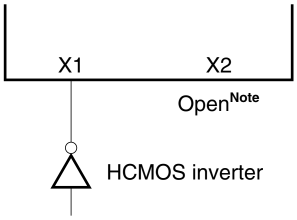
Oscillation Frequency	T_A	V_{DD}
8 MHz ≤ f_{XX} ≤ 20 MHz	–40 to +125 ˚C	4.5 to 5.5 V

Capacitance (T_A = 25 ˚C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz 0 V except measured pins			10	pF
Output capacitance	C_O				10	pF
I/O capacitance	C_{IO}				10	pF

(3) Electrical specifications of μPD784044(A2), 784046(A2) (2/6)

Oscillation Circuit Characteristics (T_A = –40 to +125 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Item	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillation frequency (f_{XX})	8	20	MHz
External clock		X1 input frequency (f_X)	8	20	MHz
		X1 input rise, fall time	0	5	ns
		X1 input high-, low-level width	20	105	ns

Note When the EXTC bit of the oscillation stabilization time specification register (OSTS) = 0. Input the reverse phase clock of the pin X1 to the pin X2 when the EXTC bit = 1.

Caution When using a system clock oscillation circuit, wire the portion enclosed by the dotted line in the diagram above as follows to prevent adverse influence from wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines. Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground potential for the capacitor in the oscillation circuit at the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not extract any signal from the oscillation circuit.**

(3) Electrical specifications of μPD784044(A2), 784046(A2) (3/6)

DC Characteristics (T_A = –40 to +125 °C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}			0		0.8	V
High-level input voltage	V_{IH1}	**Note 1**		2.2		V_{DD}	V
	V_{IH2}	**Note 2**		0.8 V_{DD}		V_{DD}	
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA				0.45	V
High-level output voltage	V_{OH}	I_{OH} = –400 μA		V_{DD} – 1.0			V
Input leakage current	I_{LI}	**Note 3**	0 V ≤ V_I ≤ V_{DD}			±10	μA
Analog pin input leakage current	I_{LIAN}	**Note 4**	0 V ≤ V_I ≤ AV_{DD}			±2	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operating mode (f_{XX} = 20 MHz)			30	60	mA
	I_{DD2}	HALT mode (f_{XX} = 20 MHz)			15	30	mA
	I_{DD3}	IDLE mode (f_{XX} = 20 MHz)			10	20	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	100	μA
			V_{DDDR} = 5 V ± 10 %		15	1000	μA
Pull-up resistor	R_L			15	40	80	kΩ

Notes 1. Pins other than pins in **Note 2**.

2. P20/NMI, P21/INTP0/TO00, P22/INTP1/TO01, P23/INTP2/TO02, P24/INTP3/TO03, P25/INTP4, P26/INTP5/TI2, P27/INTP6/TI3, P34/ASCK/$\overline{\text{SCK1}}$, P37/ASCK2/$\overline{\text{SCK2}}$, X1, X2, $\overline{\text{RESET}}$

3. Input and I/O pins (except X1 and X2, and P70/ANI0-P77/ANI7, P80/ANI8-P87/ANI15 used as analog inputs)

4. Pins P70/ANI0-P77/ANI7, P80/ANI8-P87/ANI15 (pins used as analog input, only during the non-sampling operation)

(3) Electrical specifications of μPD784044(A2), 784046(A2) (4/6)

AC Characteristics (T_A = –40 to +125 °C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Read/write operation

Parameter	Symbol	Expression	MIN.	MAX.	Unit
System clock cycle time	t_{CYK}		100	250	ns
Address setup time (vs. ASTB↓)	t_{SAST}	(0.5 + a) T – 20	30		ns
Address hold time (vs. ASTB↓)	t_{HSTA}	0.5T – 20	30		ns
ASTB high-level width	t_{WSTH}	(0.5 + a) T – 17	33		ns
Address→$\overline{\text{RD}}$↓ delay time	t_{DAR}	(1 + a) T – 15	85		ns
$\overline{\text{RD}}$↓→address float time	t_{FRA}			0	ns
Address→data input time	t_{DAID}	(2.5 + a + n) T – 56		194	ns
$\overline{\text{RD}}$↓→data input time	t_{DRID}	(1.5 + n) T – 53		97	ns
ASTB↓→$\overline{\text{RD}}$↓ delay time	t_{DSTR}	0.5T – 16	34		ns
Data hold time (vs. $\overline{\text{RD}}$↑)	t_{HRID}		0		ns
$\overline{\text{RD}}$↑→address active time	t_{DRA}	0.5T – 14	36		ns
$\overline{\text{RD}}$ low-level width	t_{WRL}	(1.5 + n) T – 30	120		ns
Address→$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓ delay time	t_{DAW}	(1 + a) T – 15	85		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→data output time	t_{DWOD}			15	ns
ASTB↓→$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓ delay time	t_{DSTW}	0.5T – 16	34		ns
Data setup time (vs. $\overline{\text{LWR}}$, $\overline{\text{HWR}}$↑)	t_{SODW}	(1.5 + n) T – 25	125		ns
Data hold time (vs. $\overline{\text{LWR}}$, $\overline{\text{HWR}}$↑)	t_{HWOD}	0.5T – 14	36		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↑→ ASTB↑ delay time	t_{DWST}	1.5T – 15	135		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$ low-level width	t_{WWL}	(1.5 + n) T – 36	114		ns
Address→$\overline{\text{WAIT}}$↓ input time	t_{DAWT}	(2 + a) T – 50		150	ns
ASTB↓→$\overline{\text{WAIT}}$↓ input time	t_{DSTWT}	1.5T – 40		110	ns
ASTB↓→$\overline{\text{WAIT}}$ hold time	t_{HSTWT}	(1.5 + n) T + 5	155		ns
ASTB↓→$\overline{\text{WAIT}}$↑ delay time	t_{DSTWTH}	(1.5 + n) T – 40		210[Note]	ns
$\overline{\text{RD}}$↓→$\overline{\text{WAIT}}$↓ input time	t_{DRWT}	T – 40		60	ns
$\overline{\text{RD}}$↓→$\overline{\text{WAIT}}$ hold time	t_{HRWT}	(1 + n) T + 5	105		ns
$\overline{\text{RD}}$↓→$\overline{\text{WAIT}}$↑ delay time	t_{DRWTH}	(1 + n) T – 40		160[Note]	ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→$\overline{\text{WAIT}}$↓ input time	t_{DWWT}	T – 40		60	ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→$\overline{\text{WAIT}}$ hold time	t_{HWWT}	(1 + n) T + 5	105		ns
$\overline{\text{LWR}}$, $\overline{\text{HWR}}$↓→$\overline{\text{WAIT}}$↑ delay time	t_{DWWTH}	(1 + n) T – 40		160[Note]	ns

Note Specification when an external wait is inserted

Remarks

1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} is internal system clock frequency)
2. a = 1 when an address wait is inserted, otherwise, 0.
3. n indicates the number of the wait cycles by specifying the external wait pins ($\overline{\text{WAIT}}$) or programmable wait control registers 1, 2 (PWC1, PWC2). (n ≥ 0. n ≥ 1 for t_{DSTWTH}, t_{DRWTH}, t_{DWWTH}).
4. Calculate values in the expression column with the system clock cycle time to be used because these values depend on the system clock cycle time (t_{CYK} = T). The values in the above expression column are calculated based on T = 100 ns.

(3) Electrical specifications of μPD784044(A2), 784046(A2) (5/6)

Serial Operation (T_A = –40 to +125 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	$\overline{\mathrm{SCK1}}$, $\overline{\mathrm{SCK2}}$ output	BRG	T_{SFT}		ns
		$\overline{\mathrm{SCK1}}$, $\overline{\mathrm{SCK2}}$ input	External clock	800		ns
Serial clock low-level width	t_{WSKL}	$\overline{\mathrm{SCK1}}$, $\overline{\mathrm{SCK2}}$ output	BRG	$0.5T_{SFT}$–40		ns
		$\overline{\mathrm{SCK1}}$, $\overline{\mathrm{SCK2}}$ input	External clock	360		ns
Serial clock high-level width	t_{WSKH}	$\overline{\mathrm{SCK1}}$, $\overline{\mathrm{SCK2}}$ output	BRG	$0.5T_{SFT}$–40		ns
		$\overline{\mathrm{SCK1}}$, $\overline{\mathrm{SCK2}}$ input	External clock	360		ns
SI1, SI2 setup time (vs. $\overline{\mathrm{SCK1}}$, $\overline{\mathrm{SCK2}}$↑)	t_{SSSK}			80		ns
SI1, SI2 hold time (vs. $\overline{\mathrm{SCK1}}$, $\overline{\mathrm{SCK2}}$↑)	t_{HSSK}			80		ns
$\overline{\mathrm{SCK1}}$, $\overline{\mathrm{SCK2}}$↓→SO1, SO2 output delay time	t_{DSBSK}	R = 1 kΩ, C = 100 pF		0	150	ns

Remarks 1. T_{SFT} is a value set in software. The minimum value is $t_{CYK} \times 8$.

2. $t_{CYK} = 1/f_{CLK}$ (f_{CLK} is internal system clock frequency)

Other Operations (T_A = –40 to +125 ˚C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

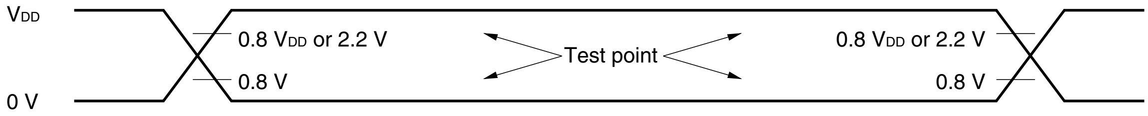
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI high, low-level width	t_{WNIH}, t_{WNIL}		10		μs
INTP0-INTP6 high, low-level width	t_{WITH}, t_{WITL}		4		t_{CYSMP}
TI2, TI3 high, low-level width	t_{WTIH}, t_{WTIL}		4		t_{CYSMP}
$\overline{\mathrm{RESET}}$ high, low-level width	t_{WRSH}, t_{WRSL}		10		μs

Remarks 1. t_{CYSMP} is a sampling clock set in the noise protection control register (NPC) in software.
When NIn = 0, $t_{CYSMP} = t_{CYK}$
When NIn = 1, $t_{CYSMP} = t_{CYK} \times 4$

2. $t_{CYK} = 1/f_{CLK}$ (f_{CLK} is internal system clock frequency)

3. NIn: Bit n of NPC (n = 0-6)

AC Timing Test Point



(3) Electrical specifications of μPD784044(A2), 784046(A2) (6/6)

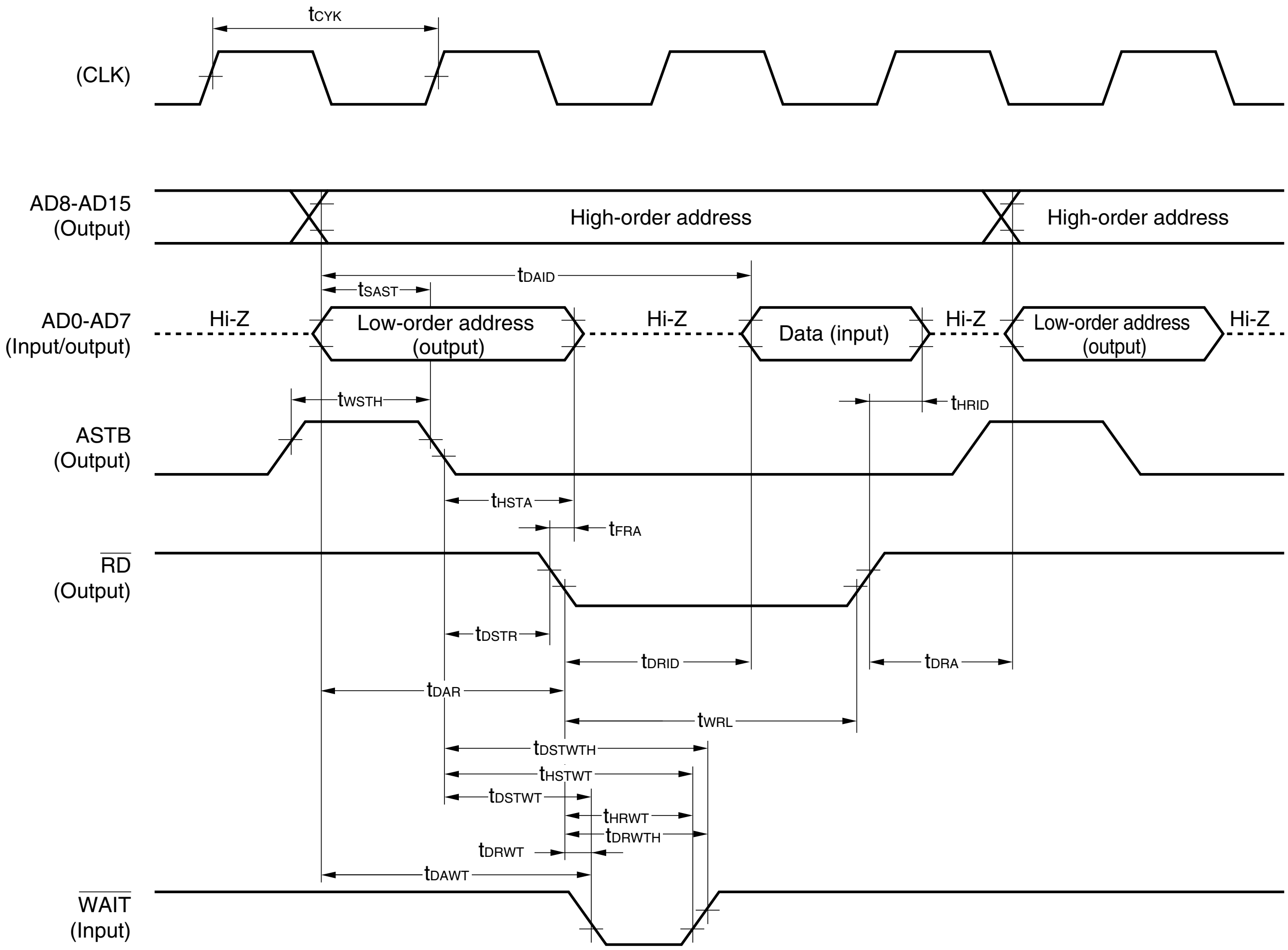
AD Converter Characteristics (T_A = –40 to +125 °C, V_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{DD} – 0.5 V ≤ AV_{DD} ≤ V_{DD})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				10			bit
Total error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD}				±0.5	%FSR
		3.4 V ≤ AV_{REF} < 4.5 V				±0.7	%FSR
Quantization error						±1/2	LSB
Conversion time	t_{CONV}			169			t_{CYK}
Sampling time	t_{SAMP}			20			t_{CYK}
Zero-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±3.5	LSB
		3.4 V ≤ AV_{REF} < 4.5 V			±1.5	±4.5	LSB
Full-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±3.5	LSB
		3.4 V ≤ AV_{REF} < 4.5 V			±1.5	±4.5	LSB
Nonlinearity error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} < 4.5 V			±1.5	±4.5	LSB
Analog input voltage	V_{IAN}			–0.3		AV_{REF}+0.3	V
A/D converter reference input voltage	AV_{REF}			3.4		AV_{DD}	V
AV_{REF} current	AI_{REF}				3.0	4.0	mA
AV_{DD} supply current	AI_{DD}				2.0	6.0	mA
A/D converter data retention current	AI_{DDDR}	STOP mode	AV_{DDDR} = 2.5 V		2	100	μA
			AV_{DDDR} = 5 V ± 10%		10	1000	μA

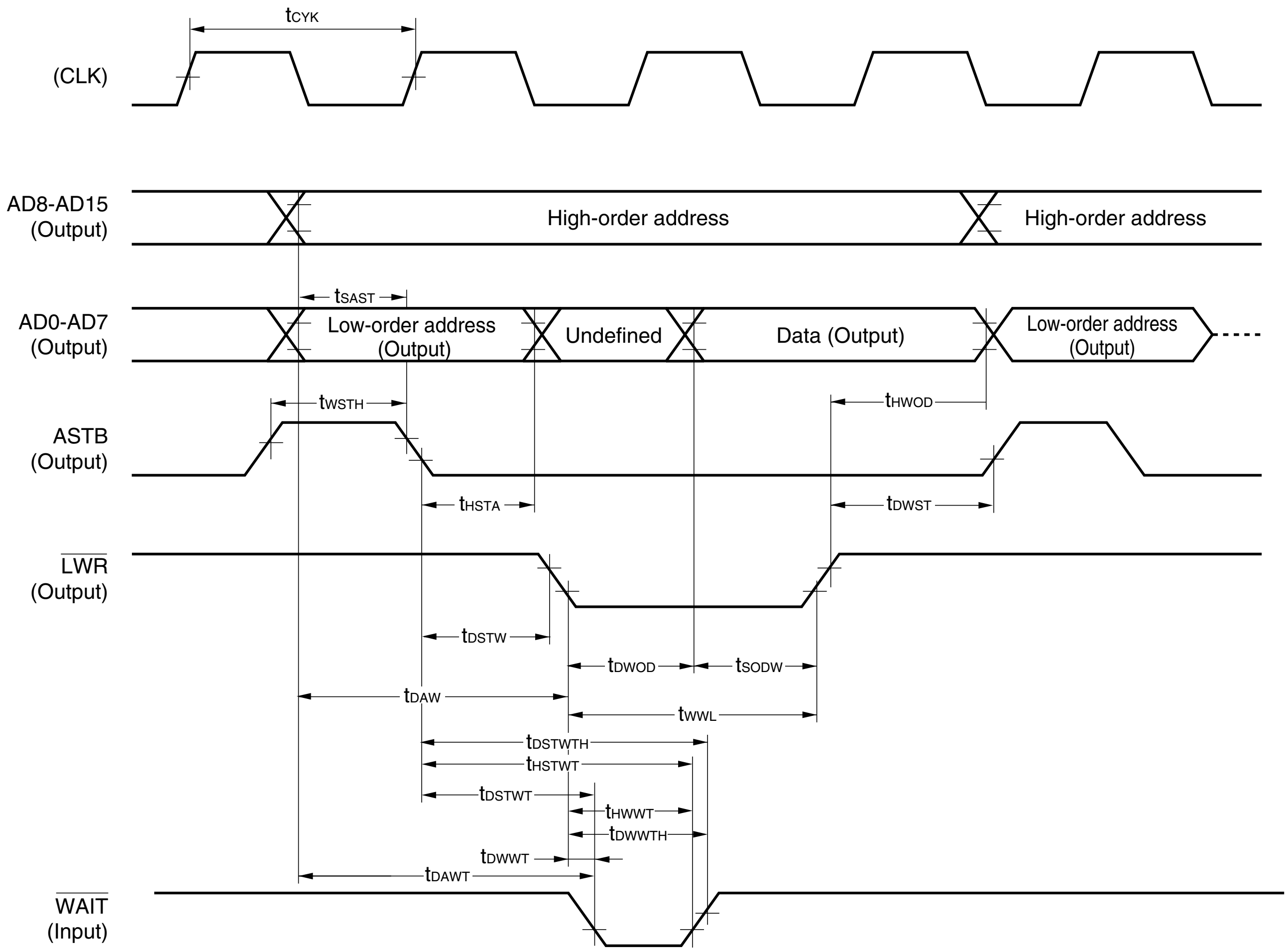
Note The quantization error is excluded.

Remark t_{CYK} = 1/f_{CLK} (f_{CLK} is internal system clock frequency).

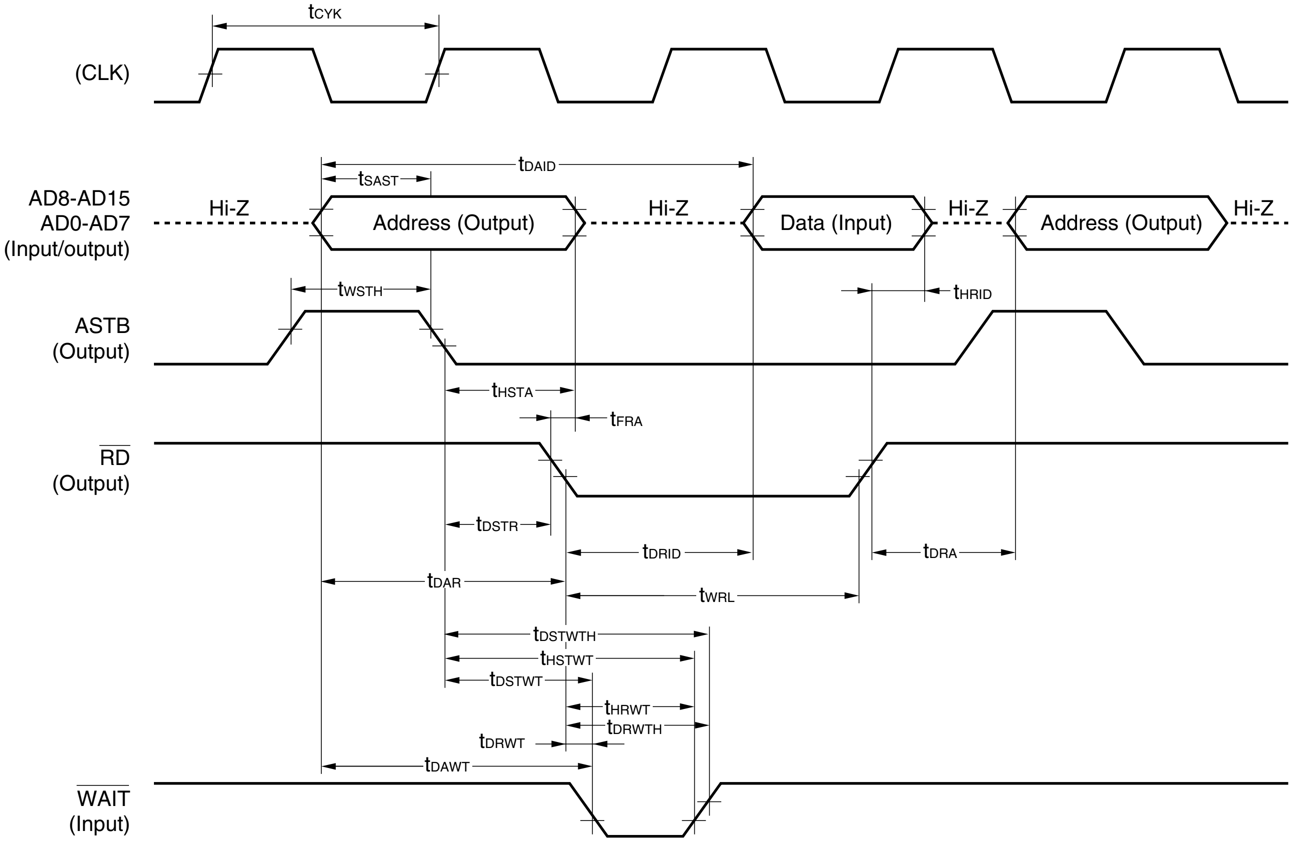
Read Operation (8 bits)



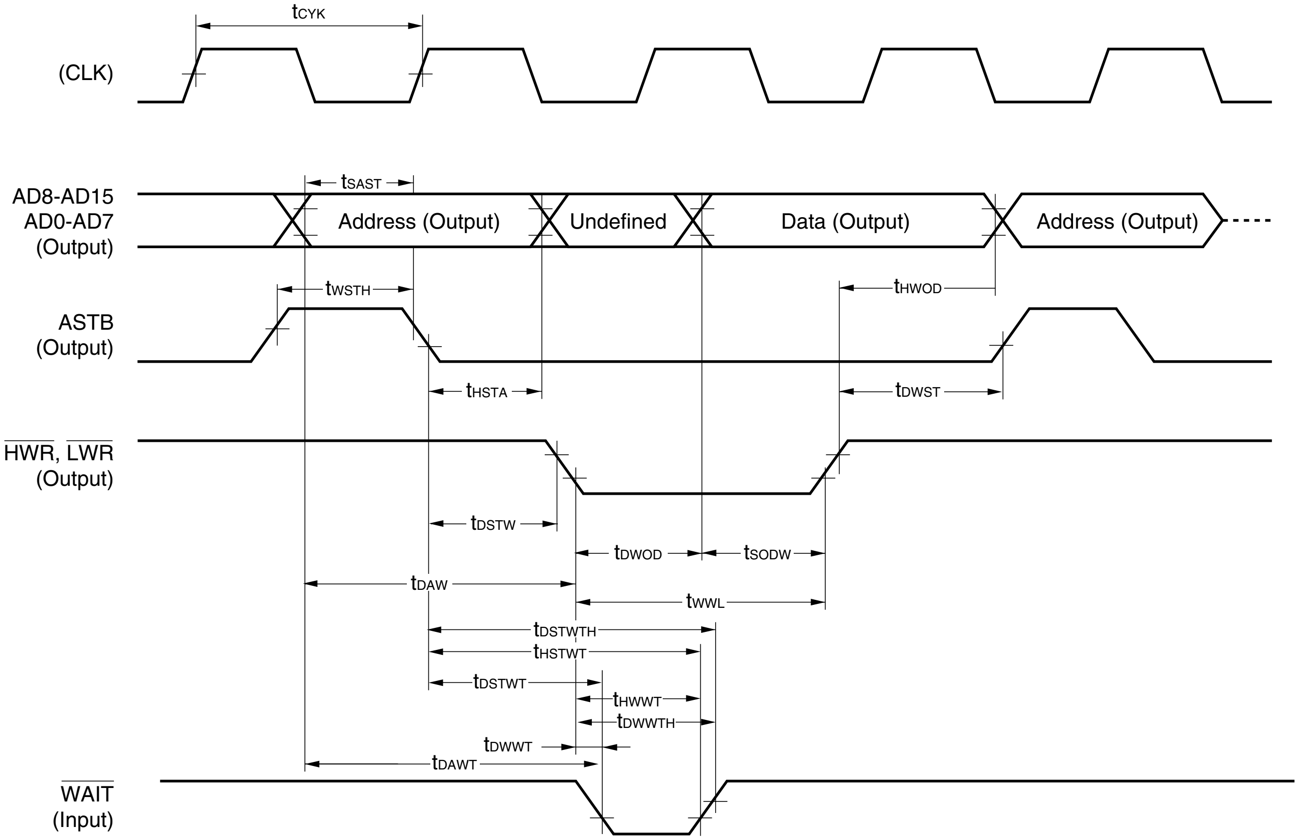
Write Operation (8 bits)



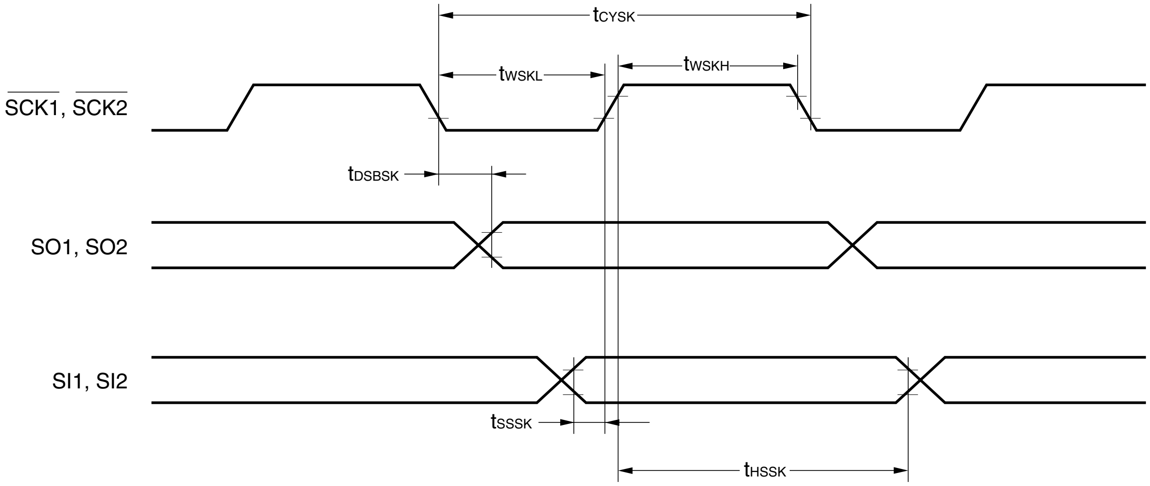
Read Operation (16 bits)



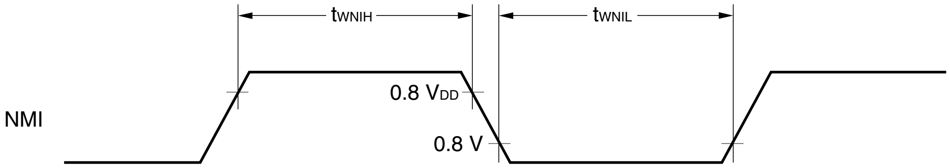
Write Operation (16 bits)

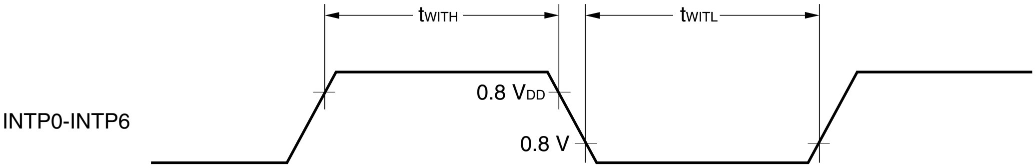


Serial Operation

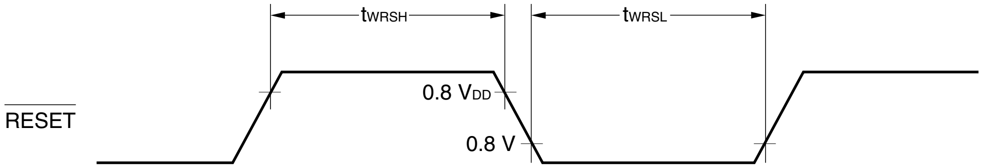


Interrupt Input Timing

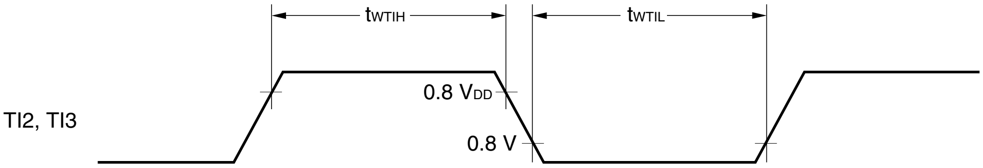




Reset Input Timing

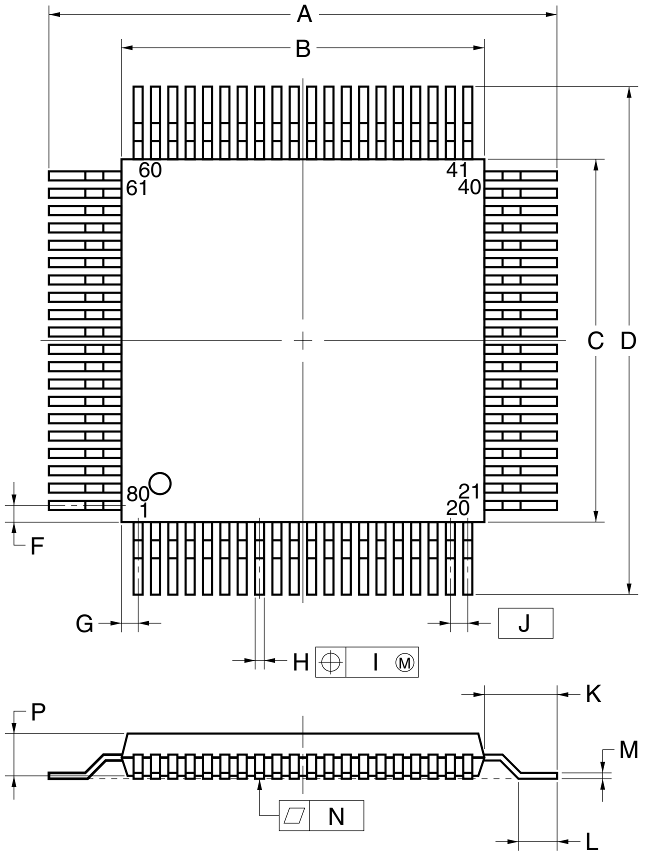


Timer Input Timing

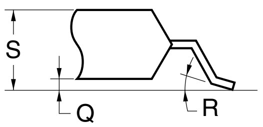


14. PACKAGE DRAWING

80 PIN PLASTIC QFP (14x14)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-5

Remark The package dimensions and materials of ES versions are the same as those of mass-production versions.

15. RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the conditions recommended below.

For details of soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, please contact your NEC representative.

Table 15-1. Surface-Mount Type Soldering Conditions

μPD784044GC(A)-×××-3B9 : 80-pin plastic QFP (14 × 14 mm)
μPD784044GC(A1)-×××-3B9 : 80-pin plastic QFP (14 × 14 mm)
μPD784044GC(A2)-×××-3B9 : 80-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 ˚C, Time: 30 sec. max. (210 ˚C min.), Number of times: 3 max.	IR35-00-3
Partial heating	Pin temterature: 300 ˚C max., 3 sec. max. (per side of device)	–

Caution The μPD784046(A), (A1), and (A2) are under development. Therefore, the soldering conditions for the μPD784046(A), (A1), and (A2) are undefined.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD784046(A).
Refer to **(5) Cautions when the development tools are used.**

(1) Language processing software

RA78K4	78K/IV series common assembler package
CC78K4	78K/IV series common C compiler package
DF784046	Device file for the μPD784046 subseries
CC78K4-L	78K/IV series common C compiler library source file

(2) Flash memory writing tools

Flashpro II (Part number: FL-PR2)	Dedicated flash programmer for microcomputers incorporating flash memory
FA-80GC	Adapter for flash memory writing

(3) Debugging tools

- **When using the IE-78K4-NS in-circuit emulator**

IE-78K4-NS**Note**	78K/IV series common in-circuit emulator
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
IE-70000-98-IF-C**Note**	Interface adapter necessary when a PC-9800 series computer (except notebook-type personal computer) is used as host machine
IE-70000-CD-IF**Note**	PC card and interface cable necessary when a PC-9800 series notebook-type personal computer is used as host machine
IE-70000-PC-IF-C**Note**	Interface adapter necessary when an IBM PC/AT™ or a compatible machine is used as host machine
IE-784046-NS-EM1**Note**	Emulation board for emulating the μPD784046 subseries
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-3B9 type)
EV-9200GC-80	Socket to be mounted on the board of the target system for 80-pin plastic QFP (GC-3B9 type)
ID78K4-NS**Note**	Integrated debugger for IE-78K4-NS
SM78K4	78K/IV series common system simulator
DF784046	Device file for the μPD784046 subseries

Note Under development

- **When using the IE-784000-R in-circuit emulator**

IE-784000-R	78K/IV series common in-circuit emulator
IE-70000-98-IF-B IE-70000-98-IF-C^Note^	Interface adapter necessary when a PC-9800 series computer (except notebook-type personal computer) is used as host machine
IE-70000-98N-IF	Interface adapter and cable necessary when a PC-9800 series notebook-type personal computer is used as host machine
IE-70000-PC-IF-B IE-70000-PC-IF-C^Note^	Interface adapter necessary when an IBM PC/AT or a compatible machine is used as host machine
IE-78000-R-SV3	Interface adapter and cable necessary when an EWS is used as host machine
IE-784000-R-EM	78K/IV series common emulation board
IE-784046-NS-EM1^Note^ IE-784046-R-EM1	Emulation board for emulating the μPD784046 subseries
IE78K4-R-EX2^Note^	Emulation probe conversion board necessary when the IE-784046-NS-EM1 is used in the IE-784000-R. Not necessary when the IE-784046-R-EM1 is used.
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-3B9 type)
EV-9200GC-80	Socket to be mounted on the board of the target system made for the 80-pin plastic QFP (GC-3B9 type)
ID78K4	Integrated debugger for IE-784000-R
SM78K4	78K/IV series common system simulator
DF784046	Device file for the μPD784046 subseries

Note Under development

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV series
MX78K4	OS for 78K/IV series

(5) Cautions when the development tools are used

- The ID-78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784046.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 and DF784046.
- Flashpro II, FA-80GC, and NP-80GC are product of Naito Densei Machida Mfg. Co., Ltd. (TEL: (044)822-3813). Contact an NEC distributor when purchasing these products.
- Host machines and OSs compatible with the software are as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 Series [Windows™] IBM PC/AT and compatible machines [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	○Note	○
CC78K4	○Note	○
ID78K4-NS	○	–
ID78K4	○	○
SM78K4	○	–
RX78K/IV	○Note	○
MX78K4	○Note	○

Note DOS based software

APPENDIX B. RELATED DOCUMENTS

Device-related documents

Document Name	Document No.
μPD784044(A), 784046(A) Data Sheet	This document
μPD78F4046 Preliminary Product Information	U11447E
μPD784046 Subseries User's Manual - Hardware	U11515E
78K/IV Series User's Manual - Instruction	U10905E
78K/IV Series Application Note - Software Basics	U10095E

Development tool-related documents (User's Manuals)

Document Name		Document No.
RA78K4 Assembler Package	Operation	U11334E
	Language	U11162E
	Structured Assembler Preprocessor	U11743E
CC78K4 C Compiler	Operation	U11572E
	Language	U11571E
IE-78K4-NS		U13356E
IE-784000-R		U12903E
IE-784046-NS-EM1		U13744E
IE-784046-R-EM1		U11677E
EP-78230		EEU-1515
SM78K4 System Simulator Windows Based	Reference	U10093E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E
ID78K4-NS Integrated Debugger	Reference	U12796E
ID78K4 Integrated Debugger Windows Based	Reference	U10440E

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of the document when designing your system.

Embedded software-related documents (User's Manual)

Document Name		Document No.
78K/IV Series Real-Time OS	Fundamental	U10603E
	Installation	U10604E
78K/IV Series OS, MX78K4	Fundamental	U11779E

Other documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability and Quality Control	C10983E
Guide to Prevent Damages for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of the document when designing your system.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-3067-5800
Fax: 01-3067-5899

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Madrid Office
Madrid, Spain
Tel: 091-504-2787
Fax: 091-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
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Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
Novena Square, Singapore
Tel: 253-8311
Fax: 250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Guarulhos-SP, Brasil
Tel: 11-6462-6810
Fax: 11-6462-6829

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Some of related document may be preliminary, but is not marked as such. Please keep this in mind as you refer to this information

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