U62H824PA

Automotive Fast 8K x 24 SRAM

Features

- 196 608 bit static CMOS RAM
- 35 ns Access Time
- Fully static Read and Write operations
- Equal address and chip enable access times
- Single bit on-chip address multiplexer
- Active high and active low chip enable inputs
- Output enable controlled three-state outputs
- TTL/CMOS-compatible
- Low power standby mode
- Power supply voltage 5 V
- Operating temperature range
  -40 °C to 125 °C
- CECC 90000 Quality Standard
- ESD protection > 2000 V
  (MIL STD 883C M3015.7)
- Latch-up immunity > 100 mA
- Package: PLCC52

Description

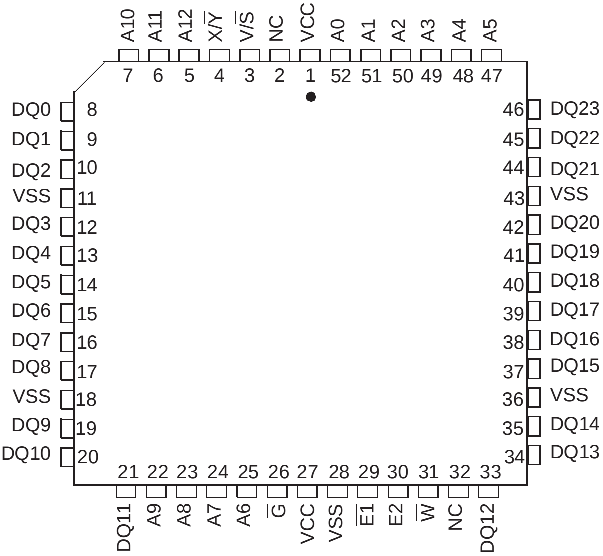
The U62H824PA is a static RAM manufactured using a CMOS process technology. The device integrates an 8K x 24 SRAM core with multiple chip enable inputs, output enable, and an externally controlled single address pin multiplexer. These functions allow for direct connection to the Motorola DSP56k Digital Signal Processor Family and provide a very efficient means for implementation of a reduced parts count system requiring no additional interface logic. The avialability of multiple chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) inputs provides for greater system flexibility when multiple devices are used. With either chip enable unasserted, the device will enter standby mode, useful in low-power applications. A single on-chip multiplexer selects A12 or X/$\overline{Y}$ as the highest order address input depending upon the state of the V/$\overline{S}$ control input. This feature allows one physical static RAM component to efficiently store program and vector or scalar operands by dynamically re-partitioning the RAM array.

Typical applications will logically map vector operands into upper memory with scalar operands being stored in lower memory.

An application example is at the end of this document for additional information.

Multiple power and ground pins have been utilized to minimize effectes induced by output noice.

Pin Configuration

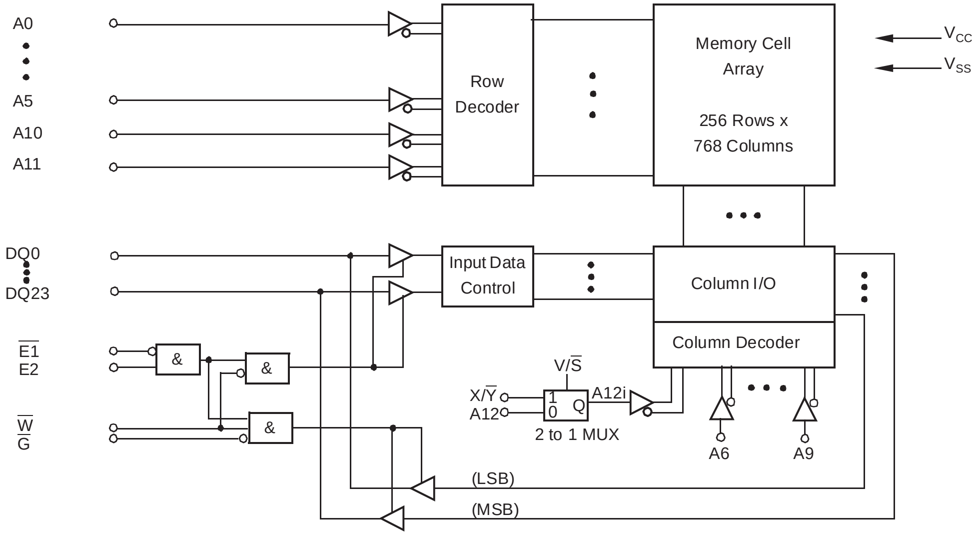


Pin Description

Signal Name	Signal Description
A0 - A11	Address Inputs
A12, X/$\overline{Y}$	Multiplexed Address
V/$\overline{S}$	Address Multiplexer Control
DQ0 - DQ23	Data Input / Output
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground
NC	Not Connected

For proper operation of the device, all V_{SS} pins must be connected to ground.

Block Diagram



Truth Table

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	V/$\overline{S}$	Mode	Supply Current	I/O Status
H	X	X	X	X	Not Selected	$I_{CC(SB)}$	High - Z
X	L	X	X	X	Not Selected	$I_{CC(SB)}$	High - Z
L	H	H	H	X	Output Disable	$I_{CC(OP)}$	High - Z
L	H	L	H	H	Read Using X/$\overline{Y}$	$I_{CC(OP)}$	Data Out
L	H	L	H	L	Read Using A12	$I_{CC(OP)}$	Data Out
L	H	X	L	H	Write Using X/$\overline{Y}$	$I_{CC(OP)}$	Data In
L	H	X	L	L	Write Using A12	$I_{CC(OP)}$	Data In

Characteristics

All voltages are referenced to V_{SS} = 0 V (ground).
All characteristics are valid in the power supply voltage range and in the operating temperature range specified.
Dynamic measurements are based on a rise and fall time of ≤ 5 ns, measured between 10 % and 90 % of V_I, as well as input levels of V_{IL} = 0 V and V_{IH} = 3 V. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis}-times and t_{en}-times, in which cases transition is measured ± 200 mV from steady-state voltage.

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V_{CC}		4.5	5.5	V
Input Low Voltage *	V_{IL}		-0.3	0.8	V
Input High Voltage	V_{IH}		2.2	V_{CC} + 0.3	V

* -2 V at Pulse Width ≤ 10 ns

Maximum Ratings	**Symbol**	**Min.**	**Max.**	**Unit**
Power Supply Voltage	V_{CC}	-0.5	7	V
Input Voltage	V_I	-0.5	V_{CC} + 0.5	V
Output Voltage	V_O	-0.5	V_{CC} + 0.5	V
Power Dissipation	P_D	-	1.75	W
Operating Temperature	T_a	-40	125	°C
Storage Temperature	T_{stg}	-65	150	°C
Output Short-Circuit Current at V_{CC} = 5 V and V_O = 0 V**	$\|I_{OS}\|$		20	mA

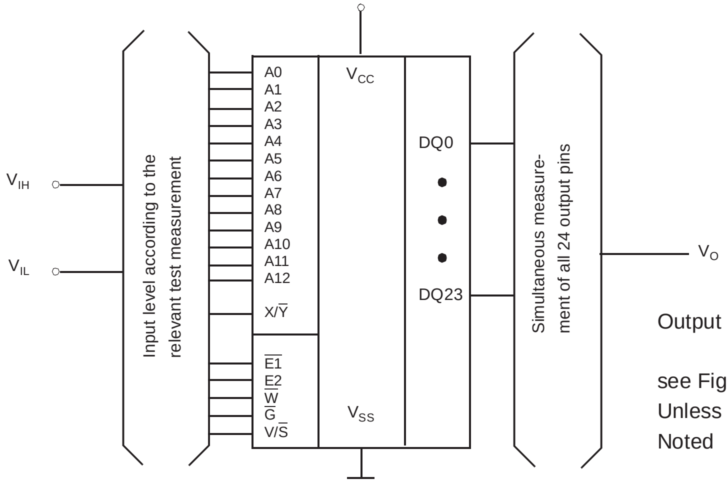
** Not more than 1 output should be shorted at the same time. Duration of the short circuit should not execeed 30 s.

Electrical Characteristics	**Symbol**	**Conditions**	**Min.**	**Max.**	**Unit**
Supply Current - Operating Mode	$I_{CC(OP)}$	V_{CC} = 5.5 V $V_{\overline{E1}}$ = 0.8 V V_{E2} = 2.2 V $V_{\overline{G}}$ = 2.2 V other inputs = V_{IL} or V_{IH} I_{out} = 0 mA t_{cW} = 35 ns		180	mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	V_{CC} = 5.5 V $V_{\overline{E1}}$ = V_{CC} - 0.2 V V_{E2} = 0.2 V all inputs ≥ V_{CC} - 0.2 V or ≤ 0.2 V		10	mA
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)1}$	V_{CC} = 5.5 V $V_{\overline{E1}}$ = 2.2 V V_{E2} = 0.8 V all inputs = V_{IH} or V_{IL}		15	mA
Output High Voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = -4.0 mA	2.4		V
Output Low Voltage	V_{OL}	I_{OL} = 8.0 mA		0.4	V
Input High Leakage Current	I_{IH}	V_{CC} = 5.5 V V_{IH} = 5.5 V		2	µA
Input Low Leakage Current	I_{IL}	V_{IL} = 0 V	-2		µA
Output High Current	I_{OH}	V_{CC} = 4.5 V V_{OH} = 2.4 V		-4	mA
Output Low Current	I_{OL}	V_{OL} = 0.4 V	8		mA
Output Leakage Current					
High at Three-State Outputs	I_{OHZ}	V_{CC} = 5.5 V V_{OH} = 5.5 V		2	µA
Low at Three-State Outputs	I_{OLZ}	V_{OL} = 0 V $V_{\overline{G}}$ = V_{IH}	-2		µA

Switching Characteristics Read Cycle	**Symbol**		**35**		**Unit**
	Alt.	**IEC**	**Min.**	**Max.**	
Read Cycle Time	t_{RC}	t_{cR}	35		ns
Address Access Time to Data Valid	t_{AA}	$t_{a(A)}$		35	ns
MUX Control to Data Valid		$t_{a(VS)}$		35	
Chip Enable Access Time to Data Valid	t_{ACE}	$t_{a(E)}$		35	ns
$\overline{G}$ LOW to Data Valid	t_{OE}	$t_{a(G)}$		15	ns
Output Hold Time from Address Change	t_{OH}	$t_{v(A)}$	5		ns
Output Hold Time from MUX Control Change		$t_{v(VS)}$	5		ns
$\overline{E1}$ LOW or E2 HIGH to Output in Low-Z	t_{LZCE}	$t_{en(E)}$	0		ns
$\overline{G}$ LOW to Output in Low-Z	t_{LZOE}	$t_{en(G)}$	0		ns
$\overline{E1}$ HIGH or E2 LOW to Output in High-Z	t_{HZCE}	$t_{dis(E)}$		15	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$		15	ns

Switching Characteristics Write Cycle	**Symbol**		**35**		**Unit**
	Alt.	**IEC**	**Min.**	**Max.**	
Write Cycle Time	t_{WC}	t_{cW}	35		ns
Write Pulse Width	t_{WP}	$t_{w(W)}$	20		ns
Write Pulse Width Setup Time	t_{WP}	$t_{su(W)}$	20		ns
Address Setup Time	t_{AS}	$t_{su(A)}$	0		ns
MUX Control Setup Time		$t_{su(VS)}$	0		ns
Address Valid to End of Write	t_{AW}	$t_{su(A-WH)}$	30		ns
MUX Control Valid to End of Write		$t_{su(VS-WH)}$	30		ns
Adress Valid to End of Write		$t_{su(A-E)}$	30		ns
MUX Control Valid to End of Write		$t_{su(VS-E)}$	30		ns
Chip Enable Setup Time	t_{CW}	$t_{su(E)}$	20		ns
Pulse Width Chip Enable	t_{CW}	$t_{w(E)}$	20		ns
Data Setup Time	t_{DS}	$t_{su(D)}$	15		ns
Data Hold Time	t_{DH}	$t_{h(D)}$	0		ns
Address Hold from End of Write	t_{AH}	$t_{h(A)}$	0		ns
MUX Control from End of Write		$t_{h(VS)}$	0		ns
$\overline{W}$ HIGH to Output in Low-Z	t_{LZWE}	$t_{en(W)}$	5		ns
$\overline{W}$ LOW to Output in High-Z	t_{HZWE}	$t_{dis(W)}$		15	ns

Test Configuration for Functional Check



Output Load

see Figure 1A
Unless Otherwide
Noted

AC Test Loads

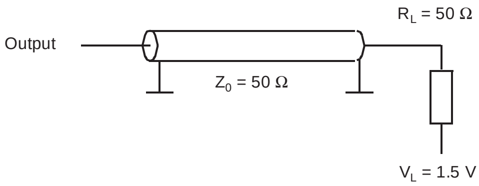


Figure 1A

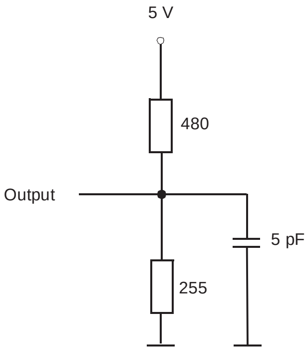


Figure 1B

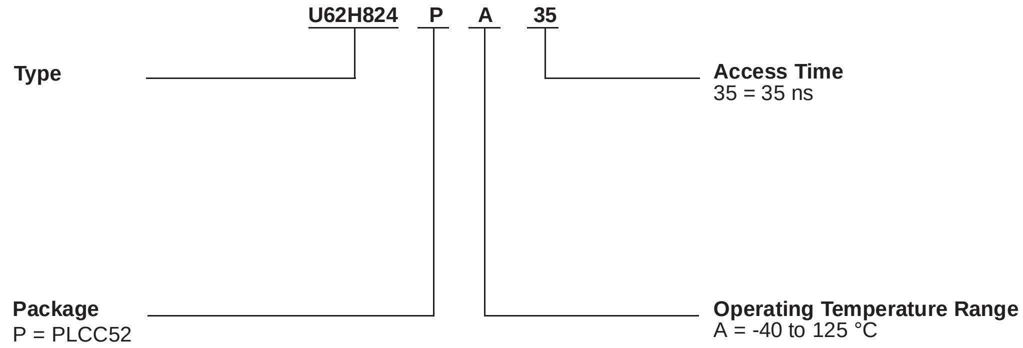
Measurement of $t_{dis(E)}$, $t_{dis(W)}$, $t_{dis(G)}$, $t_{en(E)}$, $t_{en(W)}$, $t_{en(G)}$ with Output Load from Figure 1B.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	V_{CC} = 5.0 V V_I = V_{SS} f = 1 MHz T_a = 25 °C	C_I		6	pF
Output Capacitance		C_0		8	pF

All pins not under test must be connected with ground by capacitors.

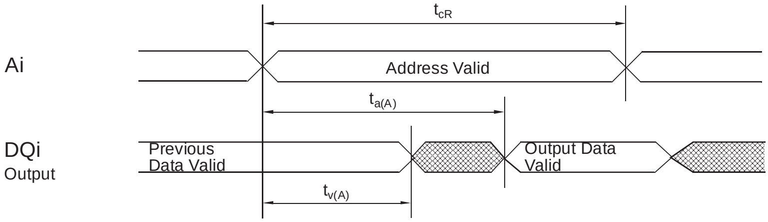
IC Code Numbers

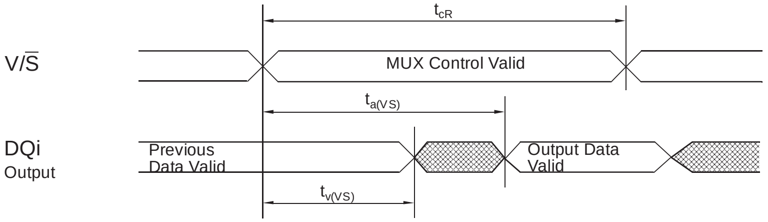
Example



The date of manufacture is given by the last 4 digits of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.

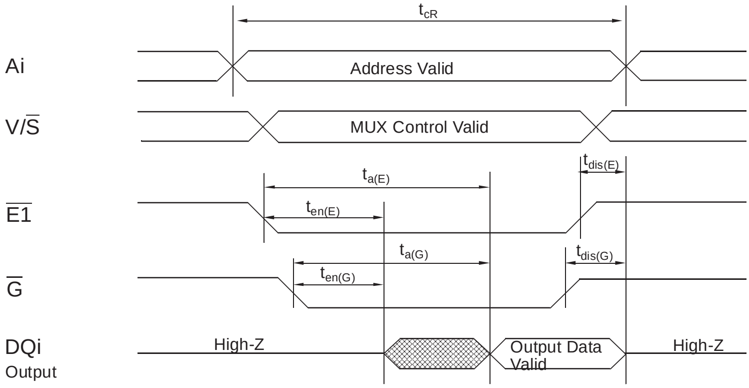
Read Cycle 1: Ai- or V/$\overline{S}$-controlled (during Read Cycle: $\overline{E1} = \overline{G} = V_{IL}$, $E2 = \overline{W} = V_{IH}$)





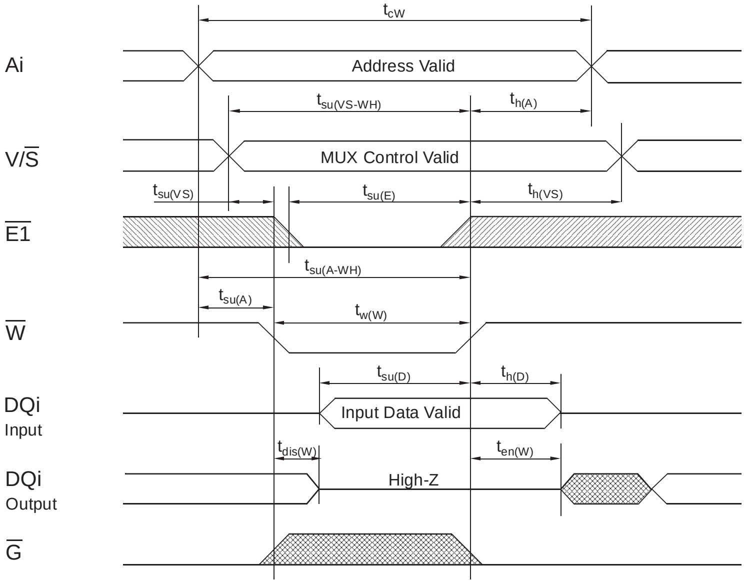
Read Cycle 2: $\overline{E}$-, $\overline{G}$-controlled (during Read Cycle: $\overline{W} = V_{IH}$)

$\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted Low and E2 asserted High.



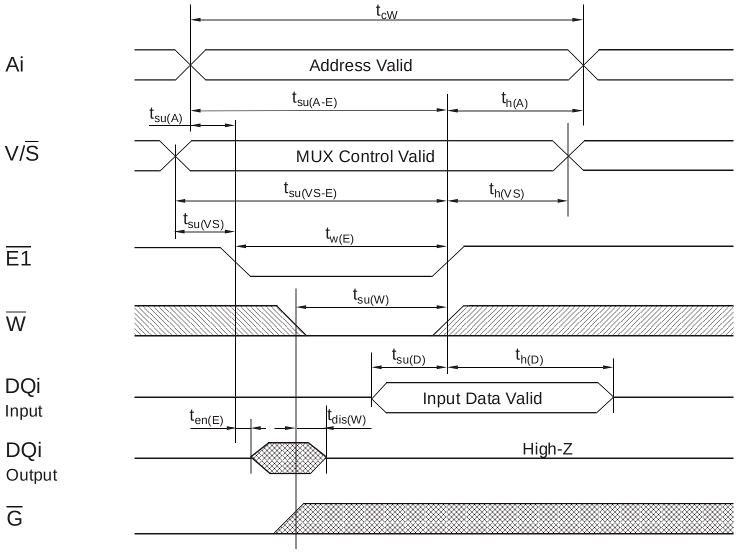
Write Cycle1: $\overline{W}$-controlled

$\overline{E1}$ in the timing diagram represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted Low and E2 asserted High.



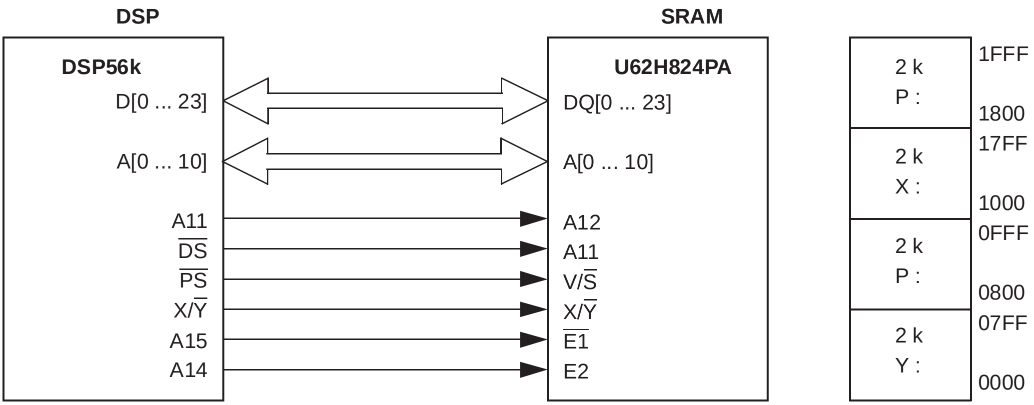
Write Cycle 2: $\overline{E}$-controlled

$\overline{E1}$ in the timing diagram represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted Low and E2 asserted High.



undefined ▩ L- to H-level ▨ H- to L-level ▧

Application Example



DSP	SRAM
P : 4000 ... 47FF P : 4800 ... 4FFF X : 4000 ... 47FF Y : 4000 ... 47FF	0800 ... 0FFF 1800 ... 1FFF 1000 ... 17FF 0000 ... 07FF

No memory overlap with internal P-, X-, Y-memorys.

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Memory Products 1998
Automotive Fast 8K x 24 SRAM U62H824PA

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