SP5659

2·7GHz I²C Bus Low Phase Noise Synthesiser

Preliminary Information

DS4296 ISSUE 2.2 May 2002

The SP5659 is a single chip frequency synthesiser designed for tuning systems up to 2·7GHz.

The RF preamplifier drives a divide-by two prescaler which can be disabled for applications up to 2GHz, allowing direct interfacing with the programmable divider, resulting in a step size equal to the comparison frequency. For applications up to 2·7GHz the divide-by two is enabled to give a step size of twice the comparison frequency.

The comparison frequency is obtained either from an on-chip crystal controlled oscillator or from an external source. The oscillator frequency F_{REF} or the comparison frequency F_{COMP} may be switched to the REF/COMP output; this feature is ideally suited to providing the reference frequency for a second synthesiser such as in a double conversion tuner (see Fig. 5).

The synthesiser is controlled via an I²C bus and responds to one of four programmable addresses which are selected by applying a specific voltage to the Address input. This feature enables two or more synthesisers to be used in a system.

The SP5659 contains four switching ports, P0-P3 and a 5-level ADC, the output of which can be read via the I²C bus.

The SP5659 also contains a varactor line disable and charge pump disable facility.

Features

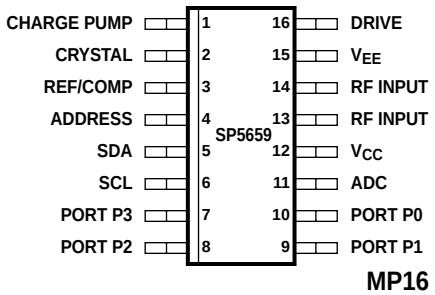
- Complete 2·7GHz Single Chip System
- Optimised for Low Phase Noise
- Selectable 42 prescaler
- Selectable Reference Division Ratio
- Selectable Reference/Comparison Frequency Output
- Selectable Charge Pump Current
- Varactor Drive Amplifier Disable
- 5-Level ADC

Ordering Information

SP5659/KG/MP1S (Tubes)

SP5659/KG/MP1T (Tape and reel)

(16-lead miniature Plastic Package)



MP16

Figure 1 – Pin connections – top view

- Variable I²C BUS Address for Multi-tuner Applications
- ESD Protection: 4kV, Mil-Std-883C, Method 3015 (1)
- Pin Compatible with SP5658

(1) Normal ESD handling precautions should be observed.

Applications

- Satellite TV
- High IF Cable Tuning Systems

Thermal Data

u_{JC} = 41°C/W

u_{JA} = 111°C/W

ELECTRICAL CHARACTERISTICS

T_{AMB} = -20°C to +80°C, V_{CC} = +4·5V to +5·5V, reference frequency = 4MHz.
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.		Max.		
Supply current, I_{CC}	12		68 58	85 73	mA mA	V_{CC} = 5V, PE = 1 (note 1) V_{CC} = 5V, PE = 0
RF input voltage	13,14	50		300	mVrms mVrms mVrms	300MHz to 2·7GHz, PE = 1 (prescaler enabled) see Fig. 4b 100MHz, PE = 1 (prescaler enabled) see Fig. 4b 100MHz to 2·0GHz, PE = 0 (prescaler disabled) see Fig. 4b
RF input impedance RF input capacitance	13,14 13,14		50 2		Ω pF	See Fig. 10 See Fig. 10
SDA, SCL Input high voltage Input low voltage Input high current Input low current Leakage current Input hysteresis	 5, 6 5, 6 5, 6 5, 6 5, 6 5, 6	 3 0	 0·8	 5·5 1·5 10 -10 10	 V V µA µA µA V	 Input voltage = V_{CC} Input voltage = V_{EE} V_{CC} = V_{EE}
SDA Output voltage	 5			 0·4	V	Sink current = 3mA
Charge Pump Output current Output leakage current Drive output current Drive saturation voltage	 1 1 16 16	 1	 +-3	 +-10 350 200	 nA mA mV	 Drive output disabled
External reference input frequency External reference input amplitude Crystal frequency Crystal oscillator drive level Recommended crystal series resistance Crystal oscillator negative resistance	2 2 2 2 2	2 200 4 35 10 400		20 500 16 200	MHz mVp-p MHz mVp-p Ω Ω	AC coupled sinewave AC coupled sinewave Parallel resonant crystal (note 2) Includes temperature and process tolerances
REF/COMP output voltage, enabled	3		350		mVp-p	AC coupled, RE = 1, see note 3
Comparison frequency Equivalent phase noise at phase detector			 -142	2 	MHz dBC/Hz	 See note 4
RF division ratio Reference division ratio		240 480		131071 262142		Prescaler disabled, see Table 1 Prescaler enabled, see Table 1 See Table 1
P0, P1, P2, P3 sink current P0, P1, P2, P3 leakage current	7,8,9,10	10		 10	mA µA	V_{PORT} = 0·7V V_{PORT} = 13·2V
ADC input voltage ADC input current	11 11			610	µA	See Fig. 3 Table 5 V_{CC} >V_{INPUT} >V_{EE}
Address input current high Address input current low	4 4			1 -0·5	mA mA	Input voltage = V_{CC} Input voltage = V_{EE}

NOTES
1. Maximum power consumption is 468mW with V_{CC} = 5·5V and all ports off.
2. Resistance specified is maximum under all conditions including start up.
3. If the REF/COMP output is not used, it should be left open circuit or connected to V_{CC} and disabled by setting RE to logic 0.
4. 6kHz loop bandwidth, phase comparator frequency 250kHZ. Figure measured at 1kHz offset DSB (within loop bandwidth).

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} at 0V

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	12	-0·3	7	V	
RF input voltage	13,14		2·5	V p-p	
RF input DC offset	13, 14		V_{CC}+0·3	V	
Port voltage	7-10	-0·3	14	V	Port in off state
	7-10	-0·3	6	V	Port in on state
Total port current	7-10		50	mA	
ADC input DC offset	11	-0·3	V_{CC}+0·3	V	
REF/COMP output DC offset	3	-0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	-0·3	V_{CC}+0·3	V	
Drive DC offset	16	-0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	-0·3	V_{CC}+0·3	V	
Address DC offset	4	-0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	5, 6	-0·3	6	V	
Storage temperature		-55	+150	°C	
Junction temperature			+150	°C	

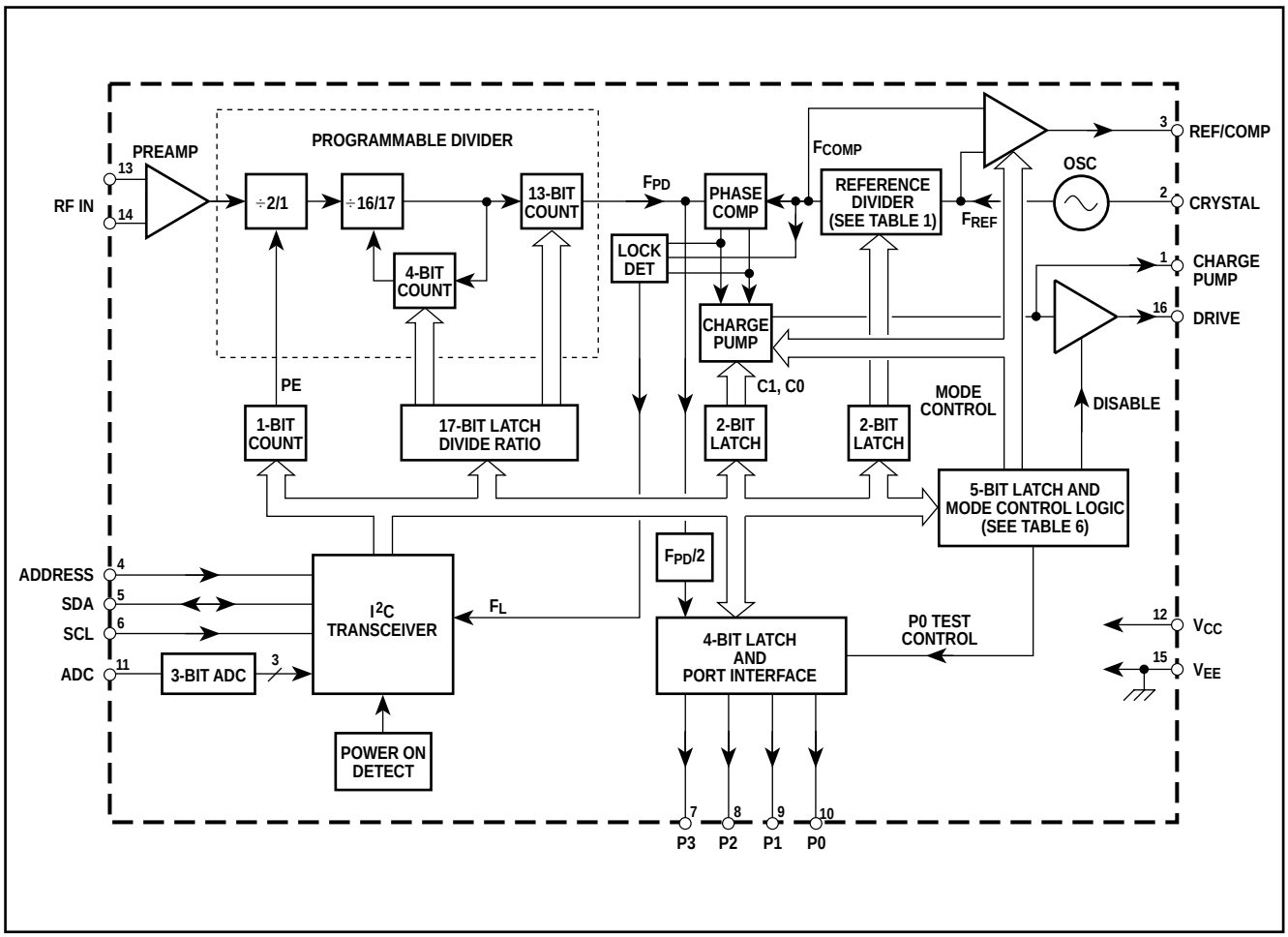


Figure 2 - Block diagram

FUNCTIONAL DESCRIPTION

The SP5659 contains all the elements necessary – with the exception of a frequency reference, loop filter and external high voltage transistor – to control a varactor tuned local oscillator, so forming a complete PLL frequency synthesised source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic which enables the generation of a loop with good phase noise performance. The block diagram is shown in Fig. 2.

The RF input signal is fed to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier interfaces with a 17-bit fully programmable divider via a 42 prescaler. For applications up to 2·0GHz RF input, the prescaler can be disabled, so eliminating the degradation in phase noise due to prescaler action. The divider is of MN1A architecture, where N = 16 or 17, the M counter is 13 bits and the A counter is 4 bits.

The output of the programmable divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency domains with the comparison frequency F_{COMP}. This frequency is derived either from the on-chip crystal controlled oscillator or from an external reference source. In either case, the reference frequency F_{REF} is divided down to the comparison frequency by the reference divider, which is programmable to one of 15 ratios as detailed in Table 1.

The output of the phase detector feeds a charge pump and loop amplifier section which, when used with an external high voltage transistor and loop filter, integrates the current pulses into the varactor line voltage. By invoking the device test modes as described in Fig. 3, Table 6, the varactor drive output can be disabled, so switching the external transistor off. This allows an external voltage to be applied to the varactor line for tuner alignment purposes. Similarly, the charge can also be disabled to a high impedance state.

The programmable divider output $F_{PD}/2$ can be switched to port P0 by programming the device into test mode as set out in Table 6.

PROGRAMMING

The SP5659 is controlled by an I^2C Bus. Data and Clock are fed in on the SDA and SCL lines respectively, as defined by the I^2C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low and read mode if it is high. Tables 1 and 2 in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I^2C Bus system. Table 4 in Fig. 3 shows how the address is selected by applying a voltage to the address input.

When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are programmed. When the device is programmed into the read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

WRITE Mode (Frequency Synthesis)

With reference to Table 2, bytes 2 and 3 contain frequency information bits 2^{14} to 2^0 inclusive. Auxiliary frequency bits 2^{16} and 2^{15} are in byte 4. For most frequencies, only bytes 2 and 3 will be required. The remainder of byte 4 and byte 5 control the prescaler enable, reference divider ratio (see Fig. 3), output ports and test modes (see Table 6).

After reception and acknowledgment of a valid address (byte 1), the first bit of the following byte determines whether the byte is interpreted as byte 2 (logic '0') or byte 4 (logic '1'); the next data byte is then interpreted as byte 3 or byte 5, respectively. After two complete data bytes have been received, additional data bytes can be entered, where byte interpretation follows the same procedure without readdressing the device. This procedure continues until a STOP condition is received. The STOP condition can be generated after any data byte; if, however, it occurs during a byte transmission then the previous data is retained.

To facilitate smooth fine tuning, the frequency data bytes are only accepted by the device after all 17 bits of the data have been received or after the generation of a STOP condition. Repeatedly sending bytes 2 and 3 only will not change the frequency. A frequency change when one of the following data sequences is sent to an addressed device:

Bytes 2, 3, 4, 5
Bytes 4, 5, 2, 3

or when a STOP condition follows valid data bytes thus:

Bytes 2, 3, 4, STOP
Bytes 4, 5, 2, STOP
Bytes 2, 3, STOP
Bytes 2, STOP
Bytes 4, STOP

It should be noted that the SP5569 must be addressed initially with both frequency AND control byte data, since the control byte contains reference divider information which must be provided before a chosen frequency can be synthesised. This implies that after initial turn on, bytes 2, 3 and 4 must be sent followed by a STOP condition as a minimum requirement. Alternatively, bytes 2, 3, 4 and 5 must be sent if port information is also required.

READ Mode

When the device is in read mode the status byte read from the device on the SDA line takes the form shown in Fig. 3, Table 3.

Bit 1 (POR) is the power-on reset indicator and is set to a logic '1' if the V_{CC} supply to the device has dropped below 3V (at 25˚C), for example, when the device is initially turned on. The POR is reset to 0 when the read sequence is

R3	R2	R1	R0	Ratio	Comparison frequency
0	0	0	0	2	2MHz
0	0	0	1	4	1MHz
0	0	1	0	8	500kHz
0	0	1	1	16	250kHz
0	1	0	0	32	125kHz
0	1	0	1	64	62·5kHz
0	1	1	0	128	31·25kHz
0	1	1	1	256	15·625kHz
1	0	0	0	Invalid	
1	0	0	1	5	800kHz
1	0	1	0	10	400kHz
1	0	1	1	20	200kHz
1	1	0	0	40	100kHz
1	1	0	1	80	50kHz
1	1	1	0	160	25kHz
1	1	1	1	320	12·5kHz

Table 1 - Reference division ratios (4MHz external reference)

terminated by a STOP command. When POR is set high (at low V_{CC}), the programmed information is lost and the output ports are all set to high impedance.

Bit 2 (FL) indicates whether the device is phase locked, a logic '1' is present if the device is locked, and a logic '0' if the device is unlocked.

Bits 6, 7 and 8 (A2, A1, A0) combine to give the output of the ADC. The ADC can be used to feed AFC information to the microprocessor via the I^2C bus.

Additional Programmable Features

Prescaler enable

The 42 prescaler is enabled by setting bit PE in byte 4 to a logic '1'. A logic '0' disables the prescaler, directly passing the RF input to the 17-bit counter. Bit PE is a static select only.

Charge pump current

The charge pump current can be programmed by bits C1 and C0 in data byte 5, as defined in Fig. 3, Table 7.

Test mode

The test modes are invoked by setting bit RE to logic '0' and bit RTS to logic '1' within the programming data and are selected by bits TS2, TS1 and TS0 as shown in Fig. 3, Table 6. When TS2, TS1 and TS0 are received, the device retains previously P2, P1 and P0 data.

Reference comparison frequency output

The reference frequency F_{REF} can be switched to the REF/COMP output (pin 3) by setting byte 5 bit RE to logic '1' and bit RTS to logic '0'. The comparison frequency F_{COMP} can be switched to the REF/COMP output by setting bit RE to logic '1' and bit RTS to logic '1'. For RE set to logic '0', the output is disabled and set to a high state. RE and RTS default to logic '1' during power-up, thus enabling F_{COMP} at the REF/COMP output.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	A	**Byte 2**
Programmable divider	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	A	**Byte 3**
Control data	1	2^{16}	2^{15}	PE	R3	R2	R1	R0	A	**Byte 4**
Control data	C1	C0	RE	RTS	P3	P2/TS2	P1/TS1	P0/TS0	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	X	X	X	A2	A1	A0	A	**Byte 2**

Table 3 Read data format

A2	A1	A0	Voltage on ADC input
1	0	0	$0{\cdot}6V_{CC}$ to V_{CC}
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0V to $0{\cdot}15V_{CC}$

Table 4 ADC levels

MA1	MA0	Address input voltage level
0	0	0V to $0{\cdot}1V_{CC}$
0	1	Open circuit
1	0	$0{\cdot}4V_{CC}$ to $0{\cdot}6V_{CC}$
1	1	$0{\cdot}9V_{CC}$ to V_{CC}

Table 5 Address selection

A	:	Acknowledge bit
MA1, MA0	:	Variable address bits (see Table 5)
2^{16}-2^0	:	Programmable division ratio control bits
PE	:	Prescaler enable
R3, R2, R1, R0	:	Reference division ratio select (see Table 1)
C1, C0	:	Charge pump current select (see Table 7)
RE	:	Reference oscillator output enable
RTS	:	REF/COMP select when RE = 1, Test mode enable when RE = 0 (see Table 6)
TS2, TS1, TS0	:	Test mode control bits (valid when RE = 0 and RTS = 1,see Table 6)
P0	:	Port P0 output state (always valid except when RE = 0 and RTS = 1 (see Table 6)
P3, P2, P1	:	Ports P2, P1 and P0 output states
POR	:	Power on reset indicator
FL	:	Phase lock flag
A2, A1, A0	:	ADC data (see Table 4)
X	:	Don't care

Figure 3 - Data formats

cont...

RE	RTS	TS2	TS1	TS0	REF/COMP O/P mode	Test mode description
0	0	X	X	X	Disabled to high state	Normal operation
0	1	X	0	0	Disabled to high state	Charge pump sink, status byte FL = 1
0	1	X	0	1	Disabled to high state	Charge pump source, status byte FL = 0
0	1	X	1	0	Disabled to high state	Charge pump disabled, status byte FL = 0
0	1	X	1	1	Disabled to high state	Port P0 = $F_{PD}/2$
0	1	1	X	X	Disabled to high state	Varactor drive output disabled
1	0	X	X	X	F_{REF} switched	Normal operation
1	1	X	X	X	F_{COMP} switched	Normal operation

Table 6 - REF/COMP output mode and test modes

C1 byte 5, bit 1	C0 byte 5, bit 2	Current (µA)		
		Min.	Typ.	Max.
0	0	+-90	+-120	+-150
0	1	+-195	+-260	+-325
1	0	+-416	+-555	+-694
1	1	+-900	+-1200	+-1500

Table 7 - Charge pump current

Figure 3 - Data formats (continued)

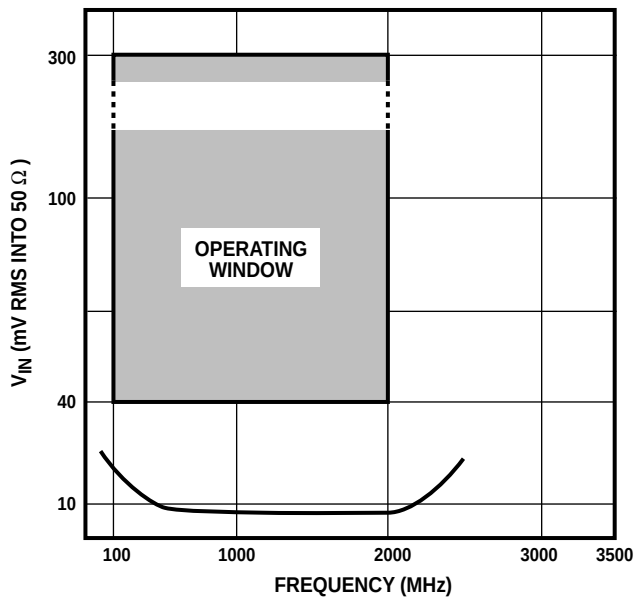


Figure 4a - Prescaler disabled, PE = 0

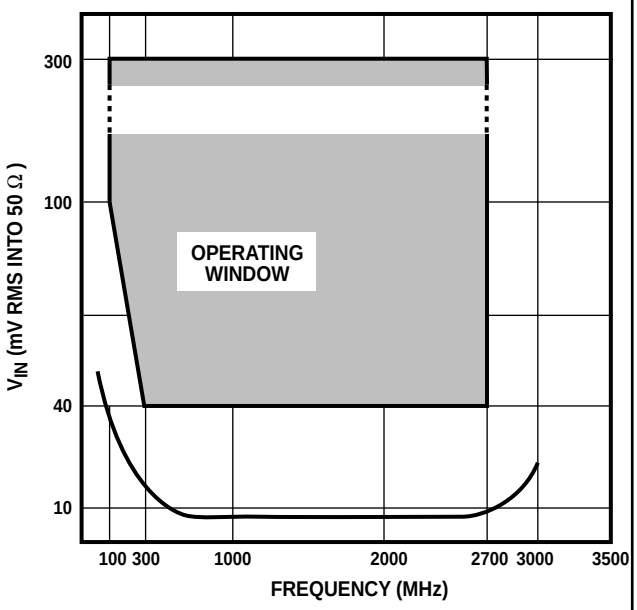


Figure 4b - Prescaler enabled, PE = 1

Figure 4 - Typical input sensitivity

DOUBLE CONVERSION TUNER SYSTEMS

The high 2·7GHz maximum operating frequency and excellent noise characteristics of the SP5659 allow the construction of double conversion high IF tuners.

A typical as shown in Fig. 5 uses the SP5659 as the first local oscillator control for full band up conversion to an IF of greater than 1GHz. The wide range of reference division ratios allows the SP5659 to be used for both the up converter local oscillator with a high phase comparison frequency (hence low phase noise) and the down converter which uses the device in a lower comparison frequency mode, which gives a fine step size.

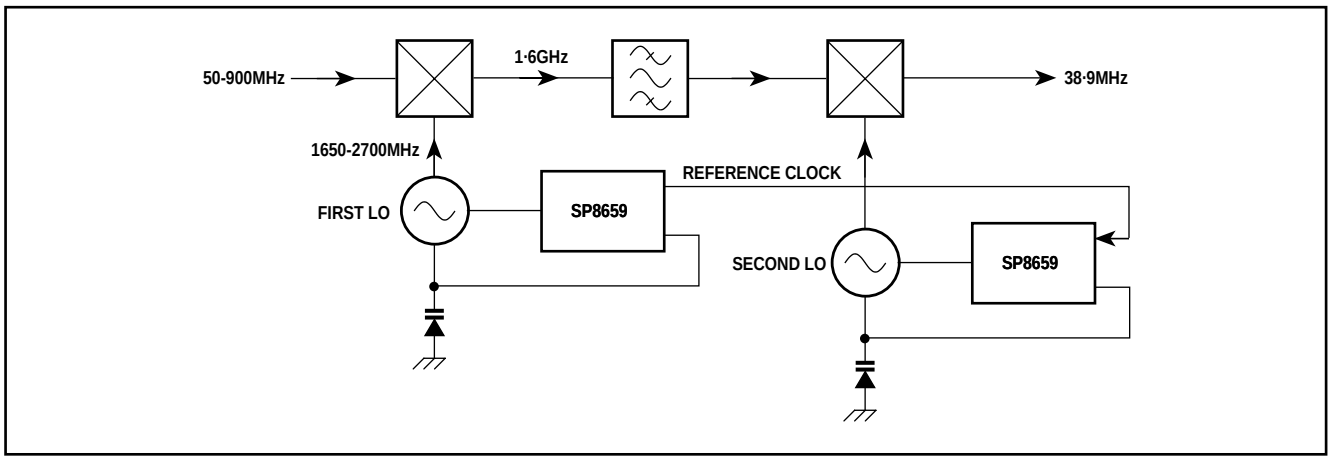


Figure 5 - Example of double conversion from VHF/UHF frequencies to TV IF

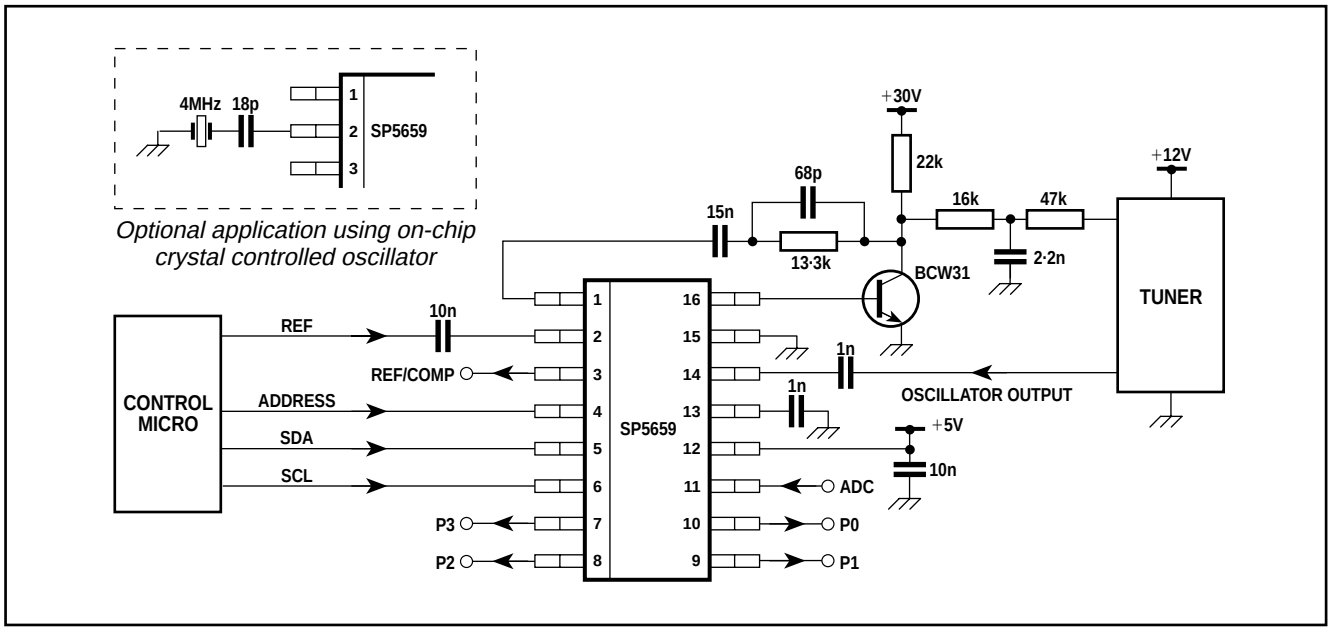


Figure 6 - Typical application

APPLICATION NOTES

An application note, AN168, is available for designing with synthesisers such as the SP5659. It covers aspects such as loop filter design and decoupling.

The application note is published in the Zarlink Semiconductor Media IC Handbook. A generic test/demonstration board has been produced, which can be used for the SP5659. A circuit diagram and layout for the board are shown in Figs. 7 and 8.

The board can be used for the following purposes:

(A) Measuring RF sensitivity performance
(B) Indicating port function
(C) Synthesising a voltage controlled oscillator
(D) Testing external reference sources

The programming codes relevant to these tests are given in Fig. 3.

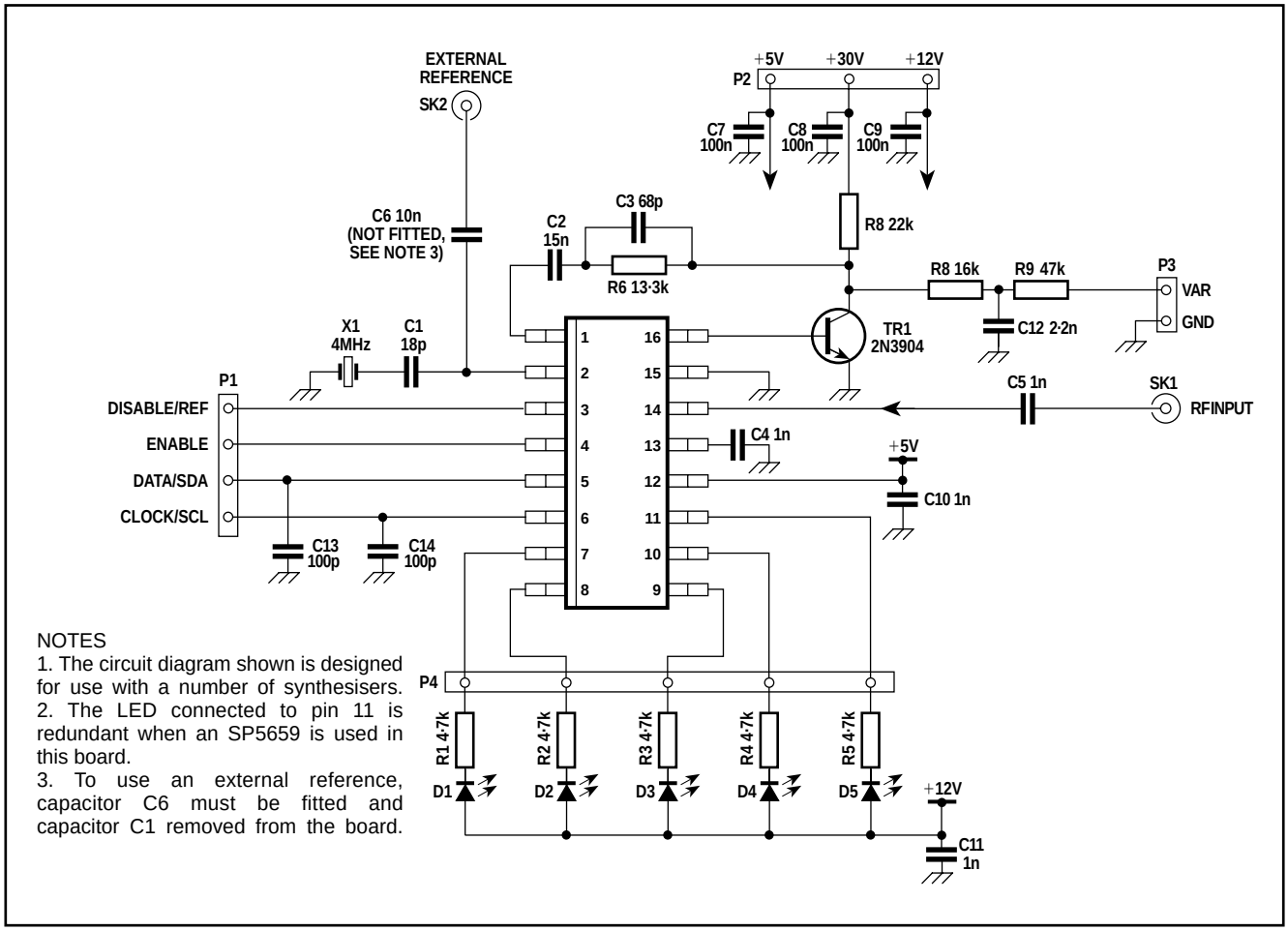


Figure 7 - Test board circuit diagram

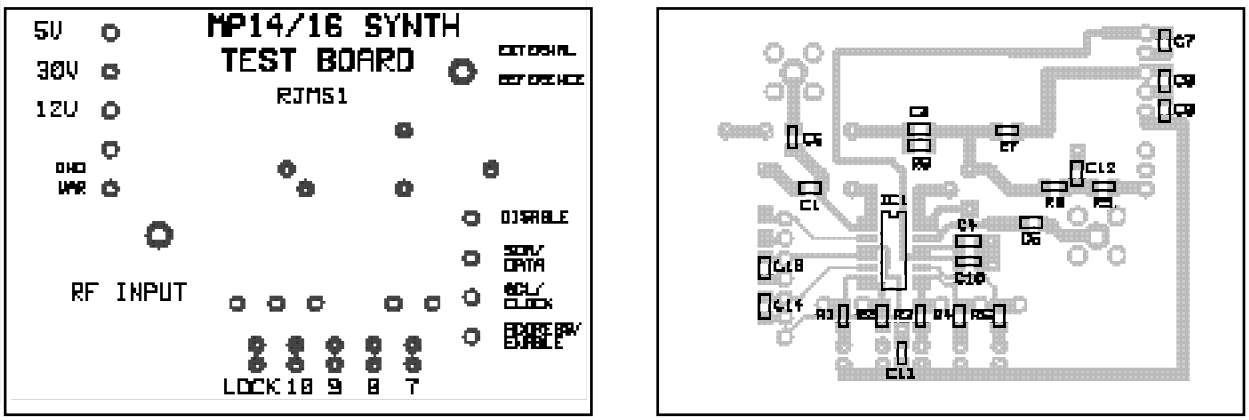


Figure 8 - Test board layout

LOOP BANDWIDTH

Most applications for which the SP5659 is intended require a loop filter bandwidth of between 2kHz and 10kHz.

Typically, the VCO phase noise will be specified at both 1kHz and 10kHz offset. It is common practice to arrange the loop filter bandwidth such that the 1kHz figure lies within the loop bandwidth. The phase noise therefore depends on the synthesiser comparator noise floor rather than the VCO

The 10kHz offset figure should depend on the VCO provided that the loop has been designed correctly and is not underdamped.

REFERENCE SOURCE

The SP5659 offers optimal local oscillator phase noise performance when operated with a large step size. This is because the local oscillator phase noise within the loop bandwidth is:

$$\text{Phase comparator noise floor } 120\log_{10}\left[\frac{F_{LO}}{F_{COMP}}\right]$$

where F_{LO} is the local oscillator frequency and F_{COMP} is the phase comparator frequency.

Assuming the phase comparator noise floor is flat regardless of sampling frequency, this means that the best performance will be achieved when the overall local oscillator to phase comparator division ratio is a minimum.

The are two ways of achieving a higher phase comparator sampling frequency:

1. Reduce the division ratio between the reference source and the phase comparator
2. Use a higher reference source frequency

The second approach may be preferred for best performance since it is possible that the noise floor of the reference oscillator may degrade the phase comparator performance if the reference division ratio is very small.

DRIVING TWO SP5659s FROM A COMMON REFERENCE

The REF/COMP output on pin 3 allows two synthesisers to be driven from a common reference. To do this, the first device should be programmed by setting RE = 1 and RTS = 0. The driven device should be programmed for normal operation with RE = 0 and RTS = 0. The two devices should be connected as shown in Fig. 9.

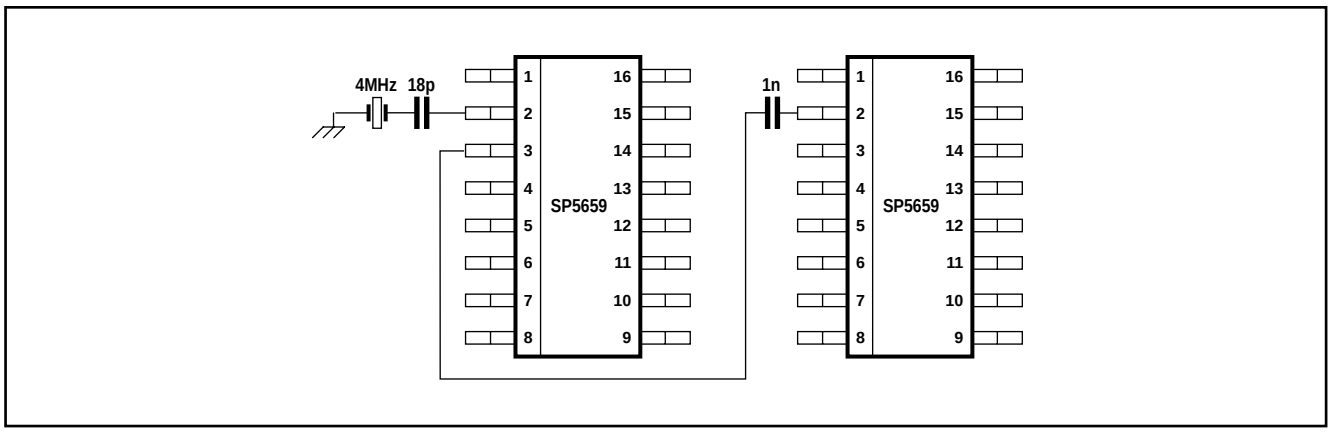


Figure 9 - Two SP5659 devices using a common reference

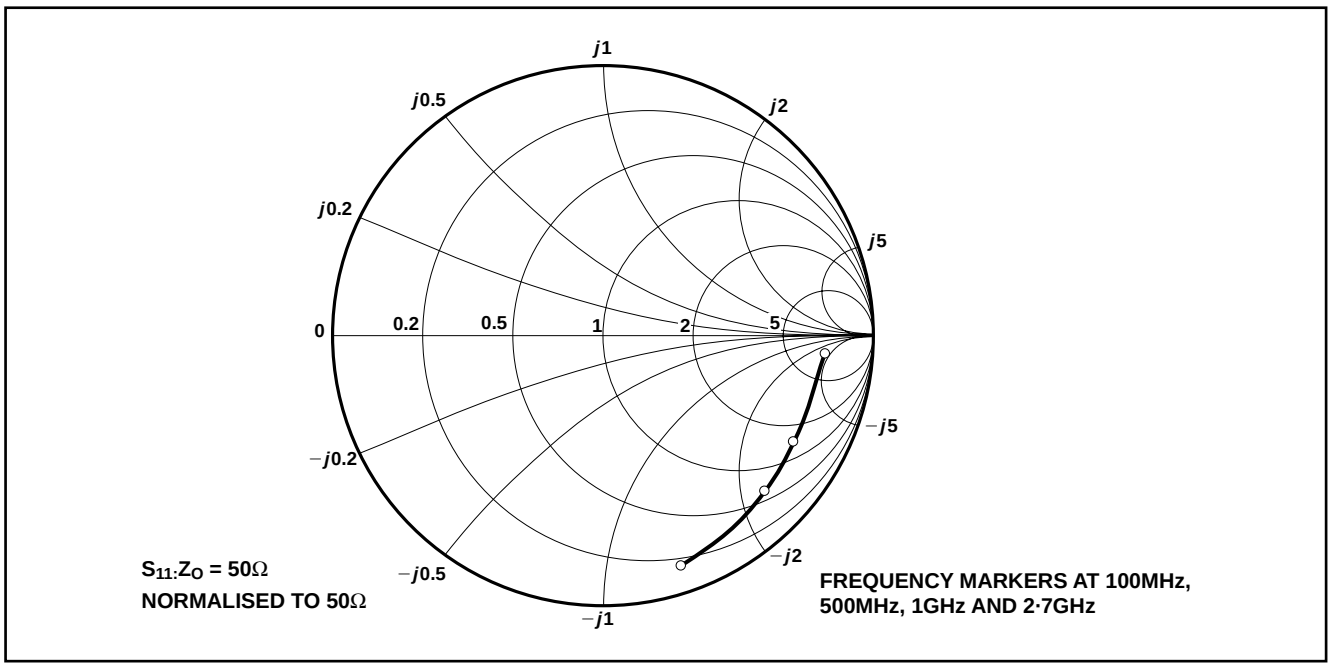


Figure 10 - Typical RF input impedance

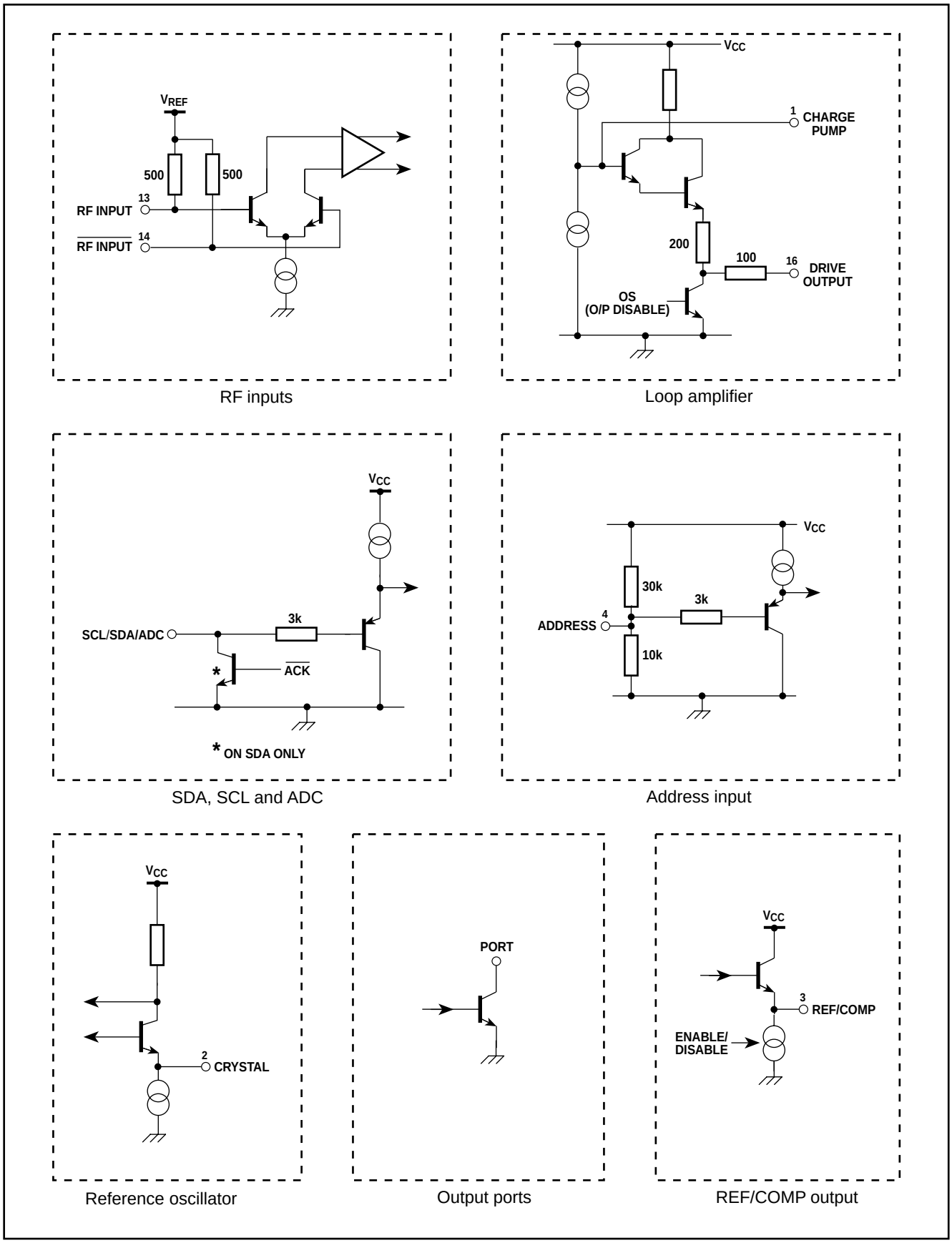


Figure 11 - Input/output interface circuits

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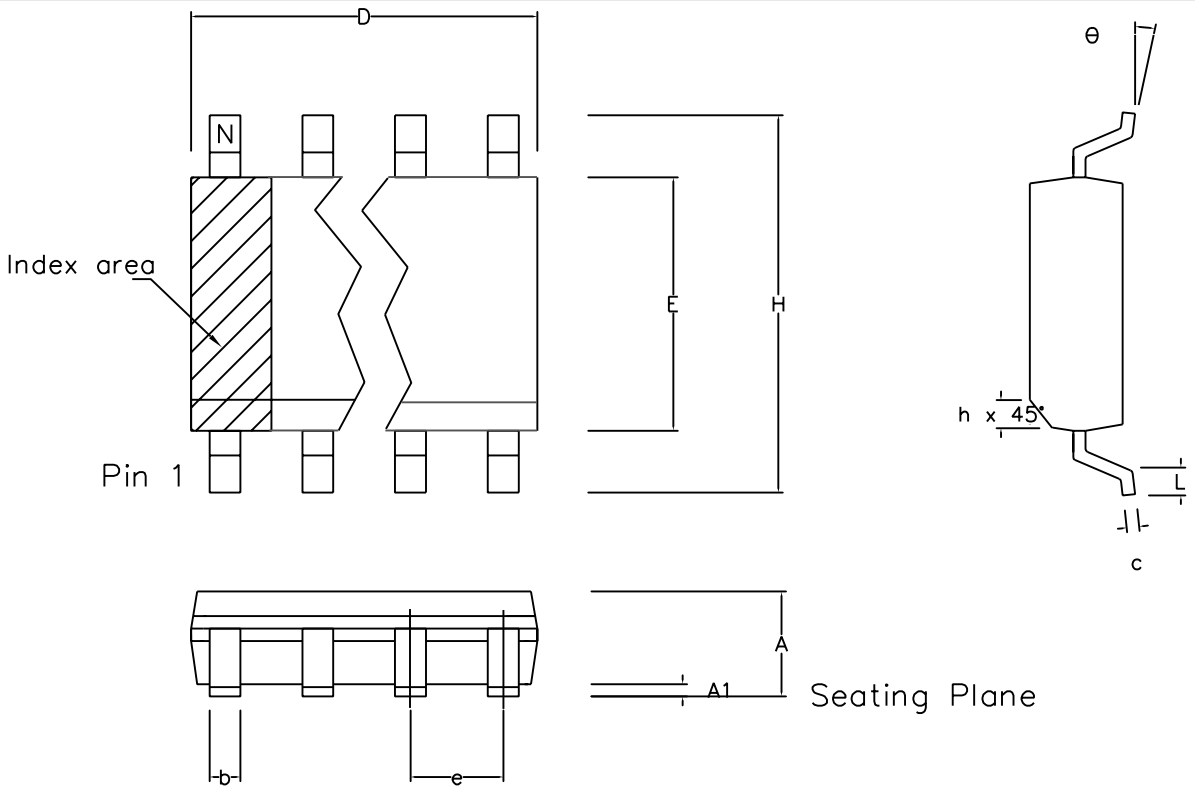

	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.00	0.386	0.394
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	16		16	
Conforms to JEDEC MS-012AC Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
ACN	6745	201938	202597	203706	212431
DATE	7Apr95	27Feb97	12Jun97	9Dec97	25Mar02
APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes
MP / S

Package Code DC

Package Outline for
16 lead SOIC
(0.150" Body Width)

GPD00012

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