P54/74PCT161/A–P54/74PCT163/A SYNCHRONOUS PRESETTABLE BINARY COUNTERS

PRELIMINARY

T-45-23-05

FEATURES

- Full CMOS Implementation
- Low Power Operation
- I_{OL} = 48 mA (Commercial) and 32mA (Military)
- Fully TTL Compatible Input and Output Levels
- Produced with PACE Technology™
- Compact Pinout
  - 16-Pin 300 mil DIP, SOIC
  - 20-Pin 350 mil sq. LCC

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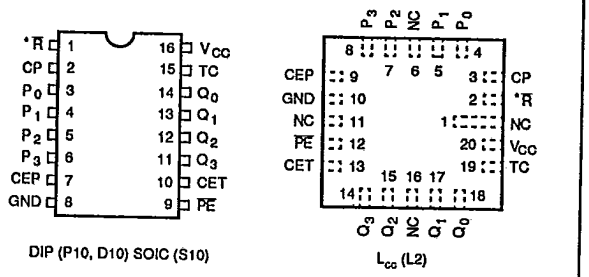
DESCRIPTION

The P54/74PCT161/A and P54/74PCT163/A are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-staged counters. The P54/74PCT161 and P54/74PCT161A have a asynchronous Master Reset input that override all other inputs and force the outputs LOW. The P54/74PCT163 and P54/74PCT163A have a Synchronous Reset input that override counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

The P54/74PCT161/A and P54/74PCT163/A is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

PIN CONFIGURATIONS



DIP (P10, D10) SOIC (S10)

L_{cc} (L2)

* $\overline{MR}$ for 'PCT161, * $\overline{SR}$ for 'PCT163

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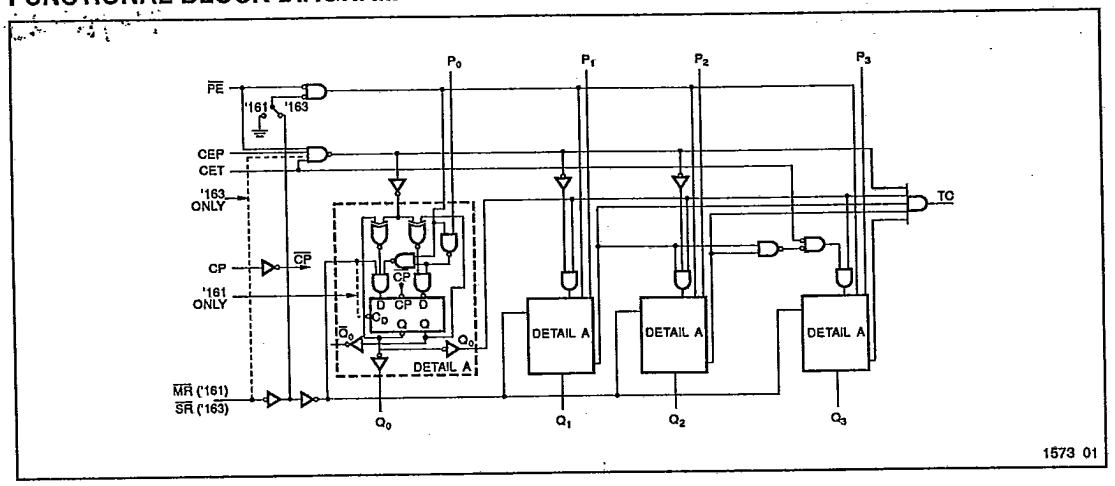
FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−65 to +150	°C
T_A	Ambient Temperature Under Bias	−55 to +125	°C
V_{CC}	V_{CC} Potential to Ground	−0.5 to +7.0	V
I_{IN}	Input Current	−30 to +5.0	mA
I_{OUTPUT}	Current Applied to Output	100	mA
V_{IN}	Input Voltage	−0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	−0.5 to V_{CC} + 0.5	V

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

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2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

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RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	−55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		−0.5		0.8	V		
V_H	Hysteresis			.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage				−1.2	V	MIN	I_{IN} = −18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} − 0.2V	V_{CC} − 0.2			V		I_{OH} = −32µA
		Military/Commercial (CMOS)	V_{CC} − 0.2			V	MIN	I_{OH} = −300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = −12mA
		Commercial (TTL)	2.7			V	MIN	I_{OH} = −15mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} − 0.2V			0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)			0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)			0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)			0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				−5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current[3]				−5	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		−60			mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF		All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF		All outputs

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Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

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DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions[6]
I_{CCQC}	Quiescent Power Supply Current (CMOS inputs) Com'l / Mil	.003 / .003	0.3 / 0.5	mA / mA	V_{CC} = MAX, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$, f = 0, Outputs Open
I_{CCQT}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ mHz	V_{CC} = MAX, One Bit Toggling, Load Mode, 50% Duty Cycle, $\overline{MR} = V_{CC} = \overline{SR}$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$, Outputs Open, CEP = CET = $\overline{PE}$ = GND
I_{CC}	Total Power Supply Current[5]		7.75[4]	mA	V_{CC} = MAX, f_0 = 10MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bit Toggling at f_1 = 5MHz, CEP = CET = $\overline{PE}$ = GND, $\overline{MR} = V_{CC} = \overline{SR}$ $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
			12.75[4]	mA	V_{CC} = MAX, f_0 = 10MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bit Toggling at f_1 = 5MHz, CEP = CET = $\overline{PE}$ = GND, $\overline{MR} = V_{CC} = \overline{SR}$ V_{IN} = 3.4V or V_{IN} =GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQC} + I_{CCQT} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CCQC} = Quiescent Current with CMOS input levels
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.
6. $\overline{MR}$ for 'PCT161, $\overline{SR}$ for 'PCT163

TRUTH TABLE

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	X	H	X	No Change

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H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

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AC CHARACTERISTICS

Sym.	Parameter	P54/74PCT161 P54/74PCT163					P54/74PCT161A P54/74PCT163A					Units	Fig. No.
		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L			
		Typ.	Min.[1]	Max.	Min.[1]	Max.	Typ.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	7.0 7.0	2.0 2.0	11.5 11.5	2.0 2.0	11.0 11.0	4.5 4.5	2.0 2.0	7.5 7.5	2.0 2.0	7.2 7.2	ns ns	1 5
t_{PLH} t_{PHL}	Propagation Delay CP to Q_N ($\overline{PE}$ Input LOW)	7.0 7.0	2.0 2.0	10.0 10.0	2.0 2.0	9.5 9.5	4.5 4.5	2.0 2.0	6.5 6.5	2.0 2.0	6.2 6.2	ns ns	1 5
t_{PLH} t_{PHL}	Propagation Delay CP to TC	10.0 10.0	2.0 2.0	16.5 16.5	2.0 2.0	15.0 15.0	6.5 6.5	2.0 2.0	10.8 10.8	2.0 2.0	9.8 9.8	ns ns	1 5
t_{PLH} t_{PHL}	Propagation Delay CET to TC	4.5 4.5	1.5 1.5	9.0 9.0	1.5 1.5	8.5 8.5	3.0 3.0	1.5 1.5	5.9 5.9	1.5 1.5	5.5 5.5	ns ns	1 5
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n ('PCT161)	9.0 9.0	2.0 2.0	14.0 14.0	2.0 2.0	13.0 13.0	5.9 5.9	2.0 2.0	9.1 9.1	2.0 2.0	8.5 8.5	ns ns	1 6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC ('PCT161)	8.0 8.0	2.0 2.0	12.5 12.5	2.0 2.0	11.5 11.5	5.2 5.2	2.0 2.0	8.2 8.2	2.0 2.0	7.5 7.5	ns ns	1 6

Note: Minimum limits are guaranteed but not tested on Propagation Delays.

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AC OPERATING REQUIREMENTS

Sym.	Parameter	P54/74PCT161 P54/74PCT163					P54/74PCT161A P54/74PCT163A					Units	Fig. No.
		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L			
		Typ.	Min.[1]	Max.	Min.[1]	Max.	Typ.	Min.[1]	Max.	Min.[1]	Max.		
$t_S(H)$ $t_S(L)$	Set-up Time, HIGH or LOW P_n to CP	5.0 5.0	5.5 5.5	— —	5.0 5.0	— —	4.0 4.0	4.5 4.5	— —	4.0 4.0	— —	ns ns	4
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW P_n to CP	2.0 2.0	2.0 2.0	— —	1.5 1.5	— —	1.5 1.5	2.0 2.0	— —	1.5 1.5	— —	ns ns	4
$t_{SU}(H)$ $t_{SU}(L)$	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	11.0 11.0	13.5 13.5	— —	11.5 11.5	— —	9.0 9.0	11.5 11.5	— —	9.5 9.5	— —	ns ns	4
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	2.0 2.0	1.5 1.5	— —	1.5 1.5	— —	1.5 1.5	1.5 1.5	— —	1.5 1.5	— —	ns ns	4
$t_{SU}(H)$ $t_{SU}(L)$	Set-up Time, HIGH or LOW CEP or CET to CP	11.0 11.0	13.0 13.0	— —	11.5 11.5	— —	9.0 9.0	11.0 11.0	— —	9.5 9.5	— —	ns ns	4
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW CEP or CET to CP	0 0	0 0	— —	0 0	— —	0 0	0 0	— —	0 0	— —	ns ns	4
$t_W(H)$ $t_W(L)$	Clock Pulse Width (Load) HIGH or LOW	5.0 5.0	5.0 5.0	— —	5.0 5.0	— —	4.0 4.0	4.0 4.0	— —	4.0 4.0	— —	ns ns	5
$t_W(H)$ $t_W(L)$	Clock Pulse Width (Count) HIGH or LOW	6.0 6.0	8.0 8.0	— —	7.0 7.0	— —	5.0 5.0	7.0 7.0	— —	6.0 6.0	— —	ns ns	5
$t_W(L)$	$\overline{MR}$ Pulse Width LOW ('PCT161)	5.0 5.0	5.0 5.0	— —	5.0 5.0	— —	4.0 4.0	4.0 4.0	— —	4.0 4.0	— —	ns ns	6
t_{REM}	Recovery Time $\overline{MR}$ to CP ('PCT161)	6.0 6.0	6.0 6.0	— —	6.0 6.0	— —	5.0 5.0	5.0 5.0	— —	5.0 5.0	— —	ns ns	6

Note: Minimum limits are guaranteed but not tested on Propagation Delays.

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DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
CEP	Count Enable Parallel Unit
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('162)	Synchronous Reset Input (Active LOW)
P_{0-3}	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q_{0-3}	Flip-Flop Outputs
TC	Terminal Count Output

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TRUTH TABLE

$\overline{SR}$(1)	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (P_n—Q_n)
H	H	H	H	Count (Incremental)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

Notes: 1573 Tbl 11

1. For PCT163/163A only.
2. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care

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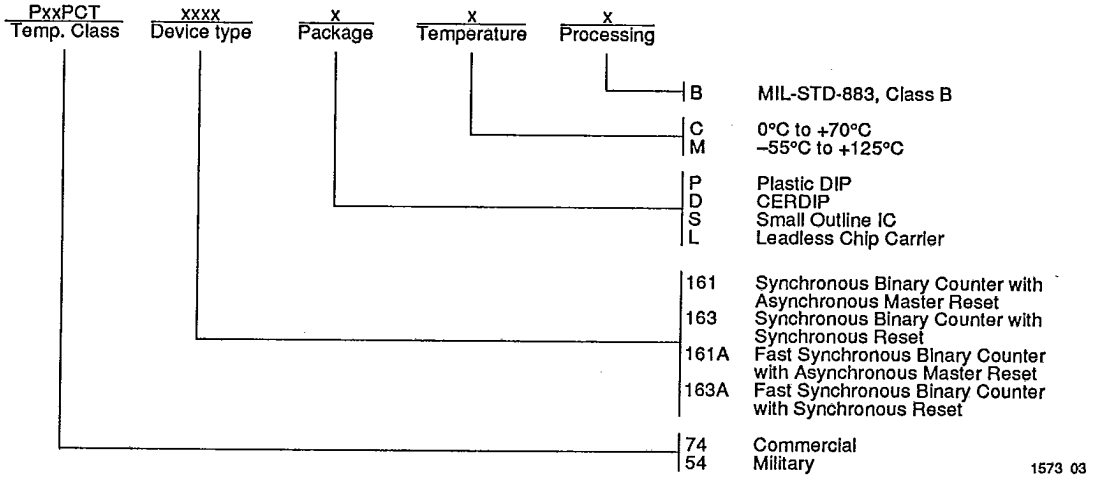
ORDERING INFORMATION



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