Preliminary

128-common x (128+2) RGB-Segment, in 4096-Color STN LCD DRIVER

■ GENERAL DESCRIPTION

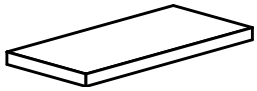
The **NJU6824** is a STN LCD driver with 128-common x (128+2) RGB-segment in 4096-color. It consists of 384(128xRGB)-segment + 6(2xRGB)-icon segment, 128-common drivers, serial and parallel MPU interface circuits, internal power supply circuits, gradation palettes and 196,608-bit for graphic display data RAM.

Each segment driver outputs 16-gradation level out of 32-gradation level of gradation palette.

The display rotate function makes easily rotated display without original display data change.

Since the **NJU6824** provides a low operating voltage of 1.7V and low operating current, it is ideally suited for battery-powered handheld applications.

■ PACKAGE OUTLINE

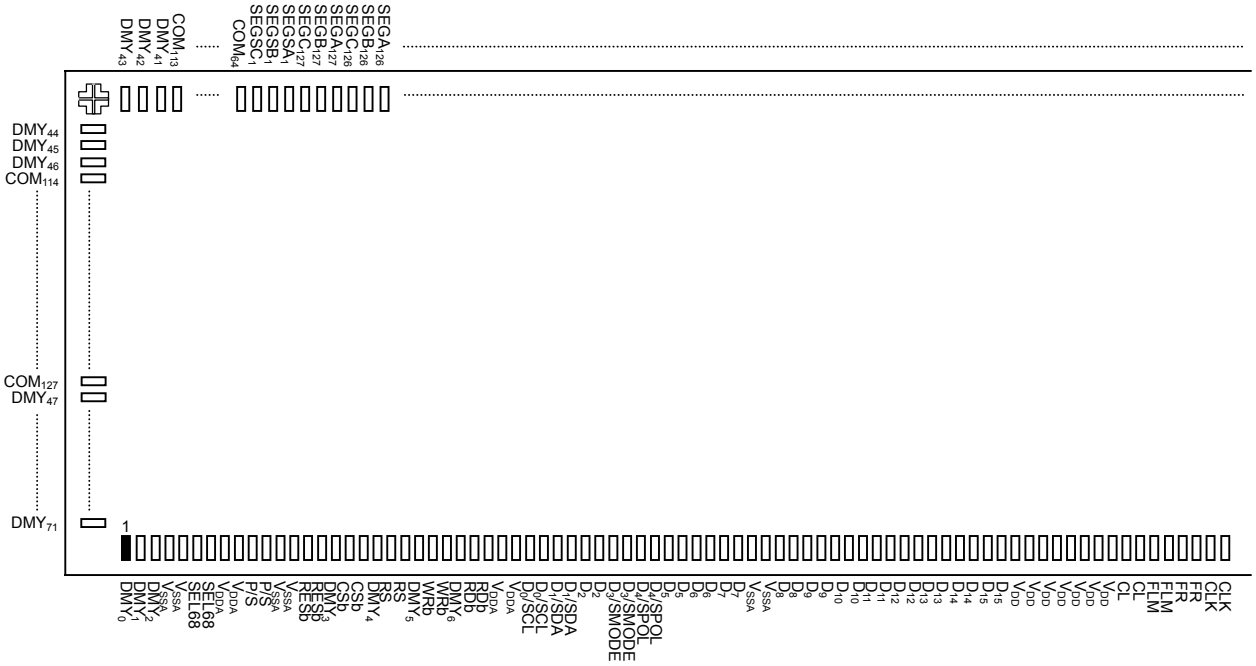


NJU6824CJ

■ FEATURES

- 4096-color STN LCD driver
- LCD drivers 128-commons, 128RGB-segments, 2RGB-icon segments
- Display data RAM (DDRAM) 196,608-bit for graphic display
- Color display mode 16 gradation level out of 32-gradation level of gradation palette
- Black & white display mode 128 x 384 pixels in 16-gradation level or 128 x 384 pixels in B&W
- 256-color driving mode
- 8/16bit Parallel interface directly-connective to 68/80 series MPU
- Programmable 8- or 16-bit data bus length for display data
- 3-/4-line serial interface
- Programmable duty and bias ratios
- Programmable internal voltage booster (Maximum 6-times)
- Bias voltage adjustment circuits
- Programmable contrast control using 128-step EVR
- Display Rotate Function / Display Mirror Inverse Function
- Various instructions
  Display data read/write, Display ON/OFF, Reverse display ON/OFF, All pixels ON/OFF, column address, row address, N-line inversion, Initial display line, Initial COM line, Read-modify-write, Gradation mode control, Increment control, Data bus length, Discharge ON/OFF, Duty cycle ratio, LCD bias ratio, Boost level, EVR control, Power save ON/OFF, etc
- Low operating current
- Low logic supply voltage 1.7V to 3.3V
- LCD driving supply voltage 5.0V to 18.0V
- C-MOS technology
- Rectangle out look for COG
- Package Bumped chip / TCP

■ PAD LOCATION

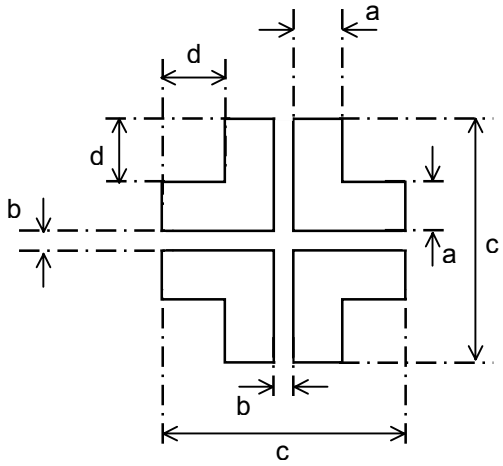


Note1) The same name PADs are shorted mutually in the LSI.
Note2) The DMY PADs are electrically open.

Chip Center	:X= 0μm, Y= 0μm
Chip Size	:22.07mm x 2.55mm
Chip Thickness	:625μm ± 25μm
Bump Size	:28μm x 110μm(COM/SEG Output, DMY_{10} ~ DMY_{71}), 60μm x 100μm(Interface), 28μm x 100μm(DMY_0 ~ DMY_9)
Bump Pitch	:43μm(Min)
Bump Height	:14.0~22.5μm (Typical 18μm) <tolerance : ±3μm >
Bump Material	:Au

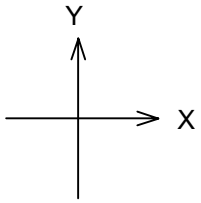
Alignment marks

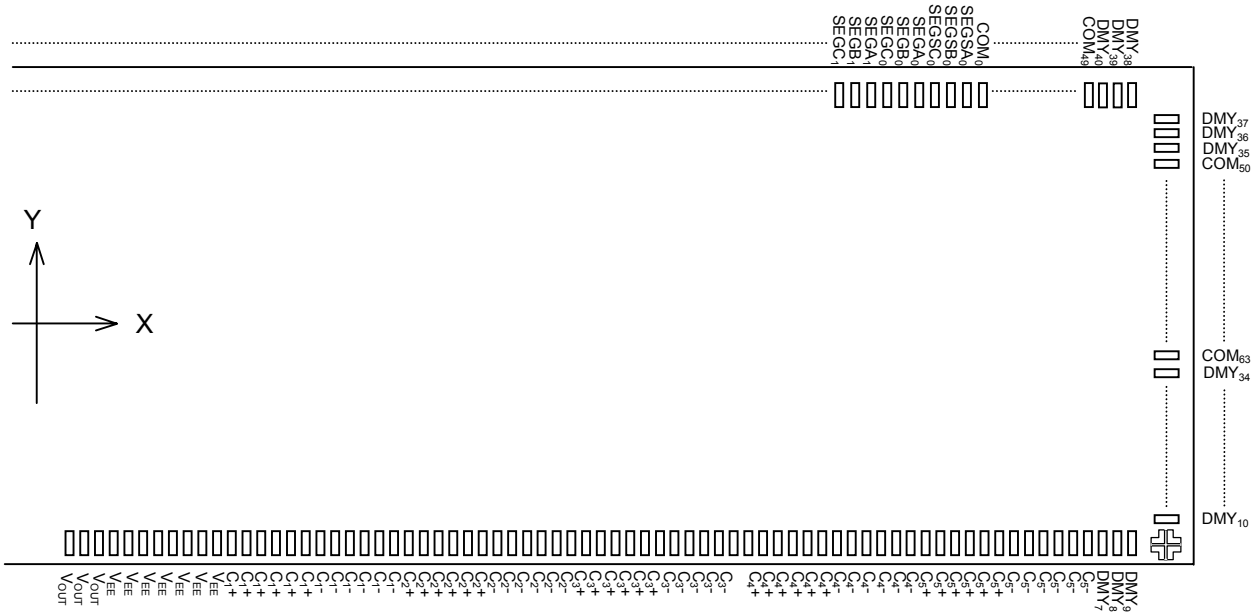
a: 30μm
b: 6μm
c: 120μm
d: 27μm



Alignment mark coordinates

X=-10866μm, Y= 1106μm
X= 10866μm, Y=-1106μm


Y
X


Y
X
DMY37
DMY36
DMY35
COM50
COM63
DMY34
DMY10

■ PAD COORDINATES 1

Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
1	DMY_0	-10642.5	-1090.0	52	D_{10}	-5584.5	-1090.0	103	V_4A_2	-292.0	-1090.0
2	DMY_1	-10599.5	-1090.0	53	D_{10}	-5511.5	-1090.0	104	V_{SSA}	-182.5	-1090.0
3	DMY_2	-10556.5	-1090.0	54	D_{11}	-5365.5	-1090.0	105	V_{SSA}	-109.5	-1090.0
4	V_{SSA}	-10475.5	-1090.0	55	D_{11}	-5292.5	-1090.0	106	V_{LCD}	0.0	-1090.0
5	V_{SSA}	-10402.5	-1090.0	56	D_{12}	-5146.5	-1090.0	107	V_{LCD}	73.0	-1090.0
6	SEL68	-10293.0	-1090.0	57	D_{12}	-5073.5	-1090.0	108	V_{LCD}	146.0	-1090.0
7	SEL68	-10220.0	-1090.0	58	D_{13}	-4927.5	-1090.0	109	V_{LCD}	219.0	-1090.0
8	V_{DDA}	-10110.5	-1090.0	59	D_{13}	-4854.5	-1090.0	110	V_{LCD}	292.0	-1090.0
9	V_{DDA}	-10037.5	-1090.0	60	D_{14}	-4708.5	-1090.0	111	V_{LCD}	365.0	-1090.0
10	P/S	-9928.0	-1090.0	61	D_{14}	-4635.5	-1090.0	112	V_1	511.0	-1090.0
11	P/S	-9855.0	-1090.0	62	D_{15}	-4489.5	-1090.0	113	V_1	584.0	-1090.0
12	V_{SSA}	-9745.5	-1090.0	63	D_{15}	-4416.5	-1090.0	114	V_1	657.0	-1090.0
13	V_{SSA}	-9672.5	-1090.0	64	V_{DD}	-4197.5	-1090.0	115	V_1	730.0	-1090.0
14	RESb	-9563.0	-1090.0	65	V_{DD}	-4124.5	-1090.0	116	V_1	803.0	-1090.0
15	RESb	-9490.0	-1090.0	66	V_{DD}	-4051.5	-1090.0	117	V_1	876.0	-1090.0
16	DMY_3	-9380.5	-1090.0	67	V_{DD}	-3978.5	-1090.0	118	V_2	1022.0	-1090.0
17	CSb	-9271.0	-1090.0	68	V_{DD}	-3905.5	-1090.0	119	V_2	1095.0	-1090.0
18	CSb	-9198.0	-1090.0	69	V_{DD}	-3832.5	-1090.0	120	V_2	1168.0	-1090.0
19	DMY_4	-9088.5	-1090.0	70	V_{DD}	-3759.5	-1090.0	121	V_2	1241.0	-1090.0
20	RS	-8979.0	-1090.0	71	CL	-3613.5	-1090.0	122	V_2	1314.0	-1090.0
21	RS	-8906.0	-1090.0	72	CL	-3540.5	-1090.0	123	V_2	1387.0	-1090.0
22	DMY_5	-8796.5	-1090.0	73	FLM	-3394.5	-1090.0	124	V_3	1533.0	-1090.0
23	WRb	-8687.0	-1090.0	74	FLM	-3321.5	-1090.0	125	V_3	1606.0	-1090.0
24	WRb	-8614.0	-1090.0	75	FR	-3175.5	-1090.0	126	V_3	1679.0	-1090.0
25	DMY_6	-8504.5	-1090.0	76	FR	-3102.5	-1090.0	127	V_3	1752.0	-1090.0
26	RDb	-8395.0	-1090.0	77	CLK	-2956.5	-1090.0	128	V_3	1825.0	-1090.0
27	RDb	-8322.0	-1090.0	78	CLK	-2883.5	-1090.0	129	V_3	1898.0	-1090.0
28	V_{DDA}	-8212.5	-1090.0	79	OSC_1	-2701.0	-1090.0	130	V_4	2044.0	-1090.0
29	V_{DDA}	-8139.5	-1090.0	80	OSC_1	-2628.0	-1090.0	131	V_4	2117.0	-1090.0
30	D_0/SCL	-7993.5	-1090.0	81	OSC_2	-2409.0	-1090.0	132	V_4	2190.0	-1090.0
31	D_0/SCL	-7920.5	-1090.0	82	OSC_2	-2336.0	-1090.0	133	V_4	2263.0	-1090.0
32	D_1/SDA	-7774.5	-1090.0	83	V_{SS}	-2044.0	-1090.0	134	V_4	2336.0	-1090.0
33	D_1/SDA	-7701.5	-1090.0	84	V_{SS}	-1971.0	-1090.0	135	V_4	2409.0	-1090.0
34	D_2	-7555.5	-1090.0	85	V_{SS}	-1898.0	-1090.0	136	V_{REG}	2555.0	-1090.0
35	D_2	-7482.5	-1090.0	86	V_{SS}	-1825.0	-1090.0	137	V_{REG}	2628.0	-1090.0
36	D_3/SMODE	-7336.5	-1090.0	87	V_{SS}	-1752.0	-1090.0	138	V_{REG}	2701.0	-1090.0
37	D_3/SMODE	-7263.5	-1090.0	88	V_{SS}	-1679.0	-1090.0	139	V_{REG}	2774.0	-1090.0
38	D_4/SPOL	-7117.5	-1090.0	89	V_{SS}	-1606.0	-1090.0	140	V_{REG}	2847.0	-1090.0
39	D_4/SPOL	-7044.5	-1090.0	90	V_1A_1	-1460.0	-1090.0	141	V_{REG}	2920.0	-1090.0
40	D_5	-6898.5	-1090.0	91	V_1A_1	-1387.0	-1090.0	142	V_{REF}	3029.5	-1090.0
41	D_5	-6825.5	-1090.0	92	V_{DDA}	-1277.5	-1090.0	143	V_{REF}	3102.5	-1090.0
42	D_6	-6679.5	-1090.0	93	V_{DDA}	-1204.5	-1090.0	144	V_{REF}	3175.5	-1090.0
43	D_6	-6606.5	-1090.0	94	V_1A_2	-1095.0	-1090.0	145	V_{REF}	3248.5	-1090.0
44	D_7	-6460.5	-1090.0	95	V_1A_2	-1022.0	-1090.0	146	V_{REF}	3321.5	-1090.0
45	D_7	-6387.5	-1090.0	96	V_{SSA}	-912.5	-1090.0	147	V_{REF}	3394.5	-1090.0
46	V_{SSA}	-6241.5	-1090.0	97	V_{SSA}	-839.5	-1090.0	148	V_{BA}	3504.0	-1090.0
47	V_{SSA}	-6168.5	-1090.0	98	V_4A_1	-730.0	-1090.0	149	V_{BA}	3577.0	-1090.0
48	D_8	-6022.5	-1090.0	99	V_4A_1	-657.0	-1090.0	150	V_{BA}	3650.0	-1090.0
49	D_8	-5949.5	-1090.0	100	V_{DDA}	-547.5	-1090.0	151	V_{BA}	3723.0	-1090.0
50	D_9	-5803.5	-1090.0	101	V_{DDA}	-474.5	-1090.0	152	V_{BA}	3796.0	-1090.0
51	D_9	-5730.5	-1090.0	102	V_4A_2	-365.0	-1090.0	153	V_{BA}	3869.0	-1090.0

■ PAD COORDINATES 2

Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
154	V_{SSH}	4051.5	-1090.0	205	C_3-	8212.5	-1090.0	256	DMY_{28}	10845.0	-107.5
155	V_{SSH}	4124.5	-1090.0	206	C_3-	8285.5	-1090.0	257	DMY_{29}	10845.0	-64.5
156	V_{SSH}	4197.5	-1090.0	207	C_3-	8358.5	-1090.0	258	DMY_{30}	10845.0	-21.5
157	V_{SSH}	4270.5	-1090.0	208	C_3-	8431.5	-1090.0	259	DMY_{31}	10845.0	21.5
158	V_{SSH}	4343.5	-1090.0	209	C_3-	8504.5	-1090.0	260	DMY_{32}	10845.0	64.5
159	V_{SSH}	4416.5	-1090.0	210	C_3-	8577.5	-1090.0	261	DMY_{33}	10845.0	107.5
160	V_{SSH}	4489.5	-1090.0	211	C_4+	8687.0	-1090.0	262	DMY_{34}	10845.0	150.5
161	V_{OUT}	4672.0	-1090.0	212	C_4+	8760.0	-1090.0	263	COM_{63}	10845.0	193.5
162	V_{OUT}	4745.0	-1090.0	213	C_4+	8833.0	-1090.0	264	COM_{62}	10845.0	236.5
163	V_{OUT}	4818.0	-1090.0	214	C_4+	8906.0	-1090.0	265	COM_{61}	10845.0	279.5
164	V_{OUT}	4891.0	-1090.0	215	C_4+	8979.0	-1090.0	266	COM_{60}	10845.0	322.5
165	V_{OUT}	4964.0	-1090.0	216	C_4+	9052.0	-1090.0	267	COM_{59}	10845.0	365.5
166	V_{OUT}	5037.0	-1090.0	217	C_4-	9161.5	-1090.0	268	COM_{58}	10845.0	408.5
167	V_{OUT}	5110.0	-1090.0	218	C_4-	9234.5	-1090.0	269	COM_{57}	10845.0	451.5
168	V_{EE}	5292.5	-1090.0	219	C_4-	9307.5	-1090.0	270	COM_{56}	10845.0	494.5
169	V_{EE}	5365.5	-1090.0	220	C_4-	9380.5	-1090.0	271	COM_{55}	10845.0	537.5
170	V_{EE}	5438.5	-1090.0	221	C_4-	9453.5	-1090.0	272	COM_{54}	10845.0	580.5
171	V_{EE}	5511.5	-1090.0	222	C_4-	9526.5	-1090.0	273	COM_{53}	10845.0	623.5
172	V_{EE}	5584.5	-1090.0	223	C_5+	9636.0	-1090.0	274	COM_{52}	10845.0	666.5
173	V_{EE}	5657.5	-1090.0	224	C_5+	9709.0	-1090.0	275	COM_{51}	10845.0	709.5
174	V_{EE}	5730.5	-1090.0	225	C_5+	9782.0	-1090.0	276	COM_{50}	10845.0	752.5
175	C_1+	5840.0	-1090.0	226	C_5+	9855.0	-1090.0	277	DMY_{35}	10845.0	795.5
176	C_1+	5913.0	-1090.0	227	C_5+	9928.0	-1090.0	278	DMY_{36}	10845.0	838.5
177	C_1+	5986.0	-1090.0	228	C_5+	10001.0	-1090.0	279	DMY_{37}	10845.0	881.5
178	C_1+	6059.0	-1090.0	229	C_5-	10110.5	-1090.0	280	DMY_{38}	10642.5	1085.0
179	C_1+	6132.0	-1090.0	230	C_5-	10183.5	-1090.0	281	DMY_{39}	10599.5	1085.0
180	C_1+	6205.0	-1090.0	231	C_5-	10256.5	-1090.0	282	DMY_{40}	10556.5	1085.0
181	C_1-	6314.5	-1090.0	232	C_5-	10329.5	-1090.0	283	COM_{49}	10513.5	1085.0
182	C_1-	6387.5	-1090.0	233	C_5-	10402.5	-1090.0	284	COM_{48}	10470.5	1085.0
183	C_1-	6460.5	-1090.0	234	C_5-	10475.5	-1090.0	285	COM_{47}	10427.5	1085.0
184	C_1-	6533.5	-1090.0	235	DMY_7	10556.5	-1090.0	286	COM_{46}	10384.5	1085.0
185	C_1-	6606.5	-1090.0	236	DMY_8	10599.5	-1090.0	287	COM_{45}	10341.5	1085.0
186	C_1-	6679.5	-1090.0	237	DMY_9	10642.5	-1090.0	288	COM_{44}	10298.5	1085.0
187	C_2+	6789.0	-1090.0	238	DMY_{10}	10845.0	-881.5	289	COM_{43}	10255.5	1085.0
188	C_2+	6862.0	-1090.0	239	DMY_{11}	10845.0	-838.5	290	COM_{42}	10212.5	1085.0
189	C_2+	6935.0	-1090.0	240	DMY_{12}	10845.0	-795.5	291	COM_{41}	10169.5	1085.0
190	C_2+	7008.0	-1090.0	241	DMY_{13}	10845.0	-752.5	292	COM_{40}	10126.5	1085.0
191	C_2+	7081.0	-1090.0	242	DMY_{14}	10845.0	-709.5	293	COM_{39}	10083.5	1085.0
192	C_2+	7154.0	-1090.0	243	DMY_{15}	10845.0	-666.5	294	COM_{38}	10040.5	1085.0
193	C_2-	7263.5	-1090.0	244	DMY_{16}	10845.0	-623.5	295	COM_{37}	9997.5	1085.0
194	C_2-	7336.5	-1090.0	245	DMY_{17}	10845.0	-580.5	296	COM_{36}	9954.5	1085.0
195	C_2-	7409.5	-1090.0	246	DMY_{18}	10845.0	-537.5	297	COM_{35}	9911.5	1085.0
196	C_2-	7482.5	-1090.0	247	DMY_{19}	10845.0	-494.5	298	COM_{34}	9868.5	1085.0
197	C_2-	7555.5	-1090.0	248	DMY_{20}	10845.0	-451.5	299	COM_{33}	9825.5	1085.0
198	C_2-	7628.5	-1090.0	249	DMY_{21}	10845.0	-408.5	300	COM_{32}	9782.5	1085.0
199	C_3+	7738.0	-1090.0	250	DMY_{22}	10845.0	-365.5	301	COM_{31}	9739.5	1085.0
200	C_3+	7811.0	-1090.0	251	DMY_{23}	10845.0	-322.5	302	COM_{30}	9696.5	1085.0
201	C_3+	7884.0	-1090.0	252	DMY_{24}	10845.0	-279.5	303	COM_{29}	9653.5	1085.0
202	C_3+	7957.0	-1090.0	253	DMY_{25}	10845.0	-236.5	304	COM_{28}	9610.5	1085.0
203	C_3+	8030.0	-1090.0	254	DMY_{26}	10845.0	-193.5	305	COM_{27}	9567.5	1085.0
204	C_3+	8103.0	-1090.0	255	DMY_{27}	10845.0	-150.5	306	COM_{26}	9524.5	1085.0

■ PAD COORDINATES 3

Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
307	COM_{25}	9481.5	1085.0	358	$SEGB_{7}$	7288.5	1085.0	409	$SEGB_{24}$	5095.5	1085.0
308	COM_{24}	9438.5	1085.0	359	$SEGC_{7}$	7245.5	1085.0	410	$SEGC_{24}$	5052.5	1085.0
309	COM_{23}	9395.5	1085.0	360	$SEGA_{8}$	7202.5	1085.0	411	$SEGA_{25}$	5009.5	1085.0
310	COM_{22}	9352.5	1085.0	361	$SEGB_{8}$	7159.5	1085.0	412	$SEGB_{25}$	4966.5	1085.0
311	COM_{21}	9309.5	1085.0	362	$SEGC_{8}$	7116.5	1085.0	413	$SEGC_{25}$	4923.5	1085.0
312	COM_{20}	9266.5	1085.0	363	$SEGA_{9}$	7073.5	1085.0	414	$SEGA_{26}$	4880.5	1085.0
313	COM_{19}	9223.5	1085.0	364	$SEGB_{9}$	7030.5	1085.0	415	$SEGB_{26}$	4837.5	1085.0
314	COM_{18}	9180.5	1085.0	365	$SEGC_{9}$	6987.5	1085.0	416	$SEGC_{26}$	4794.5	1085.0
315	COM_{17}	9137.5	1085.0	366	$SEGA_{10}$	6944.5	1085.0	417	$SEGA_{27}$	4751.5	1085.0
316	COM_{16}	9094.5	1085.0	367	$SEGB_{10}$	6901.5	1085.0	418	$SEGB_{27}$	4708.5	1085.0
317	COM_{15}	9051.5	1085.0	368	$SEGC_{10}$	6858.5	1085.0	419	$SEGC_{27}$	4665.5	1085.0
318	COM_{14}	9008.5	1085.0	369	$SEGA_{11}$	6815.5	1085.0	420	$SEGA_{28}$	4622.5	1085.0
319	COM_{13}	8965.5	1085.0	370	$SEGB_{11}$	6772.5	1085.0	421	$SEGB_{28}$	4579.5	1085.0
320	COM_{12}	8922.5	1085.0	371	$SEGC_{11}$	6729.5	1085.0	422	$SEGC_{28}$	4536.5	1085.0
321	COM_{11}	8879.5	1085.0	372	$SEGA_{12}$	6686.5	1085.0	423	$SEGA_{29}$	4493.5	1085.0
322	COM_{10}	8836.5	1085.0	373	$SEGB_{12}$	6643.5	1085.0	424	$SEGB_{29}$	4450.5	1085.0
323	COM_{9}	8793.5	1085.0	374	$SEGC_{12}$	6600.5	1085.0	425	$SEGC_{29}$	4407.5	1085.0
324	COM_{8}	8750.5	1085.0	375	$SEGA_{13}$	6557.5	1085.0	426	$SEGA_{30}$	4364.5	1085.0
325	COM_{7}	8707.5	1085.0	376	$SEGB_{13}$	6514.5	1085.0	427	$SEGB_{30}$	4321.5	1085.0
326	COM_{6}	8664.5	1085.0	377	$SEGC_{13}$	6471.5	1085.0	428	$SEGC_{30}$	4278.5	1085.0
327	COM_{5}	8621.5	1085.0	378	$SEGA_{14}$	6428.5	1085.0	429	$SEGA_{31}$	4235.5	1085.0
328	COM_{4}	8578.5	1085.0	379	$SEGB_{14}$	6385.5	1085.0	430	$SEGB_{31}$	4192.5	1085.0
329	COM_{3}	8535.5	1085.0	380	$SEGC_{14}$	6342.5	1085.0	431	$SEGC_{31}$	4149.5	1085.0
330	COM_{2}	8492.5	1085.0	381	$SEGA_{15}$	6299.5	1085.0	432	$SEGA_{32}$	4106.5	1085.0
331	COM_{1}	8449.5	1085.0	382	$SEGB_{15}$	6256.5	1085.0	433	$SEGB_{32}$	4063.5	1085.0
332	COM_{0}	8406.5	1085.0	383	$SEGC_{15}$	6213.5	1085.0	434	$SEGC_{32}$	4020.5	1085.0
333	$SEGSA_{0}$	8363.5	1085.0	384	$SEGA_{16}$	6170.5	1085.0	435	$SEGA_{33}$	3977.5	1085.0
334	$SEGSB_{0}$	8320.5	1085.0	385	$SEGB_{16}$	6127.5	1085.0	436	$SEGB_{33}$	3934.5	1085.0
335	$SEGSC_{0}$	8277.5	1085.0	386	$SEGC_{16}$	6084.5	1085.0	437	$SEGC_{33}$	3891.5	1085.0
336	$SEGA_{0}$	8234.5	1085.0	387	$SEGA_{17}$	6041.5	1085.0	438	$SEGA_{34}$	3848.5	1085.0
337	$SEGB_{0}$	8191.5	1085.0	388	$SEGB_{17}$	5998.5	1085.0	439	$SEGB_{34}$	3805.5	1085.0
338	$SEGC_{0}$	8148.5	1085.0	389	$SEGC_{17}$	5955.5	1085.0	440	$SEGC_{34}$	3762.5	1085.0
339	$SEGA_{1}$	8105.5	1085.0	390	$SEGA_{18}$	5912.5	1085.0	441	$SEGA_{35}$	3719.5	1085.0
340	$SEGB_{1}$	8062.5	1085.0	391	$SEGB_{18}$	5869.5	1085.0	442	$SEGB_{35}$	3676.5	1085.0
341	$SEGC_{1}$	8019.5	1085.0	392	$SEGC_{18}$	5826.5	1085.0	443	$SEGC_{35}$	3633.5	1085.0
342	$SEGA_{2}$	7976.5	1085.0	393	$SEGA_{19}$	5783.5	1085.0	444	$SEGA_{36}$	3590.5	1085.0
343	$SEGB_{2}$	7933.5	1085.0	394	$SEGB_{19}$	5740.5	1085.0	445	$SEGB_{36}$	3547.5	1085.0
344	$SEGC_{2}$	7890.5	1085.0	395	$SEGC_{19}$	5697.5	1085.0	446	$SEGC_{36}$	3504.5	1085.0
345	$SEGA_{2}$	7847.5	1085.0	396	$SEGA_{20}$	5654.5	1085.0	447	$SEGA_{37}$	3461.5	1085.0
346	$SEGB_{3}$	7804.5	1085.0	397	$SEGB_{20}$	5611.5	1085.0	448	$SEGB_{37}$	3418.5	1085.0
347	$SEGC_{3}$	7761.5	1085.0	398	$SEGC_{20}$	5568.5	1085.0	449	$SEGC_{37}$	3375.5	1085.0
348	$SEGA_{4}$	7718.5	1085.0	399	$SEGA_{21}$	5525.5	1085.0	450	$SEGA_{38}$	3332.5	1085.0
349	$SEGB_{4}$	7675.5	1085.0	400	$SEGB_{21}$	5482.5	1085.0	451	$SEGB_{38}$	3289.5	1085.0
350	$SEGC_{4}$	7632.5	1085.0	401	$SEGC_{21}$	5439.5	1085.0	452	$SEGC_{38}$	3246.5	1085.0
351	$SEGA_{5}$	7589.5	1085.0	402	$SEGA_{22}$	5396.5	1085.0	453	$SEGA_{39}$	3203.5	1085.0
352	$SEGB_{5}$	7546.5	1085.0	403	$SEGB_{22}$	5353.5	1085.0	454	$SEGB_{39}$	3160.5	1085.0
353	$SEGC_{5}$	7503.5	1085.0	404	$SEGC_{22}$	5310.5	1085.0	455	$SEGC_{39}$	3117.5	1085.0
354	$SEGA_{6}$	7460.5	1085.0	405	$SEGA_{23}$	5267.5	1085.0	456	$SEGA_{40}$	3074.5	1085.0
355	$SEGB_{6}$	7417.5	1085.0	406	$SEGB_{23}$	5224.5	1085.0	457	$SEGB_{40}$	3031.5	1085.0
356	$SEGC_{6}$	7374.5	1085.0	407	$SEGC_{23}$	5181.5	1085.0	458	$SEGC_{40}$	2988.5	1085.0
357	$SEGA_{7}$	7331.5	1085.0	408	$SEGA_{24}$	5138.5	1085.0	459	$SEGA_{41}$	2945.5	1085.0

■ PAD COORDINATES 4

Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
460	$SEGB_{41}$	2902.5	1085.0	511	$SEGB_{58}$	709.5	1085.0	562	$SEGB_{75}$	-1483.5	1085.0
461	$SEGC_{41}$	2859.5	1085.0	512	$SEGC_{58}$	666.5	1085.0	563	$SEGC_{75}$	-1526.5	1085.0
462	$SEGA_{42}$	2816.5	1085.0	513	$SEGA_{59}$	623.5	1085.0	564	$SEGA_{76}$	-1569.5	1085.0
463	$SEGB_{42}$	2773.5	1085.0	514	$SEGB_{59}$	580.5	1085.0	565	$SEGB_{76}$	-1612.5	1085.0
464	$SEGC_{42}$	2730.5	1085.0	515	$SEGC_{59}$	537.5	1085.0	566	$SEGC_{76}$	-1655.5	1085.0
465	$SEGA_{43}$	2687.5	1085.0	516	$SEGA_{60}$	494.5	1085.0	567	$SEGA_{77}$	-1698.5	1085.0
466	$SEGB_{43}$	2644.5	1085.0	517	$SEGB_{60}$	451.5	1085.0	568	$SEGB_{77}$	-1741.5	1085.0
467	$SEGC_{43}$	2601.5	1085.0	518	$SEGC_{60}$	408.5	1085.0	569	$SEGC_{77}$	-1784.5	1085.0
468	$SEGA_{44}$	2558.5	1085.0	519	$SEGA_{61}$	365.5	1085.0	570	$SEGA_{78}$	-1827.5	1085.0
469	$SEGB_{44}$	2515.5	1085.0	520	$SEGB_{61}$	322.5	1085.0	571	$SEGB_{78}$	-1870.5	1085.0
470	$SEGC_{44}$	2472.5	1085.0	521	$SEGC_{61}$	279.5	1085.0	572	$SEGC_{78}$	-1913.5	1085.0
471	$SEGA_{45}$	2429.5	1085.0	522	$SEGA_{62}$	236.5	1085.0	573	$SEGA_{79}$	-1956.5	1085.0
472	$SEGB_{45}$	2386.5	1085.0	523	$SEGB_{62}$	193.5	1085.0	574	$SEGB_{79}$	-1999.5	1085.0
473	$SEGC_{45}$	2343.5	1085.0	524	$SEGC_{62}$	150.5	1085.0	575	$SEGC_{79}$	-2042.5	1085.0
474	$SEGA_{46}$	2300.5	1085.0	525	$SEGA_{63}$	107.5	1085.0	576	$SEGA_{80}$	-2085.5	1085.0
475	$SEGB_{46}$	2257.5	1085.0	526	$SEGB_{63}$	64.5	1085.0	577	$SEGB_{80}$	-2128.5	1085.0
476	$SEGC_{46}$	2214.5	1085.0	527	$SEGC_{63}$	21.5	1085.0	578	$SEGC_{80}$	-2171.5	1085.0
477	$SEGA_{47}$	2171.5	1085.0	528	$SEGA_{64}$	-21.5	1085.0	579	$SEGA_{81}$	-2214.5	1085.0
478	$SEGB_{47}$	2128.5	1085.0	529	$SEGB_{64}$	-64.5	1085.0	580	$SEGB_{81}$	-2257.5	1085.0
479	$SEGC_{47}$	2085.5	1085.0	530	$SEGC_{64}$	-107.5	1085.0	581	$SEGC_{81}$	-2300.5	1085.0
480	$SEGA_{48}$	2042.5	1085.0	531	$SEGA_{65}$	-150.5	1085.0	582	$SEGA_{82}$	-2343.5	1085.0
481	$SEGB_{48}$	1999.5	1085.0	532	$SEGB_{65}$	-193.5	1085.0	583	$SEGB_{82}$	-2386.5	1085.0
482	$SEGC_{48}$	1956.5	1085.0	533	$SEGC_{65}$	-236.5	1085.0	584	$SEGC_{82}$	-2429.5	1085.0
483	$SEGA_{49}$	1913.5	1085.0	534	$SEGA_{66}$	-279.5	1085.0	585	$SEGA_{83}$	-2472.5	1085.0
484	$SEGB_{49}$	1870.5	1085.0	535	$SEGB_{66}$	-322.5	1085.0	586	$SEGB_{83}$	-2515.5	1085.0
485	$SEGC_{49}$	1827.5	1085.0	536	$SEGC_{66}$	-365.5	1085.0	587	$SEGC_{83}$	-2558.5	1085.0
486	$SEGA_{50}$	1784.5	1085.0	537	$SEGA_{67}$	-408.5	1085.0	588	$SEGA_{84}$	-2601.5	1085.0
487	$SEGB_{50}$	1741.5	1085.0	538	$SEGB_{67}$	-451.5	1085.0	589	$SEGB_{84}$	-2644.5	1085.0
488	$SEGC_{50}$	1698.5	1085.0	539	$SEGC_{67}$	-494.5	1085.0	590	$SEGC_{84}$	-2687.5	1085.0
489	$SEGA_{51}$	1655.5	1085.0	540	$SEGA_{68}$	-537.5	1085.0	591	$SEGA_{85}$	-2730.5	1085.0
490	$SEGB_{51}$	1612.5	1085.0	541	$SEGB_{68}$	-580.5	1085.0	592	$SEGB_{85}$	-2773.5	1085.0
491	$SEGC_{51}$	1569.5	1085.0	542	$SEGC_{68}$	-623.5	1085.0	593	$SEGC_{85}$	-2816.5	1085.0
492	$SEGA_{52}$	1526.5	1085.0	543	$SEGA_{69}$	-666.5	1085.0	594	$SEGA_{86}$	-2859.5	1085.0
493	$SEGB_{52}$	1483.5	1085.0	544	$SEGB_{69}$	-709.5	1085.0	595	$SEGB_{86}$	-2902.5	1085.0
494	$SEGC_{52}$	1440.5	1085.0	545	$SEGC_{69}$	-752.5	1085.0	596	$SEGC_{86}$	-2945.5	1085.0
495	$SEGA_{53}$	1397.5	1085.0	546	$SEGA_{70}$	-795.5	1085.0	597	$SEGA_{87}$	-2988.5	1085.0
496	$SEGB_{53}$	1354.5	1085.0	547	$SEGB_{70}$	-838.5	1085.0	598	$SEGB_{87}$	-3031.5	1085.0
497	$SEGC_{53}$	1311.5	1085.0	548	$SEGC_{70}$	-881.5	1085.0	599	$SEGC_{87}$	-3074.5	1085.0
498	$SEGA_{54}$	1268.5	1085.0	549	$SEGA_{71}$	-924.5	1085.0	600	$SEGA_{88}$	-3117.5	1085.0
499	$SEGB_{54}$	1225.5	1085.0	550	$SEGB_{71}$	-967.5	1085.0	601	$SEGB_{88}$	-3160.5	1085.0
500	$SEGC_{54}$	1182.5	1085.0	551	$SEGC_{71}$	-1010.5	1085.0	602	$SEGC_{88}$	-3203.5	1085.0
501	$SEGA_{55}$	1139.5	1085.0	552	$SEGA_{72}$	-1053.5	1085.0	603	$SEGA_{89}$	-3246.5	1085.0
502	$SEGB_{55}$	1096.5	1085.0	553	$SEGB_{72}$	-1096.5	1085.0	604	$SEGB_{89}$	-3289.5	1085.0
503	$SEGC_{55}$	1053.5	1085.0	554	$SEGC_{72}$	-1139.5	1085.0	605	$SEGC_{89}$	-3332.5	1085.0
504	$SEGA_{56}$	1010.5	1085.0	555	$SEGA_{73}$	-1182.5	1085.0	606	$SEGA_{90}$	-3375.5	1085.0
505	$SEGB_{56}$	967.5	1085.0	556	$SEGB_{73}$	-1225.5	1085.0	607	$SEGB_{90}$	-3418.5	1085.0
506	$SEGC_{56}$	924.5	1085.0	557	$SEGC_{73}$	-1268.5	1085.0	608	$SEGC_{90}$	-3461.5	1085.0
507	$SEGA_{57}$	881.5	1085.0	558	$SEGA_{74}$	-1311.5	1085.0	609	$SEGA_{91}$	-3504.5	1085.0
508	$SEGB_{57}$	838.5	1085.0	559	$SEGB_{74}$	-1354.5	1085.0	610	$SEGB_{91}$	-3547.5	1085.0
509	$SEGC_{57}$	795.5	1085.0	560	$SEGC_{74}$	-1397.5	1085.0	611	$SEGC_{91}$	-3590.5	1085.0
510	$SEGA_{58}$	752.5	1085.0	561	$SEGA_{75}$	-1440.5	1085.0	612	$SEGA_{92}$	-3633.5	1085.0

■ PAD COORDINATES 5

Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

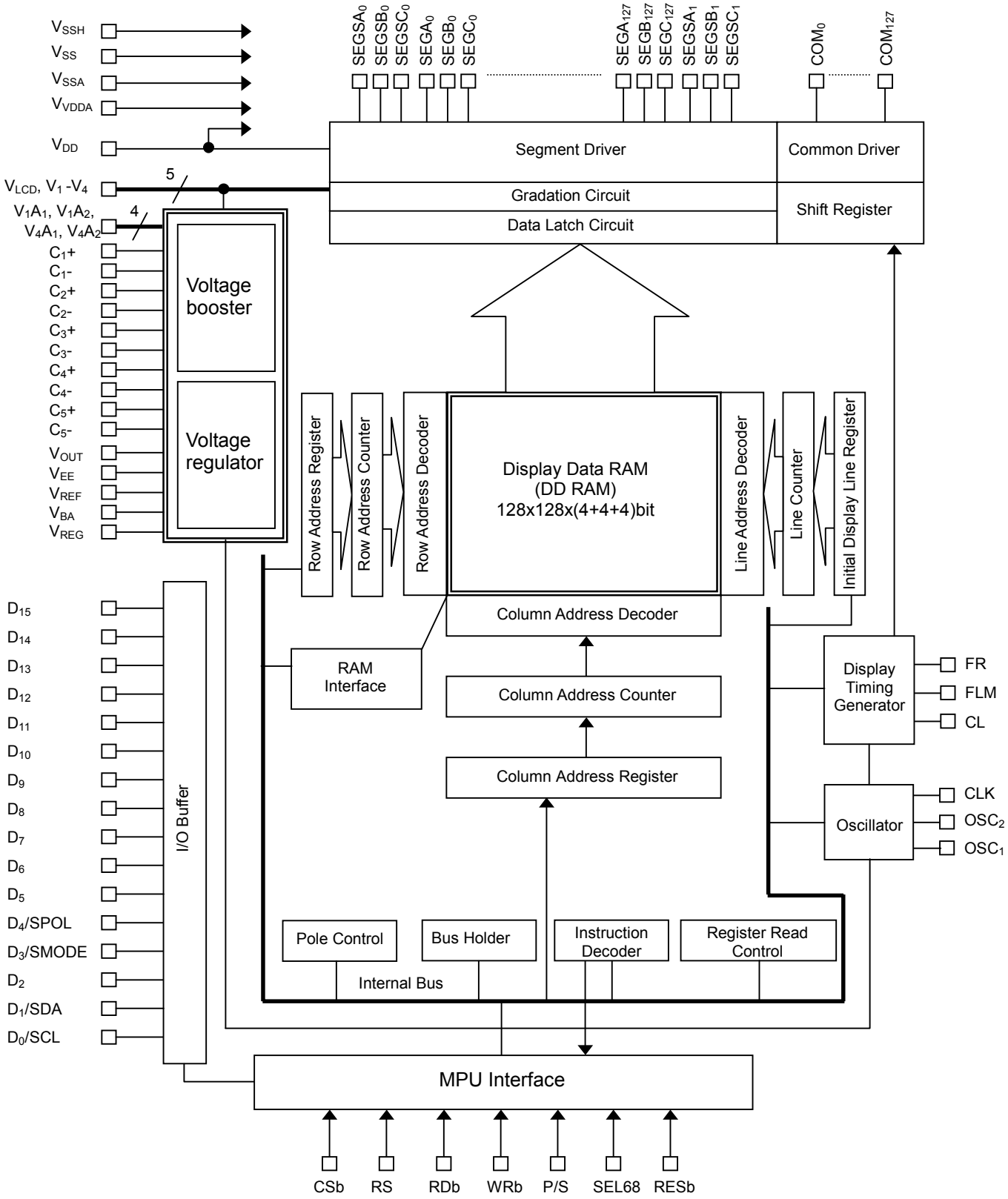
PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
613	$SEGB_{92}$	-3676.5	1085.0	664	$SEGB_{109}$	-5869.5	1085.0	715	$SEGB_{126}$	-8062.5	1085.0
614	$SEGC_{92}$	-3719.5	1085.0	665	$SEGC_{109}$	-5912.5	1085.0	716	$SEGC_{126}$	-8105.5	1085.0
615	$SEGA_{93}$	-3762.5	1085.0	666	$SEGA_{110}$	-5955.5	1085.0	717	$SEGA_{127}$	-8148.5	1085.0
616	$SEGB_{93}$	-3805.5	1085.0	667	$SEGB_{110}$	-5998.5	1085.0	718	$SEGB_{127}$	-8191.5	1085.0
617	$SEGC_{93}$	-3848.5	1085.0	668	$SEGC_{110}$	-6041.5	1085.0	719	$SEGC_{127}$	-8234.5	1085.0
618	$SEGA_{94}$	-3891.5	1085.0	669	$SEGA_{111}$	-6084.5	1085.0	720	$SEGSA_{1}$	-8277.5	1085.0
619	$SEGB_{94}$	-3934.5	1085.0	670	$SEGB_{111}$	-6127.5	1085.0	721	$SEGSB_{1}$	-8320.5	1085.0
620	$SEGC_{94}$	-3977.5	1085.0	671	$SEGC_{111}$	-6170.5	1085.0	722	$SEGSC_{1}$	-8363.5	1085.0
621	$SEGA_{95}$	-4020.5	1085.0	672	$SEGA_{112}$	-6213.5	1085.0	723	COM_{64}	-8406.5	1085.0
622	$SEGB_{95}$	-4063.5	1085.0	673	$SEGB_{112}$	-6256.5	1085.0	724	COM_{65}	-8449.5	1085.0
623	$SEGC_{95}$	-4106.5	1085.0	674	$SEGC_{112}$	-6299.5	1085.0	725	COM_{66}	-8492.5	1085.0
624	$SEGA_{96}$	-4149.5	1085.0	675	$SEGA_{113}$	-6342.5	1085.0	726	COM_{67}	-8535.5	1085.0
625	$SEGB_{96}$	-4192.5	1085.0	676	$SEGB_{113}$	-6385.5	1085.0	727	COM_{68}	-8578.5	1085.0
626	$SEGC_{96}$	-4235.5	1085.0	677	$SEGC_{113}$	-6428.5	1085.0	728	COM_{69}	-8621.5	1085.0
627	$SEGA_{97}$	-4278.5	1085.0	678	$SEGA_{114}$	-6471.5	1085.0	729	COM_{70}	-8664.5	1085.0
628	$SEGB_{97}$	-4321.5	1085.0	679	$SEGB_{114}$	-6514.5	1085.0	730	COM_{71}	-8707.5	1085.0
629	$SEGC_{97}$	-4364.5	1085.0	680	$SEGC_{114}$	-6557.5	1085.0	731	COM_{72}	-8750.5	1085.0
630	$SEGA_{98}$	-4407.5	1085.0	681	$SEGA_{115}$	-6600.5	1085.0	732	COM_{73}	-8793.5	1085.0
631	$SEGB_{98}$	-4450.5	1085.0	682	$SEGB_{115}$	-6643.5	1085.0	733	COM_{74}	-8836.5	1085.0
632	$SEGC_{98}$	-4493.5	1085.0	683	$SEGC_{115}$	-6686.5	1085.0	734	COM_{75}	-8879.5	1085.0
633	$SEGA_{99}$	-4536.5	1085.0	684	$SEGA_{116}$	-6729.5	1085.0	735	COM_{76}	-8922.5	1085.0
634	$SEGB_{99}$	-4579.5	1085.0	685	$SEGB_{116}$	-6772.5	1085.0	736	COM_{77}	-8965.5	1085.0
635	$SEGC_{99}$	-4622.5	1085.0	686	$SEGC_{116}$	-6815.5	1085.0	737	COM_{78}	-9008.5	1085.0
636	$SEGA_{100}$	-4665.5	1085.0	687	$SEGA_{117}$	-6858.5	1085.0	738	COM_{79}	-9051.5	1085.0
637	$SEGB_{100}$	-4708.5	1085.0	688	$SEGB_{117}$	-6901.5	1085.0	739	COM_{80}	-9094.5	1085.0
638	$SEGC_{100}$	-4751.5	1085.0	689	$SEGC_{117}$	-6944.5	1085.0	740	COM_{81}	-9137.5	1085.0
639	$SEGA_{101}$	-4794.5	1085.0	690	$SEGA_{118}$	-6987.5	1085.0	741	COM_{82}	-9180.5	1085.0
640	$SEGB_{101}$	-4837.5	1085.0	691	$SEGB_{118}$	-7030.5	1085.0	742	COM_{83}	-9223.5	1085.0
641	$SEGC_{101}$	-4880.5	1085.0	692	$SEGC_{118}$	-7073.5	1085.0	743	COM_{84}	-9266.5	1085.0
642	$SEGA_{102}$	-4923.5	1085.0	693	$SEGA_{119}$	-7116.5	1085.0	744	COM_{85}	-9309.5	1085.0
643	$SEGB_{102}$	-4966.5	1085.0	694	$SEGB_{119}$	-7159.5	1085.0	745	COM_{86}	-9352.5	1085.0
644	$SEGC_{102}$	-5009.5	1085.0	695	$SEGC_{119}$	-7202.5	1085.0	746	COM_{87}	-9395.5	1085.0
645	$SEGA_{103}$	-5052.5	1085.0	696	$SEGA_{120}$	-7245.5	1085.0	747	COM_{88}	-9438.5	1085.0
646	$SEGB_{103}$	-5095.5	1085.0	697	$SEGB_{120}$	-7288.5	1085.0	748	COM_{89}	-9481.5	1085.0
647	$SEGC_{103}$	-5138.5	1085.0	698	$SEGC_{120}$	-7331.5	1085.0	749	COM_{90}	-9524.5	1085.0
648	$SEGA_{104}$	-5181.5	1085.0	699	$SEGA_{121}$	-7374.5	1085.0	750	COM_{91}	-9567.5	1085.0
649	$SEGB_{104}$	-5224.5	1085.0	700	$SEGB_{121}$	-7417.5	1085.0	751	COM_{92}	-9610.5	1085.0
650	$SEGC_{104}$	-5267.5	1085.0	701	$SEGC_{121}$	-7460.5	1085.0	752	COM_{93}	-9653.5	1085.0
651	$SEGA_{105}$	-5310.5	1085.0	702	$SEGA_{122}$	-7503.5	1085.0	753	COM_{94}	-9696.5	1085.0
652	$SEGB_{105}$	-5353.5	1085.0	703	$SEGB_{122}$	-7546.5	1085.0	754	COM_{95}	-9739.5	1085.0
653	$SEGC_{105}$	-5396.5	1085.0	704	$SEGC_{122}$	-7589.5	1085.0	755	COM_{96}	-9782.5	1085.0
654	$SEGA_{106}$	-5439.5	1085.0	705	$SEGA_{123}$	-7632.5	1085.0	756	COM_{97}	-9825.5	1085.0
655	$SEGB_{106}$	-5482.5	1085.0	706	$SEGB_{123}$	-7675.5	1085.0	757	COM_{98}	-9868.5	1085.0
656	$SEGC_{106}$	-5525.5	1085.0	707	$SEGC_{123}$	-7718.5	1085.0	758	COM_{99}	-9911.5	1085.0
657	$SEGA_{107}$	-5568.5	1085.0	708	$SEGA_{124}$	-7761.5	1085.0	759	COM_{100}	-9954.5	1085.0
658	$SEGB_{107}$	-5611.5	1085.0	709	$SEGB_{124}$	-7804.5	1085.0	760	COM_{101}	-9997.5	1085.0
659	$SEGC_{107}$	-5654.5	1085.0	710	$SEGC_{124}$	-7847.5	1085.0	761	COM_{102}	-10040.5	1085.0
660	$SEGA_{108}$	-5697.5	1085.0	711	$SEGA_{125}$	-7890.5	1085.0	762	COM_{103}	-10083.5	1085.0
661	$SEGB_{108}$	-5740.5	1085.0	712	$SEGB_{125}$	-7933.5	1085.0	763	COM_{104}	-10126.5	1085.0
662	$SEGC_{108}$	-5783.5	1085.0	713	$SEGC_{125}$	-7976.5	1085.0	764	COM_{105}	-10169.5	1085.0
663	$SEGA_{109}$	-5826.5	1085.0	714	$SEGA_{126}$	-8019.5	1085.0	765	COM_{106}	-10212.5	1085.0

■ PAD COORDINATES 6

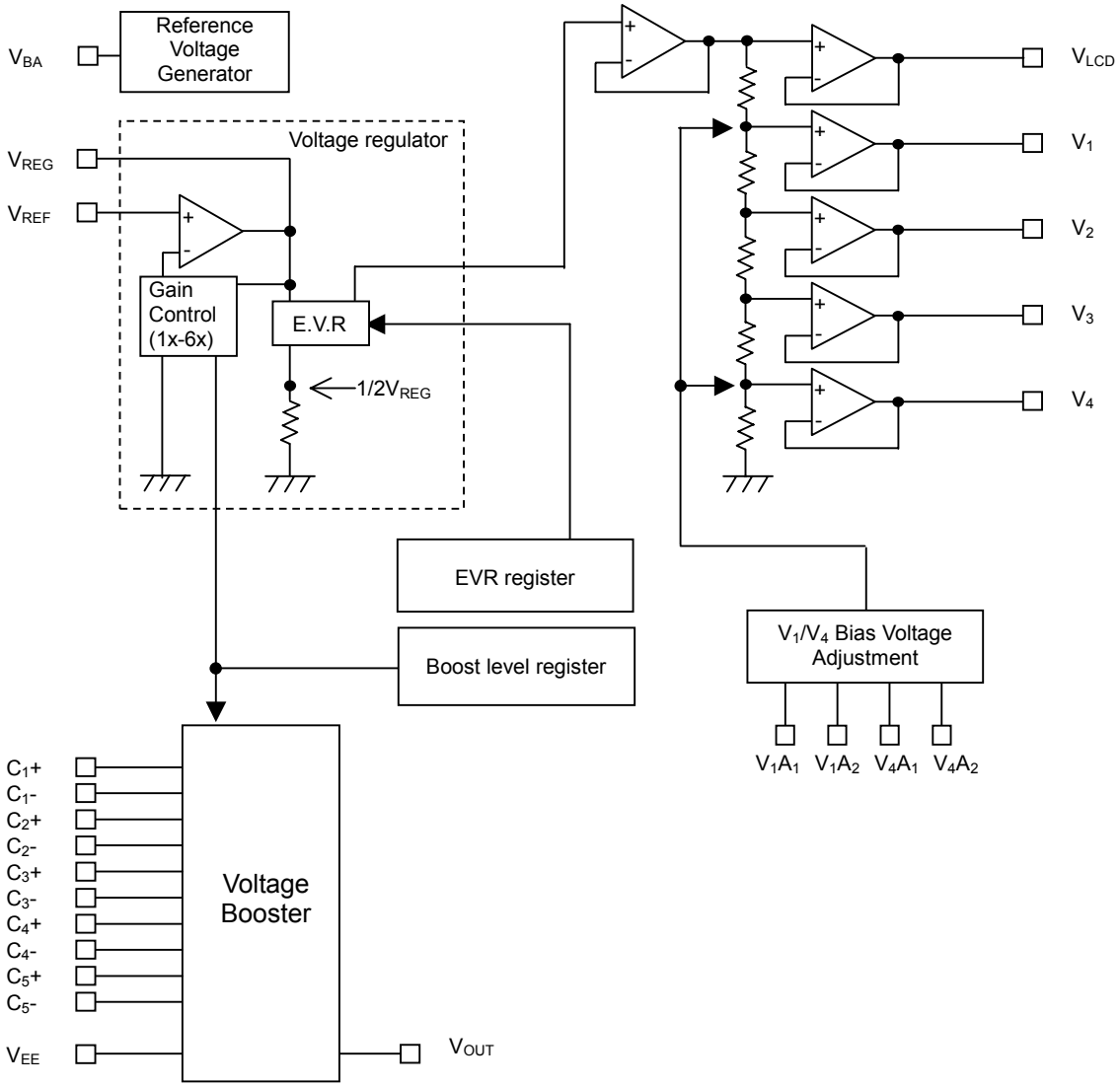
Chip Size 22070μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
766	COM_{107}	-10255.5	1085.0	817	DMY_{71}	-10845.0	-881.5				
767	COM_{108}	-10298.5	1085.0								
768	COM_{109}	-10341.5	1085.0								
769	COM_{110}	-10384.5	1085.0								
770	COM_{111}	-10427.5	1085.0								
771	COM_{112}	-10470.5	1085.0								
772	COM_{113}	-10513.5	1085.0								
773	DMY_{41}	-10556.5	1085.0								
774	DMY_{42}	-10599.5	1085.0								
775	DMY_{43}	-10642.5	1085.0								
776	DMY_{44}	-10845.0	881.5								
777	DMY_{45}	-10845.0	838.5								
778	DMY_{46}	-10845.0	795.5								
779	COM_{114}	-10845.0	752.5								
780	COM_{115}	-10845.0	709.5								
781	COM_{116}	-10845.0	666.5								
782	COM_{117}	-10845.0	623.5								
783	COM_{118}	-10845.0	580.5								
784	COM_{119}	-10845.0	537.5								
785	COM_{120}	-10845.0	494.5								
786	COM_{121}	-10845.0	451.5								
787	COM_{122}	-10845.0	408.5								
788	COM_{123}	-10845.0	365.5								
789	COM_{124}	-10845.0	322.5								
790	COM_{125}	-10845.0	279.5								
791	COM_{126}	-10845.0	236.5								
792	COM_{127}	-10845.0	193.5								
793	DMY_{47}	-10845.0	150.5								
794	DMY_{48}	-10845.0	107.5								
795	DMY_{49}	-10845.0	64.5								
796	DMY_{50}	-10845.0	21.5								
797	DMY_{51}	-10845.0	-21.5								
798	DMY_{52}	-10845.0	-64.5								
799	DMY_{53}	-10845.0	-107.5								
800	DMY_{54}	-10845.0	-150.5								
801	DMY_{55}	-10845.0	-193.5								
802	DMY_{56}	-10845.0	-236.5								
803	DMY_{57}	-10845.0	-279.5								
804	DMY_{58}	-10845.0	-322.5								
805	DMY_{59}	-10845.0	-365.5								
806	DMY_{60}	-10845.0	-408.5								
807	DMY_{61}	-10845.0	-451.5								
808	DMY_{62}	-10845.0	-494.5								
809	DMY_{63}	-10845.0	-537.5								
810	DMY_{64}	-10845.0	-580.5								
811	DMY_{65}	-10845.0	-623.5								
812	DMY_{66}	-10845.0	-666.5								
813	DMY_{67}	-10845.0	-709.5								
814	DMY_{68}	-10845.0	-752.5								
815	DMY_{69}	-10845.0	-795.5								
816	DMY_{70}	-10845.0	-838.5								

■ BLOCK DIAGRAM



■ POWER SUPPLY CIRCUITS BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Symbol	I/O	Function
64~70	V_{DD}	Power	Power supply for logic circuits
83~89	V_{SS}	Power	GND for logic circuits
154~160	V_{SSH}	Power	GND for high voltage circuits
8,9, 28,29, 92,93, 100,101	V_{DDA}	Power	This terminal is internally connected to the V_{DD} level. •This terminal is used to fix the selection terminals to the V_{DD} level. Note) Do not use this terminal for a main power supply.
4,5, 12,13, 46,47, 96,97, 104,105	V_{SSA}	Power	This terminal is internally connected to the V_{SS} level. •This terminal is used to fix the selection terminals to the V_{SS} level. Note) Do not use this terminal for a main GND.
106~111 112~117 118~123 124~129 130~135	V_{LCD} V_1 V_2 V_3 V_4	Power/O	LCD driving voltages •When the internal voltage booster is not used, external LCD driving voltages (V_1 to V_4 and V_{LCD}) must be supplied on these terminals. The external voltages must be maintained with the following relation. $V_{SS}<V_4<V_3<V_2<_{V1}<V_{LCD}$ • When the internal voltage booster is used, the LCD driving voltages (V_1 to V_4 and V_{LCD}) are enabled by the "Power control" instruction. The capacitors between the V_{SS} and these terminals are necessary.
175~180 181~186	C_1+ C_1-	O	Capacitor connection terminals for the voltage booster
187~192 193~198	C_2+ C_2-	O	Capacitor connection terminals for the voltage booster
199~204 205~210	C_3+ C_3-	O	Capacitor connection terminals for the voltage booster
211~216 217~222	C_4+ C_4-	O	Capacitor connection terminals for the voltage booster
223~228 229~234	C_5+ C_5-	O	Capacitor connection terminals for the voltage booster
148~153	V_{BA}	O	Output of the reference-voltage generator
142~147	V_{REF}	I	Input of the voltage regulator
168~174	V_{EE}	Power	Input of the voltage booster •This terminal is normally connected to the V_{DD} level.
161~167	V_{OUT}	Power/O	Output of the voltage booster Input for high voltage circuits in using external power supply
136~141	V_{REG}	O	Output of the voltage regulator
90,91 94,95	V_1A_1 V_1A_2	I	V_1 bias voltage adjustment terminal
98,99 102,103	V_4A_1 V_4A_2	I	V_4 bias voltage adjustment terminal
14,15	RESb	I	Reset Active "0"
6,7	SEL68	I	MPU interface type select SEL86 | H | L Status | 68 series | 80 series

■ TERMINAL DESCRIPTION 2

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>30,31</td><td>D_0/SCL</td><td>I/O</td><td rowspan="5">Parallel interface:
D_7 to D_0 : 8-bit bi-directional bus
• In the parallel interface mode (P/S="1"), these terminals connect to 8-bit bi-directional MPU bus.

Serial interface:
SDA : serial data
SCL : serial clock
SMODE : 3-/4-line serial interface mode selection
SPOL : RS polarity selection (in the 3-line serial interface mode)
•In the 3-/4-line serial interface mode (P/S="0"), the D0 terminal is assigned to the SCL and the D_1 terminal to the SDA.
•In the 3-line serial interface mode, the D_4 terminal is assigned to the SPOL.
•Serial data on the SDA is fetched at the rising edge of the SCL signal in the order of the D_7, D_6…D_0, and the fetched data is converted into 8-bit parallel data at the falling edge of the 8th SCL signal.
•The SCL signal must be set to "0" after data transmissions or during non-access.</td></tr>
<tr><td>32,33</td><td>D_1/SDA</td><td>I/O</td></tr>
<tr><td>36,37</td><td>D_3/SMODE</td><td>I/O</td></tr>
<tr><td>38,39</td><td>D_4/SPOL</td><td>I/O</td></tr>
<tr><td>34,35
40,41
42,43
44,45</td><td>D_2
D_5
D_6
D_7</td><td>I/O</td></tr>
<tr><td>48,49
50,51
52,53
54,55
56,57
58,59
60,61
62,63</td><td>D_8
D_9
D_{10}
D_{11}
D_{12}
D_{13}
D_{14}
D_{15}</td><td>I/O</td><td>8-bit bi-directional bus
•In the 16-bit data bus mode, these terminals are assigned to the upper 8-bit data bus.
•In the serial interface mode or 8-bit data bus mode of the parallel interface, these terminals must be fixed to "1" or "0".</td></tr>
<tr><td>17,18</td><td>CSb</td><td>I</td><td>Chip select
Active "0"</td></tr>
<tr><td>20,21</td><td>RS</td><td>I</td><td>Resister select
•This signal distinguishes transferred data as an instruction or display data as follows.
<table><tr><td>RS</td><td>H</td><td>L</td></tr><tr><td>Distinct.</td><td>Instruction</td><td>Display data</td></tr></table></td></tr>
<tr><td>26,27</td><td>RDb (E)</td><td>I</td><td>80 series MPU interface (P/S="1", SEL68="0")
RDb signal. Active "0".

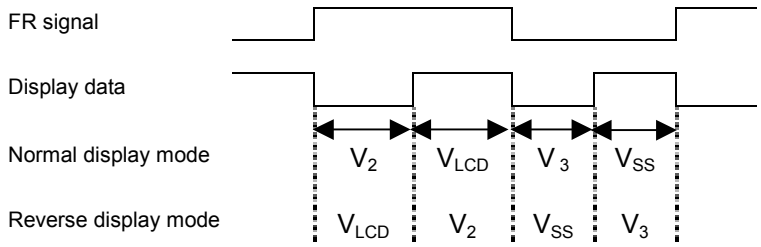
68 series MPU interface (P/S="1", SEL68="1")
Enable signal. Active "1".</td></tr>
<tr><td>23,24</td><td>WRb (R/W)</td><td>I</td><td>80 series MPU interface (P/S="1", SEL68="0")
WRb signal. Active "0".

68 series MPU interface (P/S="1", SEL68="1")
R/W signal.
<table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table></td></tr>
</table>

■ TERMINAL DESCRIPTION 3

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>10,11</td><td>P/S</td><td>I</td><td>Parallel / serial interface mode selection
<table>
<tr><th>P/S</th><th>Chip Select</th><th>Data/ Instruction</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>CSb</td><td>RS</td><td>D_0 ~ D_7</td><td>RDb, WRb</td><td>-</td></tr>
<tr><td>L</td><td>CSb</td><td>RS</td><td>SDA (D_1)</td><td>Write only</td><td>SCL (D_0)</td></tr>
</table>
•Since the D_{15} to D_5 and D_2 terminals are in the high impedance in the serial inter face mode (P/S=”0”), they must be fixed to “1” or “0”. The RDb and WRb terminals also must be “1” or “0”.</td></tr>
<tr><td>71,72</td><td>CL</td><td>O</td><td>This terminal must be opened.</td></tr>
<tr><td>73,74</td><td>FLM</td><td>O</td><td>This terminal must be opened.</td></tr>
<tr><td>75,76</td><td>FR</td><td>O</td><td>This terminal must be opened.</td></tr>
<tr><td>77,78</td><td>CLK</td><td>O</td><td>This terminal must be opened.</td></tr>
<tr><td>79,80
81,82</td><td>OSC_1
OSC_2</td><td>I
O</td><td>OSC
• When the internal oscillator clock is used, OSC_1 terminal must be fixed to “1” or “0”, and the OSC_2 terminal must be opened. When the oscillation frequency from the internal oscillator is adjusted by an external resistor between OSC_1 terminal and OSC_2.
• When an external oscillator is used, external clock is input to the OSC_1 terminal or an external resistor is connected between the OSC_1 and OSC_2 terminals.</td></tr>
</table>

■ TERMINAL DESCRIPTION 4

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>336~719</td><td>$SEGA_0$ ~ $SEGA_{127}$,
$SEGB_0$ ~ $SEGB_{127}$,
$SEGC_0$ ~ $SEGC_{127}$</td><td>O</td><td>Segment output
<table><tr><th>REV Mode</th><th>Turn-off</th><th>Turn-on</th></tr><tr><td>Normal</td><td>0</td><td>1</td></tr><tr><td>Reverse</td><td>1</td><td>0</td></tr></table>•These terminals output LCD driving waveforms in accordance with the combination of the FR signal and display data.
<u>In the B/W mode</u>
  </td></tr>
<tr><td>333,720
334,721
335,722</td><td>$SEGSA_0$, $SEGSA_1$
$SEGSB_0$, $SEGSB_1$
$SEGSC_0$, $SEGSC_1$</td><td>O</td><td>Icon segment output terminal
•These terminals are assigned at both edge of normal segment output terminals line for out line frame display.</td></tr>
<tr><td>332~283,
276~263,
723~772,
779~792</td><td>COM_0 ~ COM_{127}</td><td>O</td><td>Common output
•These terminals output LCD driving waveforms in accordance with the combination of the FR signal and scanning data.
<table><tr><th>Data</th><th>FR</th><th>Output level</th></tr><tr><td>H</td><td>H</td><td>V_{SS}</td></tr><tr><td>L</td><td>H</td><td>V_1</td></tr><tr><td>H</td><td>L</td><td>V_{LCD}</td></tr><tr><td>L</td><td>L</td><td>V_4</td></tr></table></td></tr>
</table>

(Terminal No. 1~3,16,19,22,25,235~262,277~282,773~778,793~817 are dummy.)

■ Functional Description

(1) MPU Interface

(1-1) Selection of parallel / serial interface mode

The P/S terminal is used to select parallel or serial interface mode as shown in the following table. In the serial interface mode, it is not possible to read out display data from the DDRAM and status from the internal registers.

Table1

P/S	P/S mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D_7-D_0 (D_{15}-D_0)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

Note 1) " -" : Fix to "1" or "0".

(1-2) Selection of MPU interface type

In the parallel interface mode, the SEL68 terminal is used to select 68- or 80-series MPU interface type as shown in the following table.

Table2

SEL68	MPU type	CSb	RS	RDb	WRb	Data
H	68 series MPU	CSb	RS	E	R/W	D_7-D_0 (D_{15}-D_0)
L	80 series MPU	CSb	RS	RDb	WRb	D_7-D_0 (D_{15}-D_0)

(1-3) Data distinction

In the parallel interface mode, the combination of RS, RDb, and WRb (R/W) signals distinguishes transferred data between the LSI and MPU as instruction or display data, as shown in the following table.

Table3

RS	68 series	80 series		Function
	R/W	RDb	WRb	
H	H	L	H	Read out instruction data
H	L	H	L	Write instruction data
L	H	L	H	Read out display data
L	L	H	L	Write display data

(1-4) Selection of serial interface mode

In the serial interface mode, the SMODE terminal is used to select the 3- or 4-line serial interface mode as shown in the following table.

Table4

SMODE	Serial interface mode
H	3-line
L	4-line

(1-5) 4-line serial interface mode

In the 4-line serial interface mode, when the chip select is active (CSb="0"), the SDA and the SCL are enabled. When the chip select is not active (CSb="1"), the SDA and the SCL are disabled and the internal shift register and the counter are being initialized. The 8-bit serial data on the SDA is fetched at the rising edge of the SCL signal (serial clock) in order of the D_7, D_6…D_0, and the fetched data is converted into the 8-bit parallel data at the rising edge of the 8th SCL signal.

In the 4-line serial interface mode, the transferred data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS signal.

Table5

RS	Data distinction
H	Instruction data
L	Display data

Since the serial interface operation is sensitive to external noises, the SCL should be set to "0" after data transmissions or during non-access. To release a mal-function caused by the external noises, the chip-selected status should be released (CSb="1") after each of the 8-bit data transmissions. The following figure illustrates the interface timing for the 4-line serial interface operation.

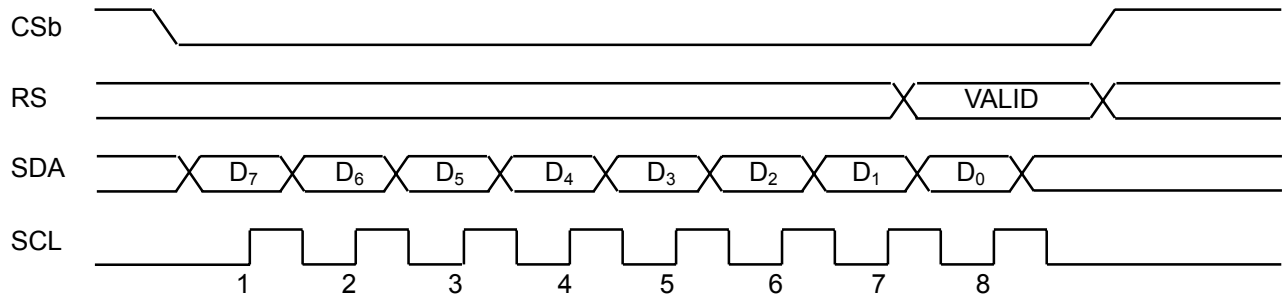


Fig1 4-line serial interface timing

(1-6) 3-line serial interface mode

In the 3-line serial interface mode, when the chip select is active (CSb="0"), the SDA and SCL are enabled. When the chip select is not active (CSb="1"), the SDA and SCL are disabled and the internal shift register and counter are being initialized. 9-bit serial data on the SDA is fetched at the rising edge of the SCL signal in order of the RS, D_7, D_6…D_0, and the fetched data is converted into the 9-bit parallel data at the rising edge of the 9th SCL signal.

In the 3-line serial interface mode, data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS bit of the SDA data and the status of the SPOL, as follows.

Table6

SPOL=L		SPOL=H	
RS	Data distinction	RS	Data distinction
L	Display data	L	Instruction data
H	Instruction data	H	Display data

Since the serial interface operation is sensitive to external noises, the SCL must be set to “0” after data transmissions or during non-access. To release a mal-function caused by the external noises, the chip-selected status should be released (CSb=“1”) after each of 9-bit data transmissions. The following figure illustrates the interface timing of the 3-line serial interface operation.

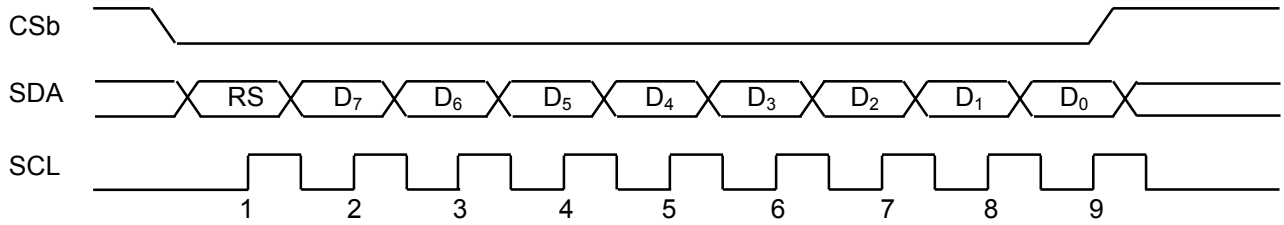


Fig2 3-line serial interface timing

(2) Access to the DDRAM

When the CSb signal is ”0”, the transferred data from MPU is written into the DDRAM or instruction register in accordance with the condition of the RS signal.

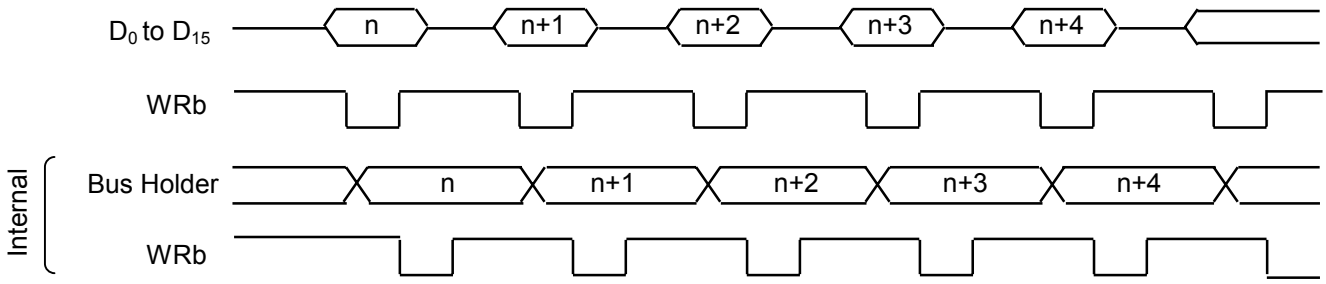
When the RS signal is “1”, the transferred data is distinguished as display data. After the “column address” and “row address” instructions are executed, the display data can be written into the DDRAM by the “display data write” instruction. The display data is written at the rising edge of the WRb signal in the 80 series MPU mode, or at the falling edge of the E signal in the 68 series MPU mode.

Table6

RS	Data
L	Display RAM Data
H	Internal Command Register

In the sequence of the “display data read” operation, the transferred data from MPU is temporarily held in the internal bus-holder, then transferred to the internal data-bus. When the “display data read” operation is executed just after the “column address” and “row address” instructions or “display data write” instruction, unexpected data on the bus-holder is read out at the 1st execution, then the data of designated DDRAM address is read out from the 2nd execution. For this reason, a dummy read cycle must be executed to avoid the unexpected 1st data read.

Display data write operation



Display data read operation

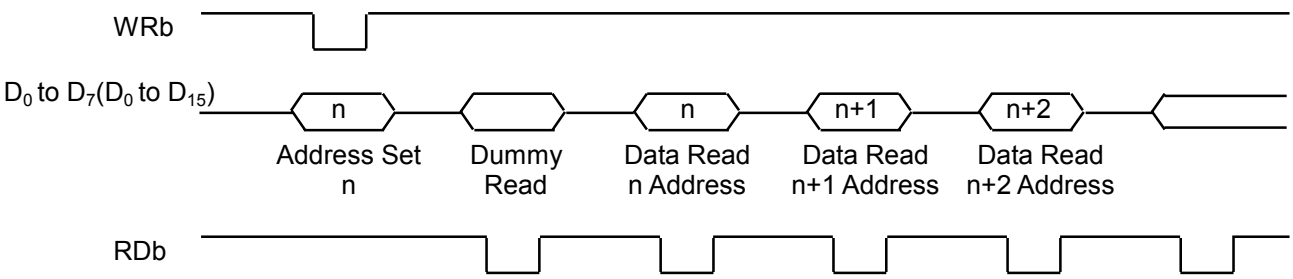


Fig3

Note) In the16-bit data bus mode, instruction data must be 16-bit as well as the display data.

(3) Access to the instruction register

Each instruction resisters is assigned to each address between 0_H and F_H, and the content of the instruction register can be read out by the combination of the “Instruction resister address” and ”Instruction resister read”.

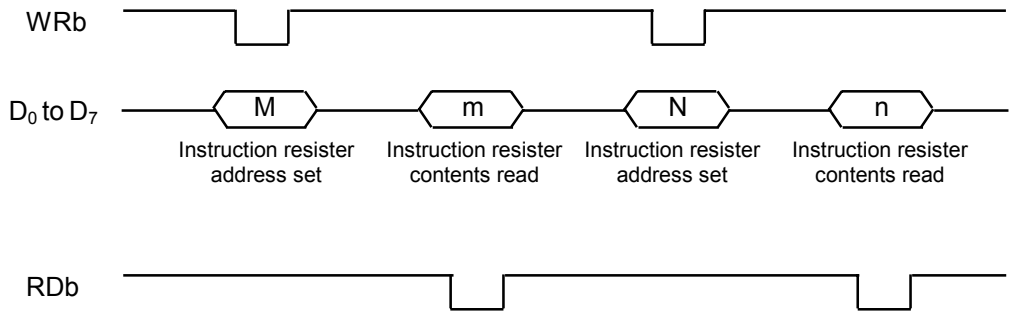


Fig4

(4) 8-/16-bit data bus length for display data (in the parallel interface mode)

The 8- or 16-bit data bus length for display data is determined by the “WLS” of the “Data bus length” instruction.

In the 16-bit data bus mode, instruction data must be 16-bit data (D_{15} to D_0) as well as display data. However, for the access to the instruction register, the only lower 8-bit data (D_7 to D_0) of the 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

Table8

WLS	Data bus length mode
L	8-bit
H	16-bit

(5) Initial display line register

The initial display line resister specifies the line address, corresponding to the initial COM line, by the “Initial display line” instruction. The initial COM line signifies the common driver, starting scanning the display data in the DDRAM, and specified by the “Initial COM line” instruction.

The line address, established in the initial display line resister, is preset into the line counter whenever the FLM signal becomes “1”. At the rising edge of the CL signal, the line counter is counted-up and addressed 384-bit display data corresponding to the counted-up line address, is latched into the data latch circuit. At the falling edge of the CL signal, the latched data outputs to the segment drivers.

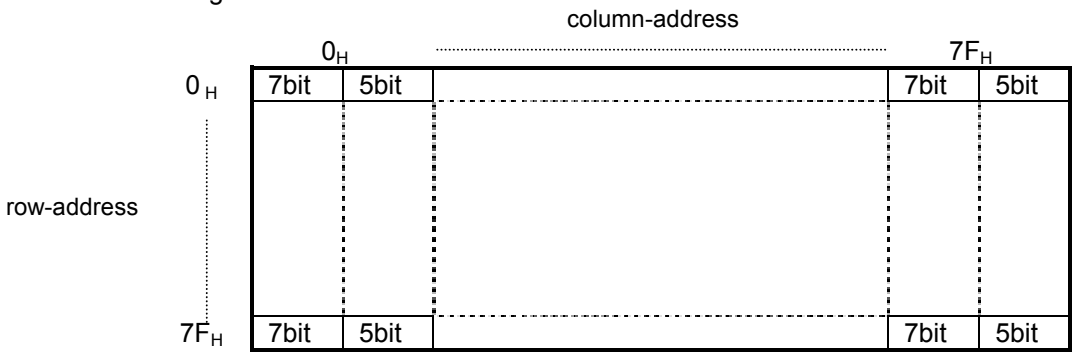
(6) DDRAM mapping

The DDRAM is capable of 1,536-bit (12-bit x 128-segment) for the column address and 128-bit for the row address.

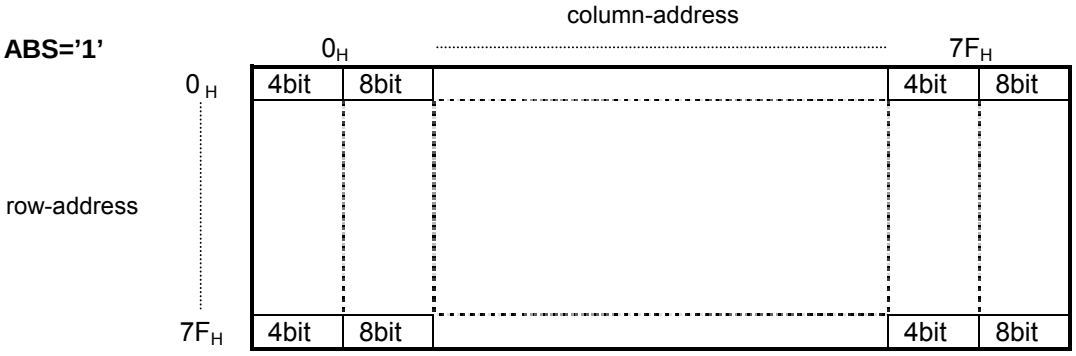
In the gradation mode, each pixel for RGB corresponds to successive 3-segment drivers, and each segment driver has 16-gradation. Therefore, the LSI can drive up to 128x128 pixels in 4096-color display (16-gradation x 16-gradation x 16-gradation).

In 8-bit access mode(C256 mode) for DDRAM, sequential twice accesses to DDRAM complete one pixel data access. Therefore, it must be accessed with a couple of operation.

- In the 8-bit data bus length mode



ABS='1'



C256='1'

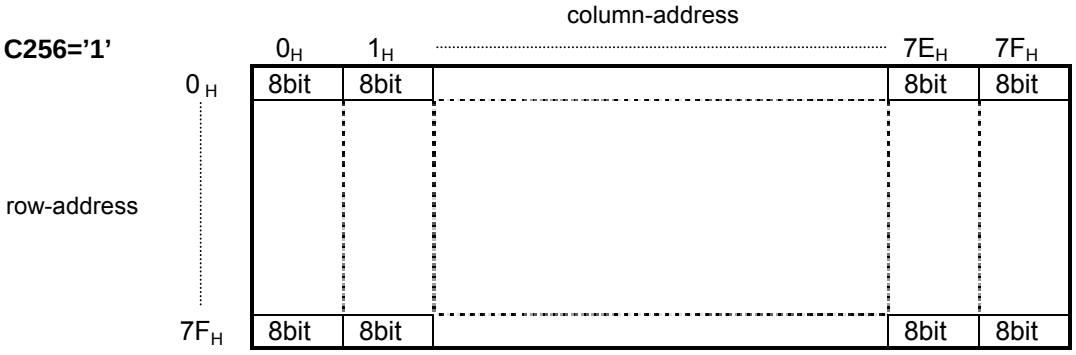


Fig5

- In the 16-bit data bus length mode

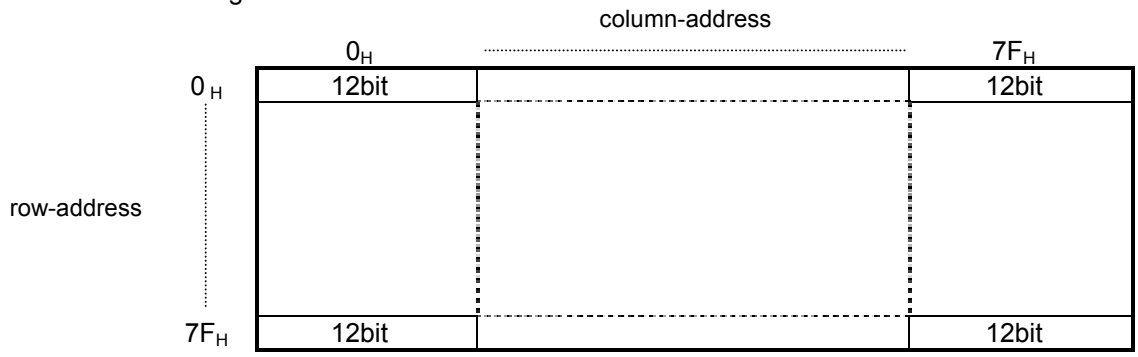


Fig6

In the B&W mode, only MSB data from each 4-bit display data group in the DDRAM is used. Therefore, 384 x 128 pixels in the B&W and 128 x 128 pixels in the 8-gradation are available.

The range of the column address varies depending on data bus length. The range between 00_H and $7F_H$ is used in the 8-bit or 16-bit data bus length.

The DDRAM is accessing 8-bit or 16-bit unit addressed by column and row address. In the 8-bit or 16-bit data bus length mode, over 80_H address setting is prohibited.

The increments for the column address and row address are set to the auto-increment mode by programming the “HV”, “XD” and “YD” registers of the “Increment control” instruction. In this mode, the contents of the column address and row address counters automatically increment whenever the DDRAM is accessed.

The column address and row address counters, independent of the line counter. They are used to designate the column and row addresses for the display data transferred from MPU. On the other hand, the line counter is used to generate the line address, and output display data to the segment drivers, being synchronized with the display control timing of the FLM and CL signals.

RAM Map 1

Mode	WLS	ABS	256	SEG0												SEG1												SEG126												SEG127											
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
				A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
16bit	1	0	0	X=00H												X=01H												X=7EH												X=7FH											
				D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1
	1	1	0	X=00H												X=01H												X=7EH												X=7FH											
				D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8bit	0	0	0	X=00H (Upper)							X=00H (Lower)					X=01H (Upper)							X=01H (Lower)					X=7EH (Upper)							X=7EH (Lower)				X=7FH (Upper)							X=7FH (Lower)			
				D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1
	0	1	0	X=00H (Upper)				X=00H (Lower)								X=01H (Upper)				X=01H (Lower)								X=7EH (Upper)				X=7EH (Lower)								X=7FH (Upper)				X=7FH (Lower)							
				D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

RAM Map 2 (256 Color Mode)

Mode	WLS	ABS	256	SEG0												SEG1												SEG126												SEG127											
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
				A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
8bit	0	X	1	X=00H												X=01H												X=7EH												X=7FH											
				-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0

SWAP

SWAP	Palette A				Palette B				Palette C			
	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
0	SEGAx				SEGBx				SEGCx			
1	SEGCx				SEGBx				SEGAx			

Note1) In the 256-color mode, the vacant LSB bit is filled with "1".
Note2) The function of 256-color mode is different from that of fixed 8-gradation mode (fixed 256-color mode).
Note3) The written data in the DD RAM in "C256"=0 is not compatible with the data in "C256"=1.
Note4) In the 256-color mode, only 8-bit length mode is available, but 16-bit is not.
Note5) In 8-bit access mode(C256 mode) for DDRAM, sequential twice accesses to DDRAM complete one pixel data access. Therefore, it must be accessed with a couple of operation.
Note6) In 8-bit access mode(non C256 mode) for DDRAM, After address set up display data will be written in an order from lower to higher.
This order has no relation with address direction of RAM access (Display rotation)

Icon Segment Map 1

Mode	WLS	ABS	256	SEGS0												SEGS1											
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
				A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
16bit	1	0	0	X=00H												X=01H											
				D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1
	1	1	0	X=00H												X=01H											
				D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8bit	0	0	0	X=00H (Upper)							X=00H (Lower)					X=01H (Upper)							X=01H (Lower)				
				D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1
	0	1	0	X=00H (Upper)				X=00H (Lower)								X=01H (Upper)				X=01H (Lower)							
				D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

Icon Segment Map 2 (256 Color Mode)

Mode	WLS	ABS	256	SEGS0												SEGS1											
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
				A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
8bit	0	X	1	X=00H												X=01H											
				-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0

SWAP

SWAP	Palette A				Palette B				Palette C			
	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
0	SEGSAx				SEGSBx				SEGSCx			
1	SEGSCx				SEGSBx				SEGSAx			

Note1) In the 256-color mode, the vacant LSB bit is filled with "1".
Note2) The function of 256-color mode is different from that of fixed 8-gradation mode (fixed 256-color mode).
Note3) The written data in the DD RAM in "C256"=0 is not compatible with the data in "C256"=1.
Note4) In the 256-color mode, only 8-bit length mode is available, but 16-bit is not.
Note5) In 8-bit access mode(C256 mode) for DDRAM, sequential twice accesses to DDRAM complete one pixel data access. Therefore, it must be accessed with a couple of operation.
Note6) In 8-bit access mode(non C256 mode) for DDRAM, After address set up display data will be written in an order from lower to higher.
This order has no relation with address direction of RAM access (Display rotation)

(7) Window addressing mode

Window area must be designated before RAM access.

In the window addressing mode, the address space of the DDRAM designated by the start and end point is defined. The start point is determined by the “column address” and “row address” instructions, and the end point is determined by the “Window end column address “and ”Window end row address” instructions. The setting for the window addressing is listed in the following.

1. “Increment control” instruction set (HV, XD, YD)
2. Set the start point by the “column address” and “row address” instructions
3. Set the end point by the “Window end column address” and “Window end row address” instructions
4. Enable to access to the DDRAM in the window addressing mode

In addition, the read-modify-write operation is available by setting “AIM” register to ”L” in the “Increment control” instruction.

For the window area designation, the address directions of RAM (HV, XD, YD) must be set first, and Column address and Row of Start point must be set second, Column address and Row of Stop point must be set third, then RAM should be accessed. Low address must be set first and High address must be set second in all of addresses. The directions of HV, XD, YD should be check to keep the area in RAM.

And in the window addressing mode, the following start and end point must be maintained to abide a malfunction.

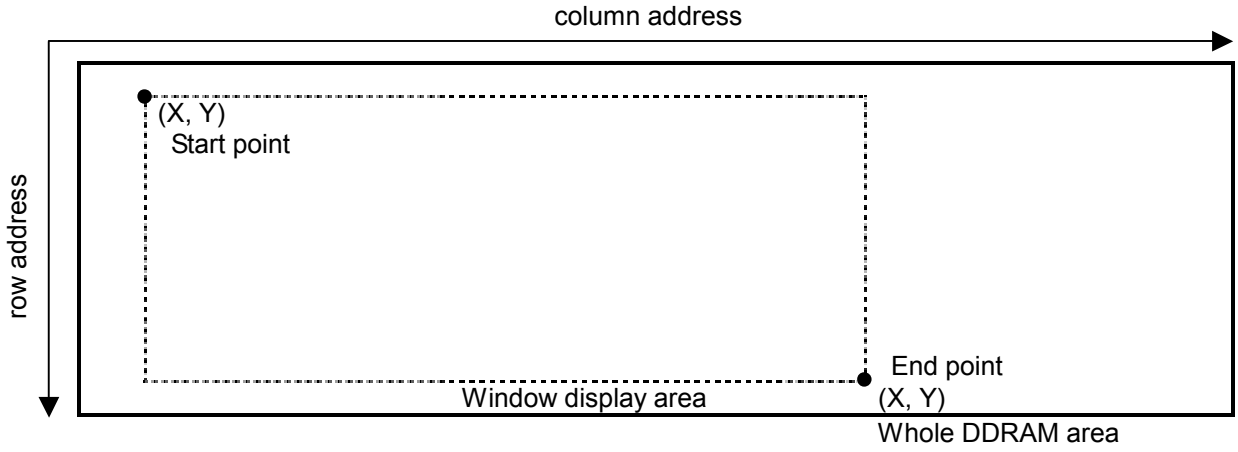


Fig7

(8) Reverse display ON/OFF

The “Reverse display ON/OFF” function is used to reverse the display data without changing the contents of the DDRAM.

Table9

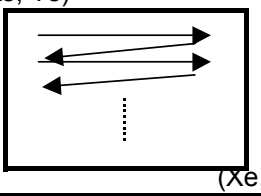
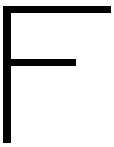
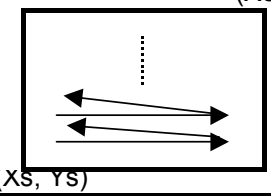
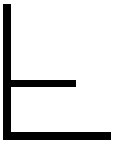
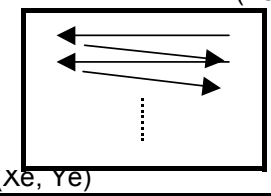
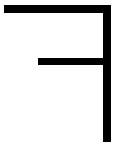
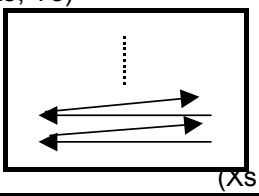
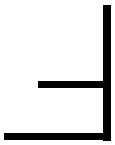
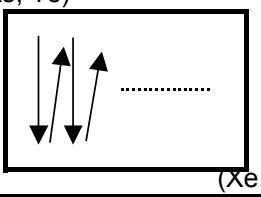
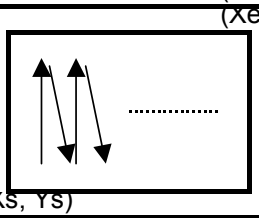
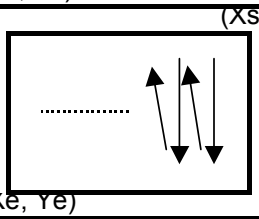
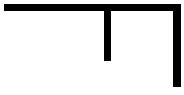
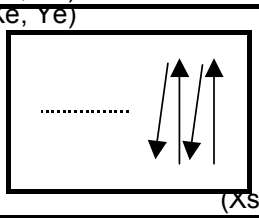
REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(9) Address directions of RAM access (Display rotation)

The bellow picture shows display image after set of HV, XD and YD for address directions. The display data from CPU can be written into RAM with rotation to 90 degrees or 180 degrees or 270 degrees, and also mirrored.

The address directions of RAM access is set by HV, XD and YD.

* : The segments of Icon are not rotated.

No	HV	XD	YD	Data writing direction	Display image	Valid address
1	0	0	0	(Xs, Ys)  (Xe, Ye)		Xs < Xe Ys < Ye
2	0	0	1	(Xe, Ye)  (Xs, Ys)		Xs < Xe Ys > Ye
3	0	1	0	(Xs, Ys)  (Xe, Ye)		Xs > Xe Ys < Ye
4	0	1	1	(Xe, Ye)  (Xs, Ys)		Xs > Xe Ys > Ye
5	1	0	0	(Xs, Ys)  (Xe, Ye)		Xs < Xe Ys < Ye
6	1	0	1	(Xe, Ye)  (Xs, Ys)		Xs < Xe Ys > Ye
7	1	1	0	(Xs, Ys)  (Xe, Ye)		Xs > Xe Ys < Ye
8	1	1	1	(Xe, Ye)  (Xs, Ys)		Xs > Xe Ys > Ye

*:The display image shows the display direction when the same data as No.1 are written into RAM for condition change.

*: The outside address of RAM must not be set for correct operation.
Xs : start address of X , Ys : Start address of Y, Xe : End address of X, Ye : End address of Y

(10) The relationship among the DDRAM column address, display data and segment drivers

In the color mode, and 16-bit data bus mode

ABS	SWAP	Column address / bit / segment assign																									
0	0	X=00_H												←→	X=$7F_H$												
		D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
		palette A				palette B				palette C				←→	palette A				palette B				palette C			
		$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

ABS	SWAP	Column address / bit / segment assign																									
0	1	X=00_H												←→	X=$7F_H$												
		D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
		palette A				palette B				palette C				←→	palette A				palette B				palette C			
		$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

ABS	SWAP	Column address / bit / segment assign																									
1	0	X=00_H												←→	X=$7F_H$												
		D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette A				palette B				palette C				←→	palette A				palette B				palette C			
		$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

ABS	SWAP	Column address / bit / segment assign																									
1	1	X=00_H												←→	X=$7F_H$												
		D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette A				palette B				palette C				←→	palette A				palette B				palette C			
		$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

In the color mode, and 8-bit data bus mode

ABS	SWAP	Column address / bit / segment assign																									
0	0	X=00_H(Upper)							X=00_H(Lower)					←→	X=$7F_H$(Upper)							X=$7F_H$(Lower)					
		D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	←→	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
		palette A				palette B			palette C					←→	palette A				palette B			palette C					
		$SEGA_0$				$SEGB_0$			$SEGC_0$					←→	$SEGA_{127}$				$SEGB_{127}$			$SEGC_{127}$					

ABS	SWAP	Column address / bit / segment assign																									
0	1	X=00_H(Upper)							X=00_H(Lower)					←→	X=$7F_H$(Upper)							X=$7F_H$(Lower)					
		D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	←→	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
		palette A				palette B			palette C					←→	palette A				palette B			palette C					
		$SEGC_0$				$SEGB_0$			$SEGA_0$					←→	$SEGC_{127}$				$SEGB_{127}$			$SEGA_{127}$					

ABS	SWAP	Column address / bit / segment assign																									
1	0	X=00_H(Upper)				X=00_H(Lower)								←→	X=$7F_H$(Upper)				X=$7F_H$(Lower)								
		D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette A				palette B				palette C				←→	palette A				palette B				palette C			
		$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

ABS	SWAP	Column address / bit / segment assign																									
1	1	X=00_H(Upper)				X=00_H(Lower)								←→	X=$7F_H$(Upper)				X=$7F_H$(Lower)								
		D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette A				palette B				palette C				←→	palette A				palette B				palette C			
		$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

In the color mode, 8-bit data bus mode, and C256 mode (C256=1)

ABS	SWAP	Column address / bit / segment assign																
*	0	X=00_H								←→	X=$7F_H$							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette A			palette B			palette C		←→	palette A			palette B			palette C	
		$SEGA_0$			$SEGB_0$			$SEGC_0$		←→	$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$	

ABS	SWAP	Column address / bit / segment assign																
*	1	X=00_H								←→	X=$7F_H$							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette A			palette B			palette C		←→	palette A			palette B			palette C	
		$SEGC_0$			$SEGB_0$			$SEGA_0$		←→	$SEGC_{127}$			$SEGB_{127}$			$SEGA_{127}$	

In the B&W mode, and 16-bit data bus mode

ABS	SWAP	Column address / bit / segment assign																													
0	0	X=00$_H$															←→	X=7F$_H$													
		D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		$SEGA_0$					$SEGB_0$						$SEGC_0$					←→	$SEGA_{127}$					$SEGB_{127}$						$SEGC_{127}$			

ABS	SWAP	Column address / bit / segment assign																													
0	1	X=00$_H$															←→	X=7F$_H$													
		D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		$SEGC_0$					$SEGB_0$						$SEGA_0$					←→	$SEGC_{127}$					$SEGB_{127}$						$SEGA_{127}$			

ABS	SWAP	Column address / bit / segment assign																													
1	0	X=00$_H$															←→	X=7F$_H$													
		D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
						$SEGA_0$				$SEGB_0$				$SEGC_0$				←→					$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

ABS	SWAP	Column address / bit / segment assign																													
1	1	X=00$_H$															←→	X=7F$_H$													
		D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
						$SEGC_0$				$SEGB_0$				$SEGA_0$				←→					$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

In the B&W mode, and 8-bit data bus mode

ABS	SWAP	Column address / bit / segment assign																									
0	0	X=00_H(Upper)							X=00_H(Lower)					←→	X=$7F_H$(Upper)							X=$7F_H$(Lower)					
		D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	←→	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
		$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$				

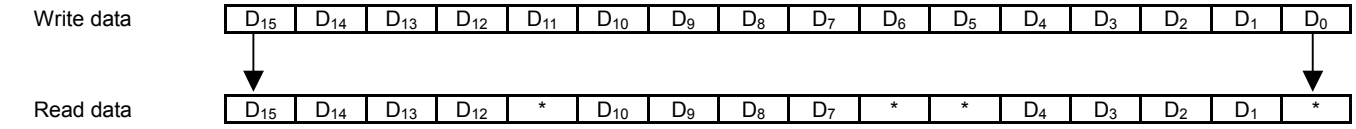
ABS	SWAP	Column address / bit / segment assign																									
0	1	X=00_H(Upper)							X=00_H(Lower)					←→	X=$7F_H$(Upper)							X=$7F_H$(Lower)					
		D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	←→	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
		$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$				

ABS	SWAP	Column address / bit / segment assign																									
1	0	X=00_H(Upper)				X=00_H(Lower)								←→	X=$7F_H$(Upper)				X=$7F_H$(Lower)								
		D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

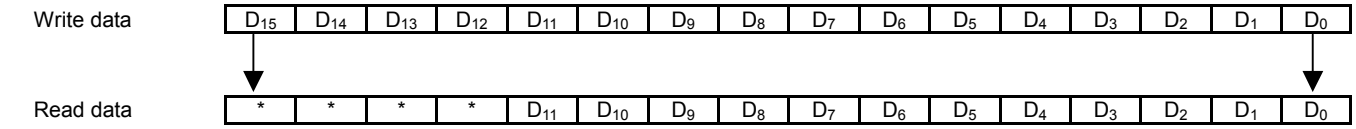
ABS	SWAP	Column address / bit / segment assign																									
1	1	X=00_H(Upper)				X=00_H(Lower)								←→	X=$7F_H$(Upper)				X=$7F_H$(Lower)								
		D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

Bit assignments between write and read data (in the 16-bit data bus mode)

ABS=0

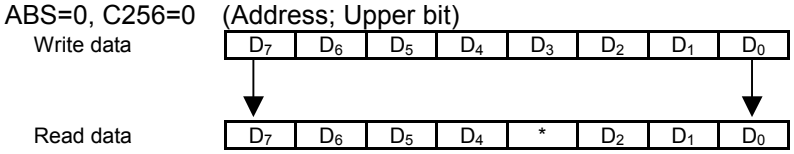


ABS=1

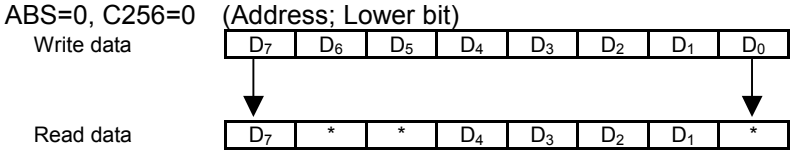


Examples of write and read data (In the 8 bit bus mode)

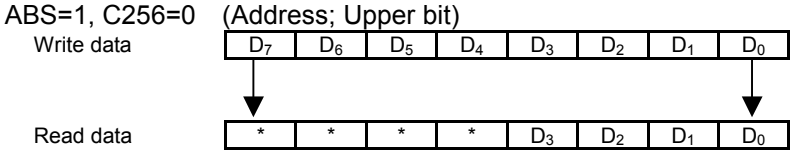
ABS=0, C256=0 (Address; Upper bit)



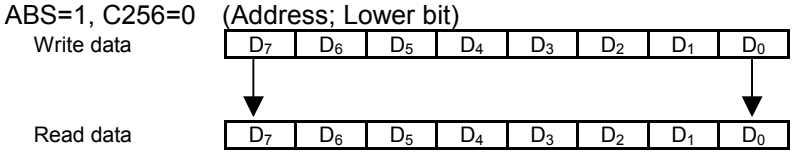
ABS=0, C256=0 (Address; Lower bit)



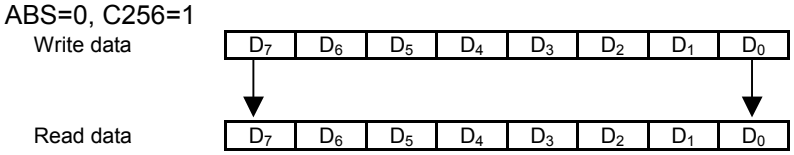
ABS=1, C256=0 (Address; Upper bit)



ABS=1, C256=0 (Address; Lower bit)



ABS=0, C256=1



*: Invalid Data

Icon segment register address bit assignment

In the color mode, and 16-bit data bus mode

ABS	SWAP	Column address / bit / segment assign																							
0	0	X=00_H												X=01_H											
		D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
		palette A				palette B				palette C				palette A				palette B				palette C			
		$SEGSA_0$				$SEGSB_0$				$SEGSC_0$				$SEGSA_1$				$SEGSB_1$				$SEGSC_1$			

ABS	SWAP	Column address / bit / segment assign																							
0	1	X=00_H												X=01_H											
		D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
		palette A				palette B				palette C				palette A				palette B				palette C			
		$SEGSC_0$				$SEGSB_0$				$SEGSA_0$				$SEGSC_1$				$SEGSB_1$				$SEGSA_1$			

ABS	SWAP	Column address / bit / segment assign																							
1	0	X=00_H												X=01_H											
		D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette A				palette B				palette C				palette A				palette B				palette C			
		$SEGSA_0$				$SEGSB_0$				$SEGSC_0$				$SEGSA_1$				$SEGSB_1$				$SEGSC_1$			

ABS	SWAP	Column address / bit / segment assign																							
1	1	X=00_H												X=01_H											
		D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette A				palette B				palette C				palette A				palette B				palette C			
		$SEGSC_0$				$SEGSB_0$				$SEGSA_0$				$SEGSC_1$				$SEGSB_1$				$SEGSA_1$			

In the color mode, and 8-bit data bus mode

ABS	SWAP	Column address / bit / segment assign																							
0	0	X=00_H(Upper)							X=00_H(Lower)					X=01_H(Upper)							X=01_H(Lower)				
		D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
		palette A				palette B			palette C					palette A				palette B			palette C				
		$SEGSA_0$				$SEGSB_0$			$SEGSC_0$					$SEGSA_1$				$SEGSB_1$			$SEGSC_1$				

ABS	SWAP	Column address / bit / segment assign																							
0	1	X=00_H(Upper)							X=00_H(Lower)					X=01_H(Upper)							X=01_H(Lower)				
		D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
		palette A				palette B			palette C					palette A				palette B			palette C				
		$SEGSC_0$				$SEGSB_0$			$SEGSA_0$					$SEGSC_1$				$SEGSB_1$			$SEGSA_1$				

ABS	SWAP	Column address / bit / segment assign																							
1	0	X=00_H(Upper)				X=00_H(Lower)								X=01_H(Upper)				X=01_H(Lower)							
		D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette A				palette B				palette C				palette A				palette B				palette C			
		$SEGSA_0$				$SEGSB_0$				$SEGSC_0$				$SEGSA_1$				$SEGSB_1$				$SEGSC_1$			

ABS	SWAP	Column address / bit / segment assign																							
1	1	X=00_H(Upper)				X=00_H(Lower)								X=01_H(Upper)				X=01_H(Lower)							
		D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette A				palette B				palette C				palette A				palette B				palette C			
		$SEGSC_0$				$SEGSB_0$				$SEGSA_0$				$SEGSC_1$				$SEGSB_1$				$SEGSA_1$			

In the B/W mode, and 16-bit data bus mode

ABS	SWAP	Column address / bit / segment assign																											
0	0	X=00_H															X=01_H													
		D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		$SEGSA_0$					$SEGSB_0$						$SEGSC_0$					$SEGSA_1$					$SEGSB_1$						$SEGSC_1$			

ABS	SWAP	Column address / bit / segment assign																											
0	1	X=00_H															X=01_H													
		D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		$SEGSC_0$					$SEGSB_0$						$SEGSA_0$					$SEGSC_1$					$SEGSB_1$						$SEGSA_1$			

ABS	SWAP	Column address / bit / segment assign																											
1	0	X=00_H															X=01_H													
		D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
						$SEGSA_0$				$SEGSB_0$				$SEGSC_0$								$SEGSA_1$				$SEGSB_1$				$SEGSC_1$			

ABS	SWAP	Column address / bit / segment assign																											
1	1	X=00_H															X=01_H													
		D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
						$SEGSC_0$				$SEGSB_0$				$SEGSA_0$								$SEGSC_1$				$SEGSB_1$				$SEGSA_1$			

In the B/W mode, and 8-bit data bus mode

ABS	SWAP	Column address / bit / segment assign																							
0	0	X=00_H(Upper)							X=00_H(Lower)					X=01_H(Upper)							X=01_H(Lower)				
		D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
		$SEGSA_0$				$SEGSB_0$				$SEGSC_0$				$SEGSA_1$				$SEGSB_1$				$SEGSC_1$			

ABS	SWAP	Column address / bit / segment assign																							
0	1	X=00_H(Upper)							X=00_H(Lower)					X=01_H(Upper)							X=01_H(Lower)				
		D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
		$SEGSC_0$				$SEGSB_0$				$SEGSA_0$				$SEGSC_1$				$SEGSB_1$				$SEGSA_1$			

ABS	SWAP	Column address / bit / segment assign																							
1	0	X=00_H(Upper)				X=00_H(Lower)								X=01_H(Upper)				X=01_H(Lower)							
		D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		$SEGSA_0$				$SEGSB_0$				$SEGSC_0$				$SEGSA_1$				$SEGSB_1$				$SEGSC_1$			

ABS	SWAP	Column address / bit / segment assign																							
1	1	X=00_H(Upper)				X=00_H(Lower)								X=01_H(Upper)				X=01_H(Lower)							
		D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		$SEGSC_0$				$SEGSB_0$				$SEGSA_0$				$SEGSC_1$				$SEGSB_1$				$SEGSA_1$			

(11) Gradation palette

In the gradation mode, either variable or fixed gradation mode is selected by programming the “PWM” register of the “Gradation control” instruction.

PWM=0: Variable gradation mode
(Select 16 gradation levels out of 32-gradation level of the gradation palette)

PWM=1: Fixed gradation mode
(Fixed 8-gradation levels)

In these modes, each of the gradation palettes Aj, Bj and Cj can select 16-gradation level out of 32-gradation level by setting 5-bit data to the “PA” registers in the “Gradation palette j” instructions (j=0 to Fh).

For instance, the gradation palettes Aj correspond to the SEGAi, the Bj to SEGBi and the Cj to SEGCi (j=0 to 15, i=0 to 127).

Correspondence between display data and gradation palettes

Table 10 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

(MSB) Display data (LSB)				Gradation palette	Default palette value
0	0	0	0	Palette 0	0 0 0 0 0
0	0	0	1	Palette 1	0 0 0 1 1
0	0	1	0	Palette 2	0 0 1 0 1
0	0	1	1	Palette 3	0 0 1 1 1
0	1	0	0	Palette 4	0 1 0 0 1
0	1	0	1	Palette 5	0 1 0 1 1
0	1	1	0	Palette 6	0 1 1 0 1
0	1	1	1	Palette 7	0 1 1 1 1
1	0	0	0	Palette 8	1 0 0 0 1
1	0	0	1	Palette 9	1 0 0 1 1
1	0	1	0	Palette10	1 0 1 0 1
1	0	1	1	Palette11	1 0 1 1 1
1	1	0	0	Palette12	1 1 0 0 1
1	1	0	1	Palette13	1 1 0 1 1
1	1	1	0	Palette14	1 1 1 0 1
1	1	1	1	Palette15	1 1 1 1 1

Gradation palette table (Variable gradation mode, PWM="0", MON="0")

Table 11 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

Palette value	Gradation level	Gradation palette	Palette value	Gradation level	Gradation palette
0 0 0 0 0	0	Palette 0(default)	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette 0(default)8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette 1(default)	1 0 0 1 1	19/31	Palette 9(default)
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette 2(default)	1 0 1 0 1	21/31	Palette 10(default)
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette 3(default)	1 0 1 1 1	23/31	Palette 11(default)
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette 4(default)	1 1 0 0 1	25/31	Palette 12(default)
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette 5(default)	1 1 0 1 1	27/31	Palette 13(default)
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette 6(default)	1 1 1 0 1	29/31	Palette 14(default)
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette 7(default)	1 1 1 1 1	31/31	Palette 15(default)

Gradation palette table (Fixed gradation mode, PWM="1", MON="0")

Table 12 8-gradation segment drivers

(MSB) Display data (LSB)				Gradation level
0	0	0	*	0/7
0	0	1	*	1/7
0	1	0	*	2/7
0	1	1	*	3/7
1	0	0	*	4/7
1	0	1	*	5/7
1	1	0	*	6/7
1	1	1	*	7/7

(MSB) Display data (LSB)				Gradation level
0	0	*	*	0/7
0	0	*	*	
0	1	*	*	3/7
0	1	*	*	
1	0	*	*	5/7
1	0	*	*	
1	1	*	*	7/7
1	1	*	*	

Correspondence between display data and gradation level (B&W mode, MON="1")

Table 13

(MSB) Display data (LSB)				Gradation level
0	*	*	*	0
1	*	*	*	1

*:Don't care

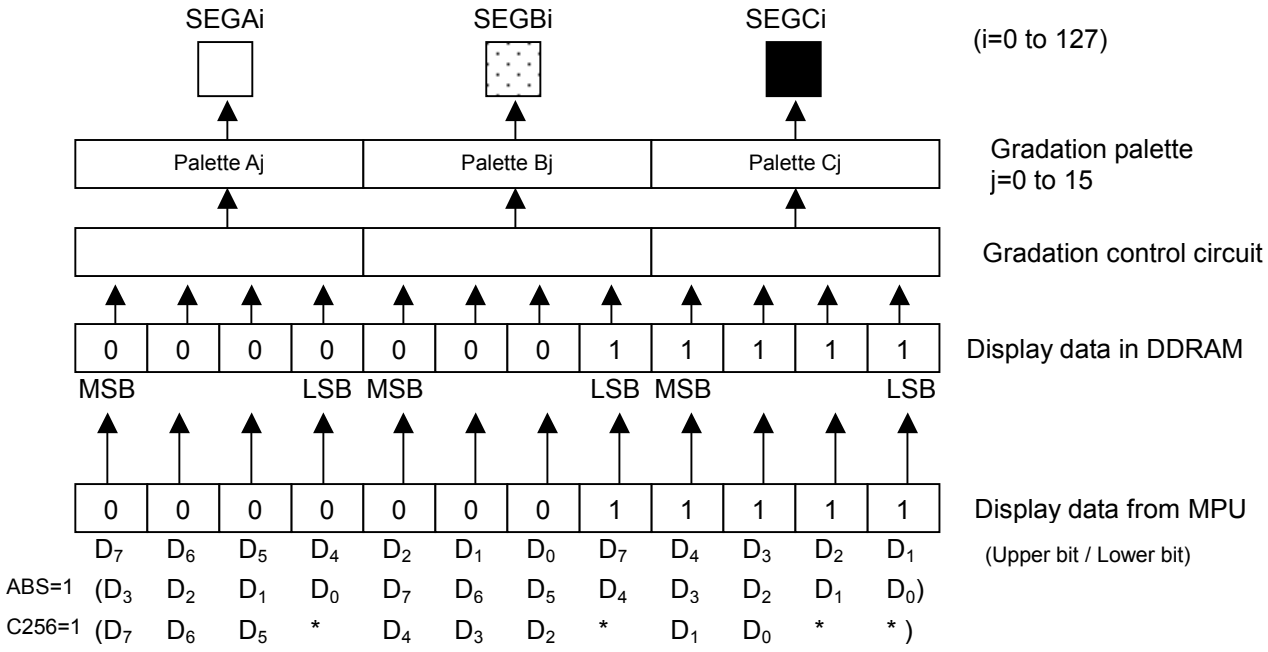
(12) Gradation control and display data

(12-1) Gradation mode

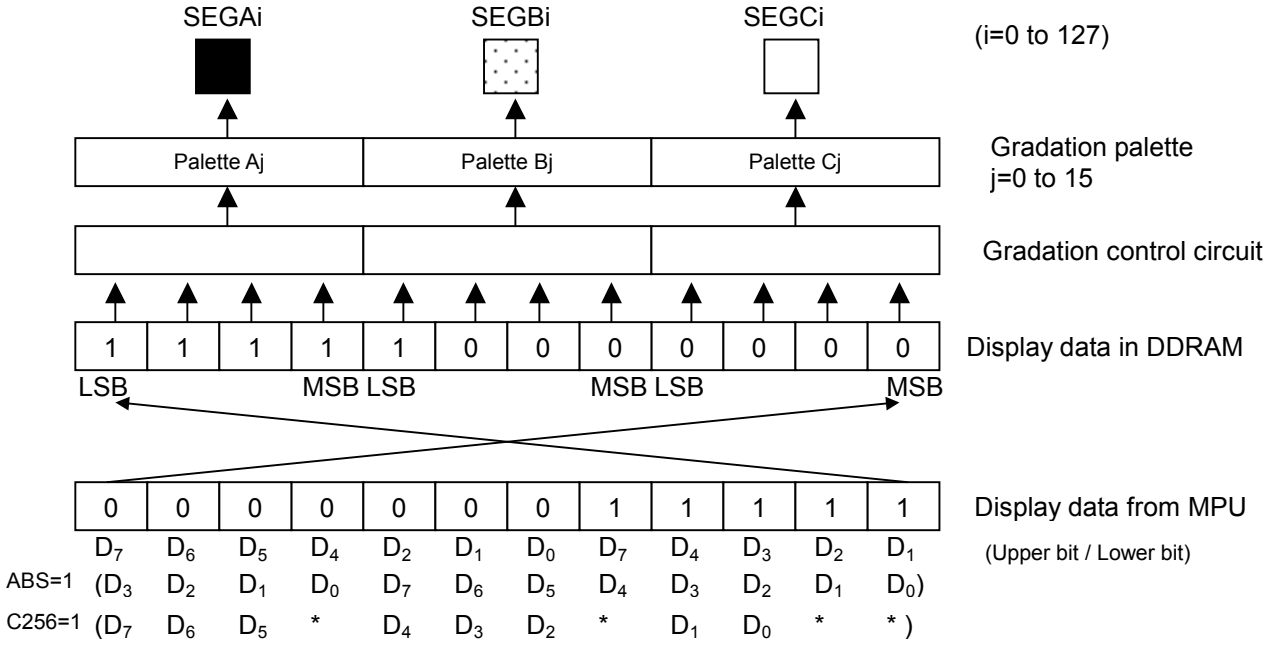
In the graduation mode, each pixel for RGB corresponds to successive 3 segment drivers, and each segment driver provides 16-gradation PWM output by controlling 4 bit display data of the DDRAM. Accordingly, the LSI can drive up to 128x128 pixels in 4096-color (16-gradation x 16-gradation x 16-gradation = 4-bit x 4-bit x 4-bit).

In addition, the LSI can transfer the display data for the RGB by 16-bit at once or 8-bit two-times. The data assignment between gradation palettes and segment drivers varies in accordance with setting for the “SWAP” registers of the "Display control (2)" instruction.

- SWAP = 0

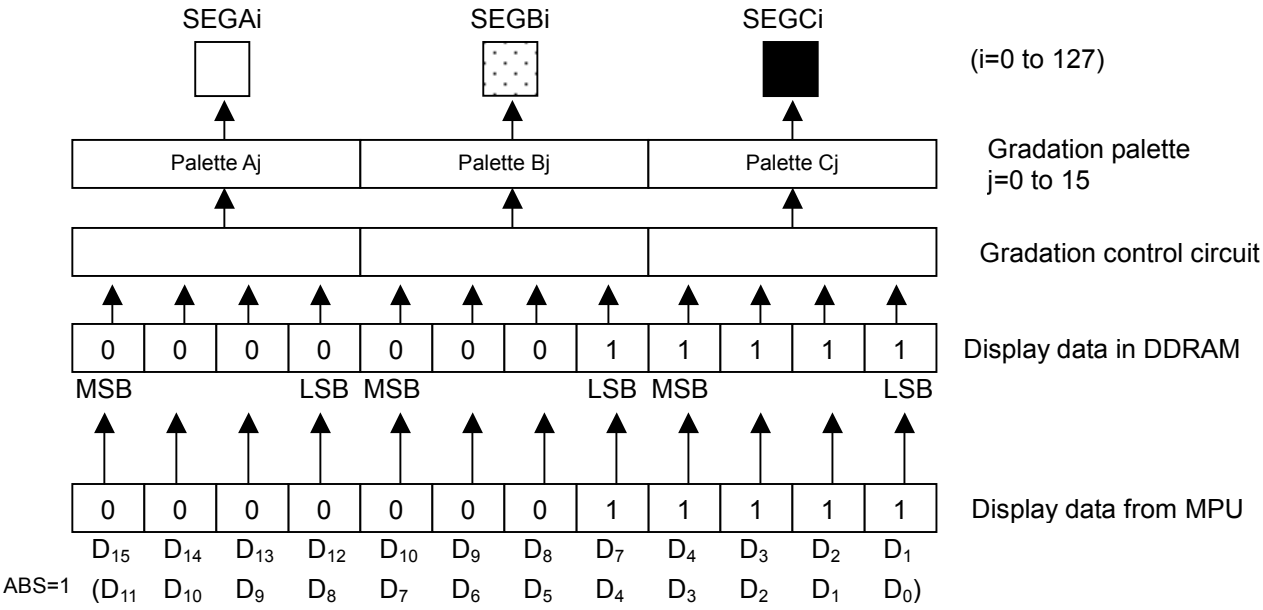


- SWAP = 1

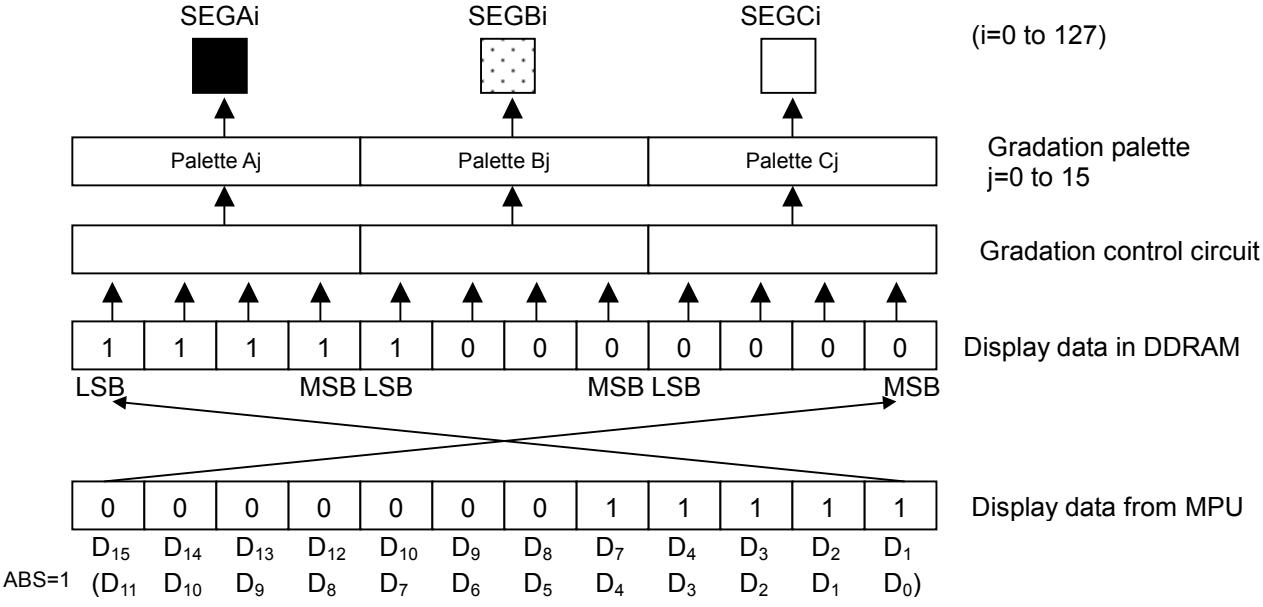


In the 16-bit data bus mode, the data assignments between the gradation palettes and the segment drivers vary in accordance with setting for the “SWAP” bit of the "Display control (2)" instruction as well as the assignment in the 8-bit data bus mode.

- SWAP = 0



- SWAP = 1

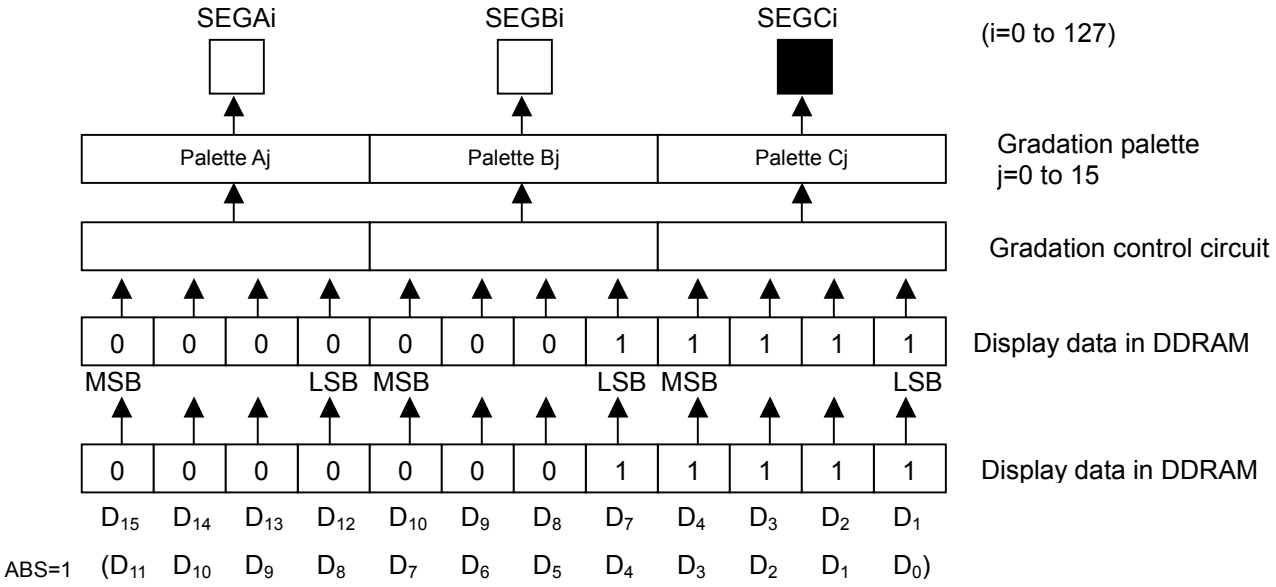


(12-2) B&W mode (MON="1")

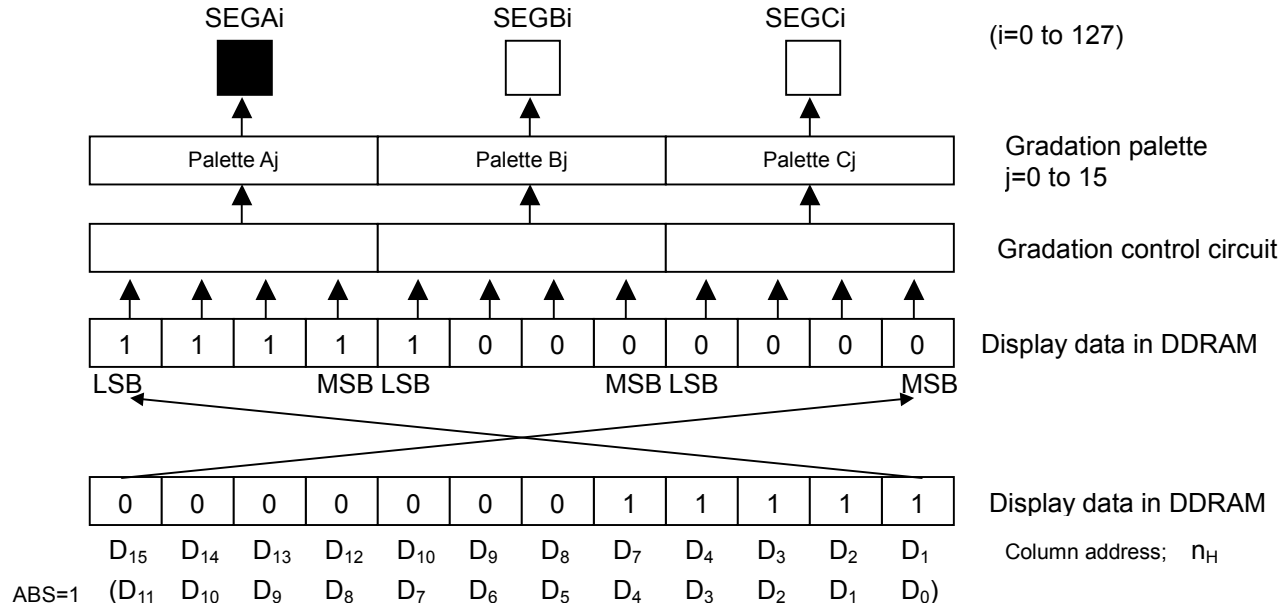
In the B&W mode, 3 bits of the MSB data are used in both of the 16-bit and 8-bit data bus modes.

In the 16-bit data bus mode (Similarly 8-bit data bus access)

- SWAP = 0



- SWAP = 1



The correlation of display data with gradation control is also applied to Icon segment.

(13) Display timing generator

The display-timing generator creates the timing pulses such as the CL, the FLM, the FR and the CLK by dividing the oscillation frequency oscillate an external or internal resister mode. The each of timing pulses is outputted through the each output terminals by “SON”=1.

(14) LCD line clock (CL)

The LCD line clock (CL) is used as a count-up signal for the line counter and a latch signal for the data latch circuit. At the rising edge of the CL signal, the line counter is counted-up and the 384-bit display data, corresponding to this line address, is latched into the data latch circuit. And at the falling edge of the CL signal, this latched data output on the segment drivers. Read out timing of the display data, from DDRAM to the latch circuits is completely independent of the access timing to the MPU. For this reason, the MPU can access to the LSI regardless of an internal operation.

(15) LCD alternate signal (FR) and LCD synchronous signal (FLM)

The FR and FLM signals are created from the CL signal. The FR signal is used to alternate the crystal polarization on a LCD panel. It is programmed that the FR signal is toggle on every frame in the default setting or once every N lines in the N-line inversion mode. The FLM signal is used to indicate a start line of a new display frame. It presets an initial display line address of the line counter when the FLM signal becomes ”1”.

(16) Data latch circuit

The data latch circuit is used temporarily store the display data that will output to the segment drivers. The display data in this circuit is updated in synchronization of the CL signal.

The “All pixels ON/OFF”, “Display ON/OFF” and “Reverse display ON/OFF” instructions change the display data in this circuit but do not change the display data of the DDRAM.

(17) Common and segment drivers

The LSI includes 384+6-segment drivers and 128-common drivers. The common drivers generate the LCD driving waveforms composed of the V_{LCD}, V_1, V_4 and V_{SS} in accordance with the FR signal and scanning data. The segment drivers generate waveforms composed of the V_{LCD}, V_2, V_3 and V_{SS} in accordance with the FR signal and display data.

LCD Driving waveforms (In the B&W mode, Reverse display OFF, 1/129 duty)

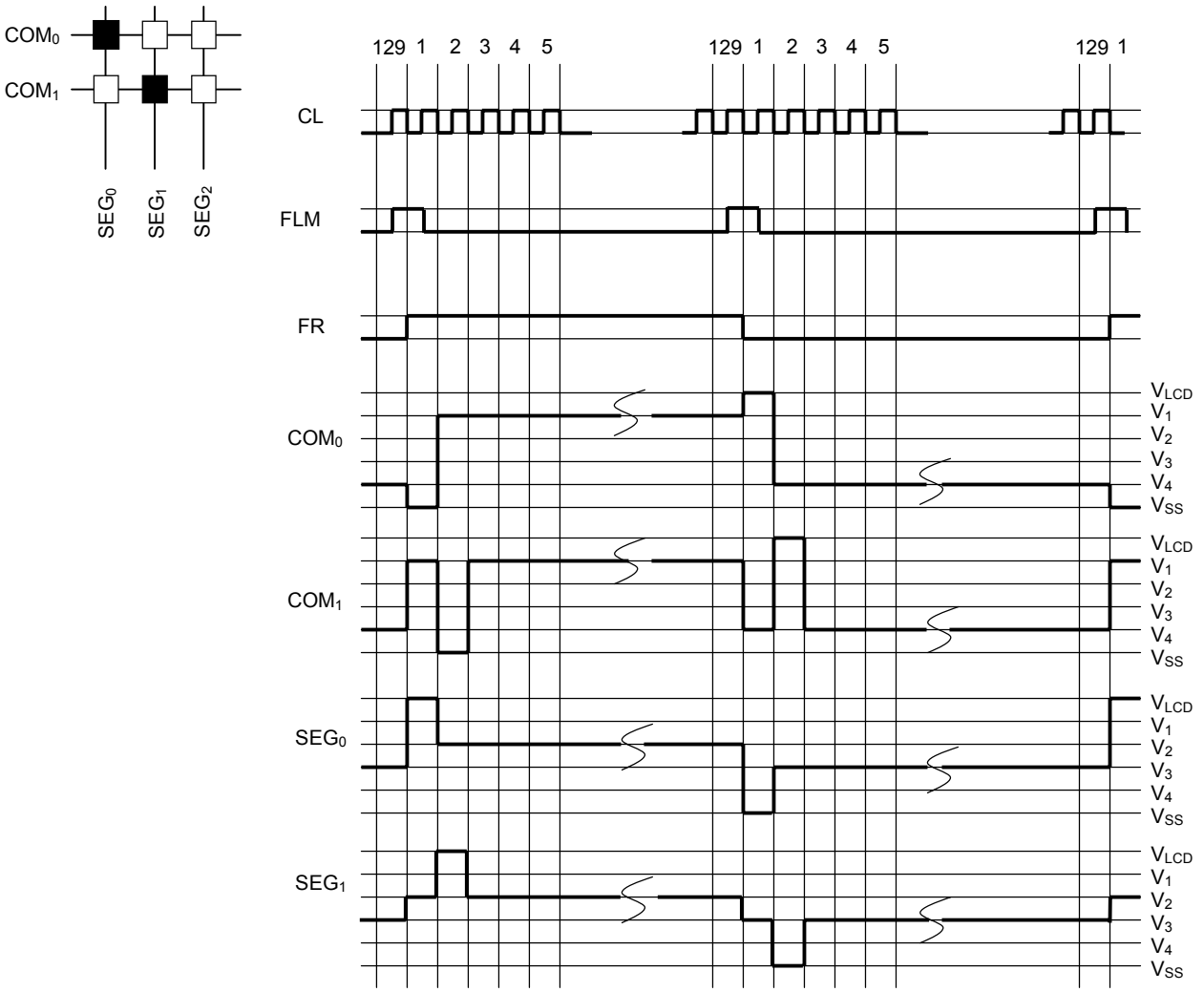


Fig 8

(18) Icon Segment Driver Circuit

Each 3 outputs (SEGSA0 to SEGSA1, SEGSB0 to SEGSB1, SEGSC0 to SEGSC1) placed at both edges of normal segment output terminals line are Segment outputs for Icon. Although normal Segment output generates the LCD driving voltage corresponding with the data in Display Data RAM, Icon segment driver provides the register instead of the display data RAM. The data corresponding to SEGSA0, SEGSB0 and SEGSC0 are in 12-bit register and output the same driving voltage on the row direction. (The data corresponding to SEGSA1, SEGSB1 and SEGSC1 are same as SEGSA0, SEGSB0 and SEGSC0.)

The outputs of SEGSA0 to SEGSA1 assign the same gradation pallet as SEGA0 to SEGA127, SEGSB0 to SEGSB1 are SEGB0 to SEGB127 and SEGSC0 to SEGSC1 are SEGC0 to SEGC127.

Icon Segment Driver Circuit operates for the outline frame display or background. These displays are changed in accordance with attribute of ALLON or REV command, but no change by LREV command.

The capacity of register corresponding with Icon segment driver (SEGSA0 to SEGSA1, SEGSB0 to SEGSB1, SEGSC0 to SEGSC1) is 24 bits. The access to from this register performed at DMY="1"..

Table14

RS	DMY	68type	80 type		Function
		R/W	$\overline{RD}$	$\overline{WR}$	
L	0	H	L	H	Display data read
L	0	L	H	L	Display data write
L	1	H	L	H	Icon segment register read
L	1	L	H	L	Icon segment register read

Read out function from the Icon segment register is restricted as same as the display data read out function from Display Data RAM. After address set, the addressed data does not come out by the first read instruction immediately but comes out by the second read instruction. Therefore, one dummy read out function is required for data read from Icon segment register after the address set or the data write operation.

When the Icon segment registers are accessed in DMY="1", the valid addressing is just a column address. Because of 24 bits Icon register, the valid addresses are "00h" and "01h" in 8-bit or 16-bit mode.

When the Icon segment registers are accessed in DMY="1", the data write operation into Icon register is enabled with the increment / decrement operation.

The column address increment operates as shown below. But the auto carry up operation like as the maximum address to "00h" does not operate of the display data RAM access.

00h -> Max.

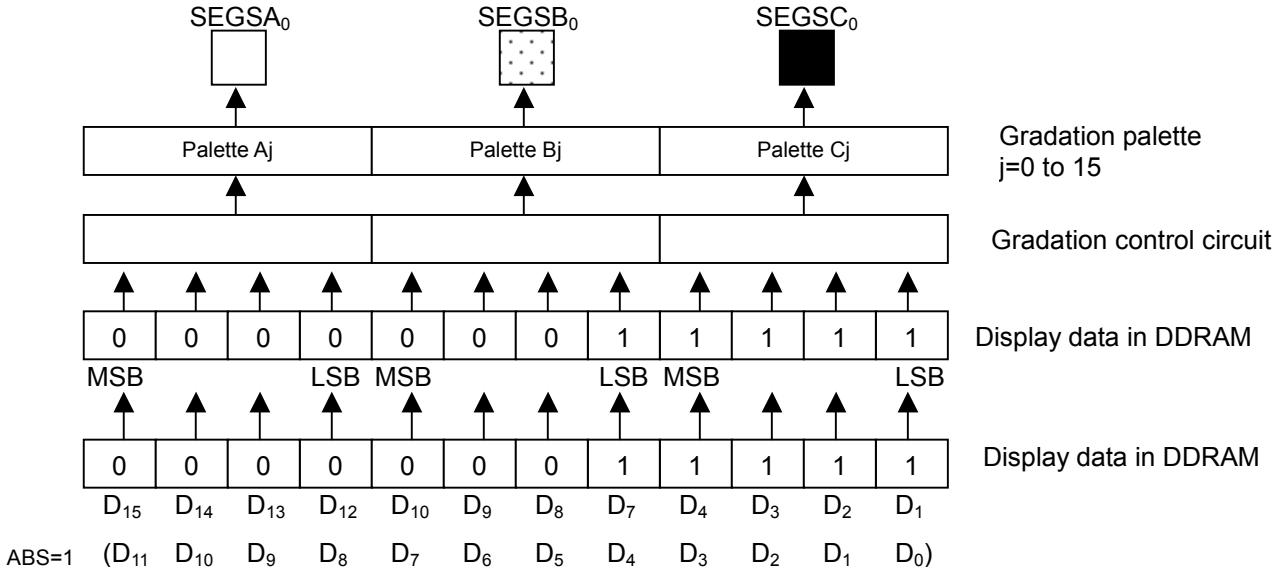
- 8-bit or 16-bit data bus mode (DMY="1")
  Column address 00_H: $SEGSA_0$, $SEGSB_0$, $SEGSC_0$
  01_H: $SEGSA_1$, $SEGSB_1$, $SEGSC_1$

Note) Refer the "Icon segment register address bit assignment" in (10) The relationship among the DDRAM column address, display data and segment drivers. Both of Icon segment register and Display data RAM operate a same address counter so that the address is set again in the status transition of DMY = "0" to "1" or "1" to "0".

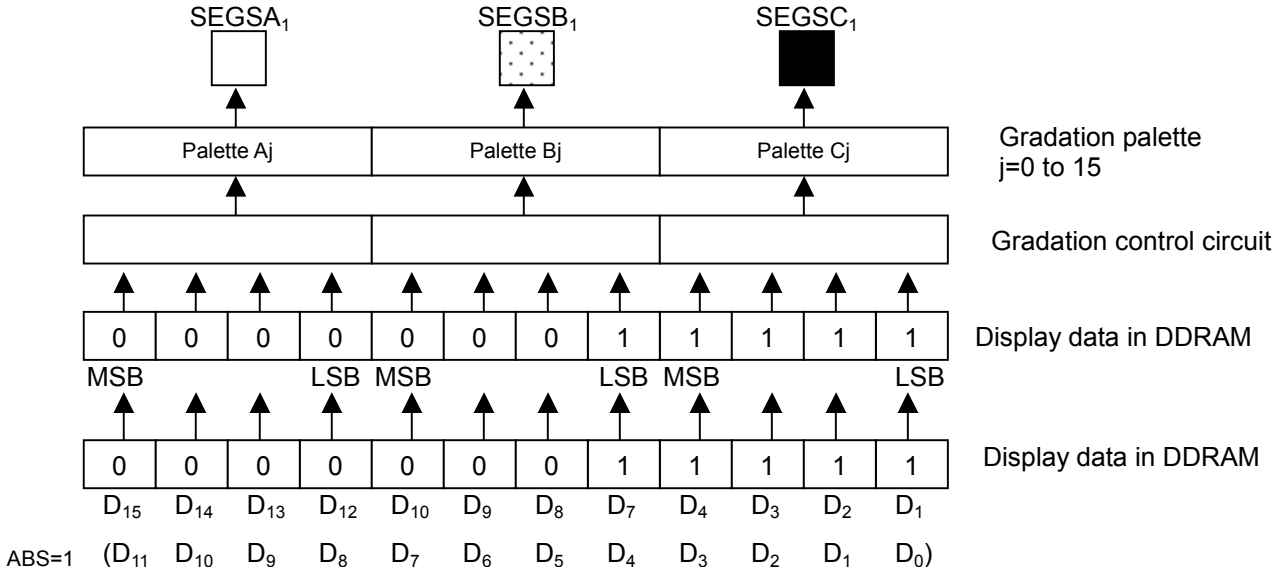
The access to Icon register must be operated in the condition of HV=0.

Examples for the dummy segment registers (DMY="1")
(In the 16-bit data bus mode, gradation mode, (REF,SWAP)=(0,0))

Column address: 00_H



Column address: 01_H



(19) Oscillator

The oscillator generates internal clocks for the display timing and the voltage booster. Since the LSI has internal capacitor (C) and resistor (R) for the oscillation, external capacitor and resistor are not usually required. However, in case that an external resistor is used, the resister is connected between the OSC_1 and OSC_2 terminals. The external resistor becomes enabled by setting "1" to the "CKS" register of "Data bus length" instruction. When the internal oscillator is not used, the external clocks with 50% duty cycle ratio must be input to the OSC_1 terminal.

In addition, the feed back resister for the oscillation is varied by programming the "Rf" register of the "Frequency control" instruction, so that it is possible to optimize the frame frequency for a LCD panel. Setting examples of the MON (B&W /Gradation) and the PWM (Variable gradation /Fixed gradation) are described, as follows.

Internal oscillation mode (CKS=0)

Symbol	MON	PWM	Display mode
f_1	0	0	Variable gradation mode
f_2	0	1	Fixed gradation mode
f_3	1	*	B&W mode

*: Don't care

External resistor oscillation mode(CKS=1)

The internal clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "MON" and "PWM" registers must be set as well.

External clock input mode(CKS=1)

The external clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "MON" and "PWM" registers must be set as well.

(20) Power supply circuits

The internal power supply circuits are composed of the voltage booster, the electrical variable resister (EVR), the voltage regulator, reference voltage generator and the voltage followers.

The condition of the power supply circuits is arranged by programming the "DCON" and "AMPON" registers on the "Power control" instruction. For this arrangement, some parts of the internal power supply circuits are activated in using an external power supply, as shown in the following table.

Table 15

DCON	AMPON	Voltage booster	Voltage followers Voltage regulator EVR	External voltage	Note
0	0	Disable	Disable	V_{OUT}, V_{LCD}, V_1, V_2, V_3, V_4	1, 3
0	1	Disable	Enable	V_{OUT}	2, 3
1	1	Enable	Enable	–	–

Note1) The internal power circuits are not used. The external V_{OUT} is required and the C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, V_{REF}, V_{REG} and V_{EE} terminals must be open.

Note2) The internal power circuits except the voltage booster are used. The external V_{OUT} is required and the C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5- and V_{EE} terminals must be open. The reference voltage is required to V_{REF} terminal.

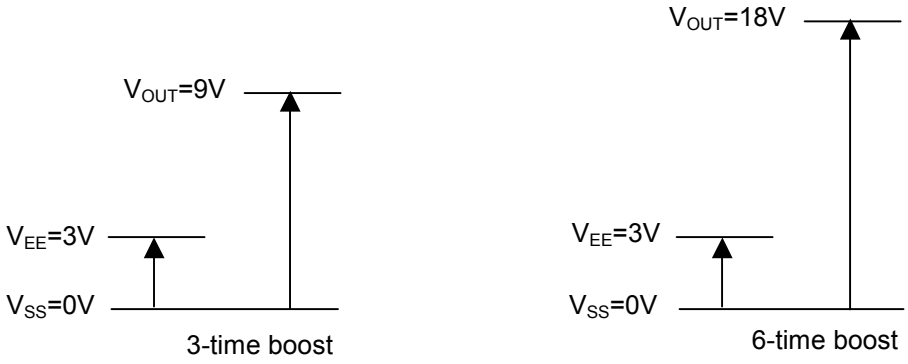
Note3) The relation among the voltages should be maintained as follows.

$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$

(21) Voltage booster

The voltage booster generates maximum 6x voltage of the V_{EE} level. It is programmed so that the boost level is selected out of 1x, 2x, 3x, 4x, 5x and 6x by the “Boost level select” instruction. The boosted voltage V_{OUT} must not exceed beyond the value of 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

Boosted voltages



Capacitor connections for the voltage Booster

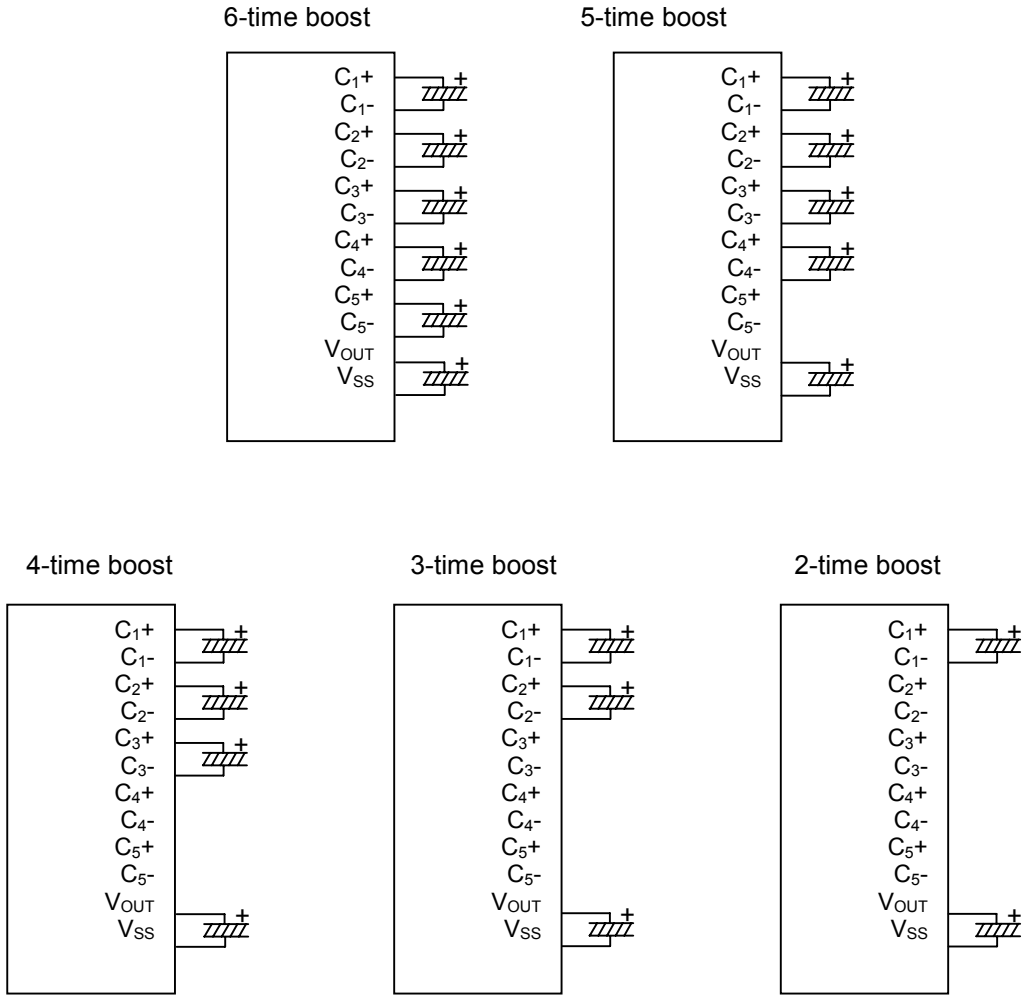


Fig 9

(22) Reference voltage generator

The reference voltage generator is used to produce the reference voltage (V_{BA}), which is output from the V_{BA} terminal and should be input to the V_{REF} terminal.

$V_{BA} = V_{EE} \times 0.9$

(23) Voltage regulator

The voltage regulator, composed of the gain control circuit and an operational amplifier, and is used to gain the reference voltage (V_{REF}) and to create the regulated voltage (V_{REG}). The V_{REG} is used as an input voltage to the EVR circuits, which is programmed by the "VU" register of the "Boost level" instruction.

$V_{REG} = V_{REF} \times N$ (N: register value for the boost level)

(24) Electrical variable resister (EVR)

The EVR is variable within 128-step, and is used to fine-tune the LCD driving voltage (V_{LCD}) by programming the "DV" register in the "EVR control" instruction, so that it is possible to optimize the contrast level for a LCD panels.

$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127$ (M: register value for the EVR)

(25) LCD driving voltage generation circuit

LCD driving voltage generation circuit generates the V_{LCD} voltage levels as V_{LCD}, V_1, V_2, V_3 and V_4 with internal E.V.R and the Bleeder resistors. The bias ratio of the LCD driving voltage is selected out of 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11 and 1/12.

In using the internal power supply, the capacitors CA_2 must be connected to the V_{LCD}, V_1, V_2, V_3 and V_4 terminals, and the CA_2 value must be determined by the evaluation with actual LCD modules.

In using the external power supply, the external LCD driving voltages such as the V_{LCD}, V_1, V_2, V_3 and V_4 are supplied and the internal power supply circuits must be set to "OFF" by DCON = AMPON = "0". In this mode, voltage booster terminals such as C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, V_{EE}, V_{REF} and V_{REG} must be opened.

In case that the voltage booster is not used but only some parts of internal power supply circuits (Voltage followers, Voltage regulator and EVR) are used, the C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+ and C_5- terminals must be opened. And, the external power supply is input to the V_{OUT} terminal, and the reference voltage to the V_{REF} terminal. The capacitor CA_3 must connect to the V_{REG} terminal for voltage stabilization.

< Bias adjustment function >

NJU6824 prepares bias adjustment terminals V_1A_1, V_1A_2, V_4A_1 and V_4A_2 for fine adjustment of V1 and V4 out of voltages.

The status combination of V_1A_1 terminal and V_1A_2 can adjust V1 voltage in below table and V_4A_1 and V_4A_2 can adjust V4 voltage. These adjustment performs by the connection change between the Bleeder resistors and the output buffer operational amplifier as voltage follower circuit.

V_1A_1 terminal	V_1A_2 terminal	Fluctuation voltage [mV] *1
0	0	0
0	1	+5
1	0	-5
1	1	+10

V_4A_1 terminal	V_4A_2 terminal	Fluctuation voltage [mV] *1
0	0	0
0	1	+5
1	0	-5
1	1	-10

Note 1) The fluctuation voltage is a adjusted voltage against the default voltage at (V_1A_1, V_1A_2 = "0, 0" and V_4A_1, V_4A_2 = "0, 0"). The "+" mark means a direction of voltage fluctuation to V_{LCD} and the "-" is to V_{SS}.
Note 2) The fluctuation voltage is an ideal value.
Note 3) The fluctuation voltage is at V_{LCD}=13.5V.
Note 4) "0" of V_1A_1, V_1A_2, V_4A_1 and V_4A_2 means V_{SS} and "1" means V_{DD}.

Connections of the capacitors for voltage boost

Using all of the internal power supply circuits
(6-time boost)

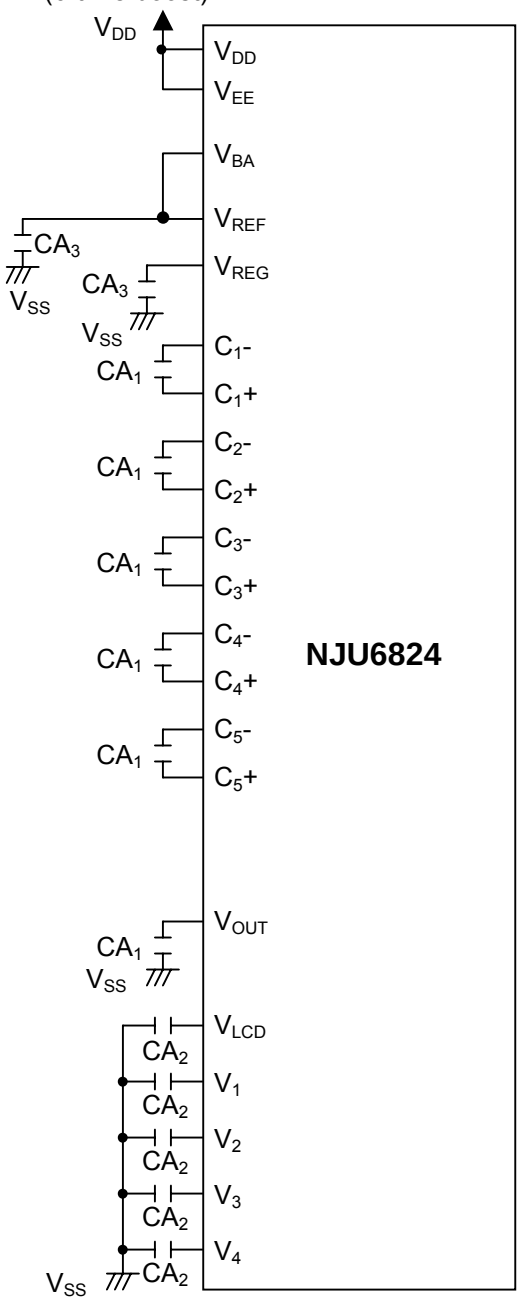


Fig 10

Using only external power supply circuits

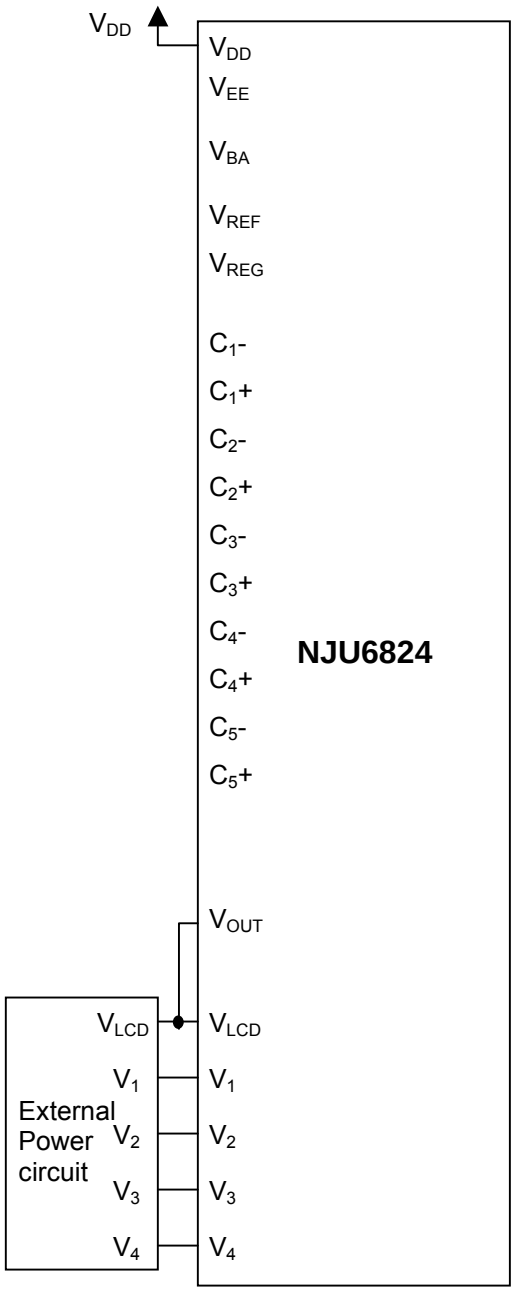


Fig11

Reference values

CA_1	1.0 to 4.7uF
CA_2	1.0 to 2.2uF
CA_3	0.1uF

Note) B grade capacitors are required.

Using internal power supply circuits
Without the reference voltage generator(1)
(6-time boost)

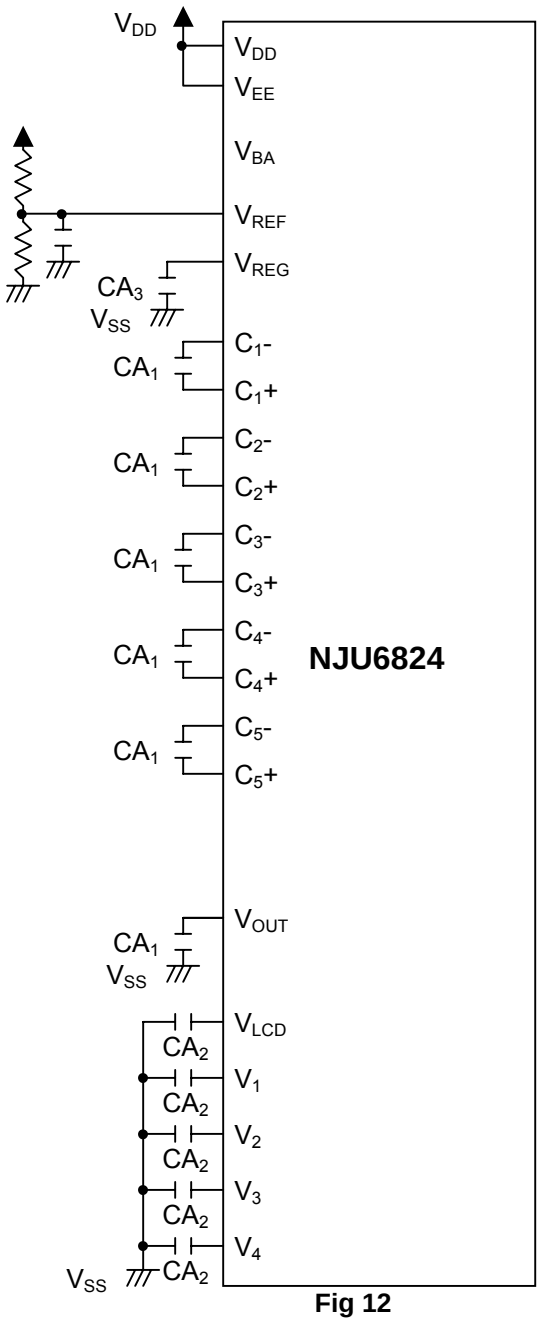


Fig 12

Using internal power supply circuit
Without the reference voltage generator(2)
(6-time boost)

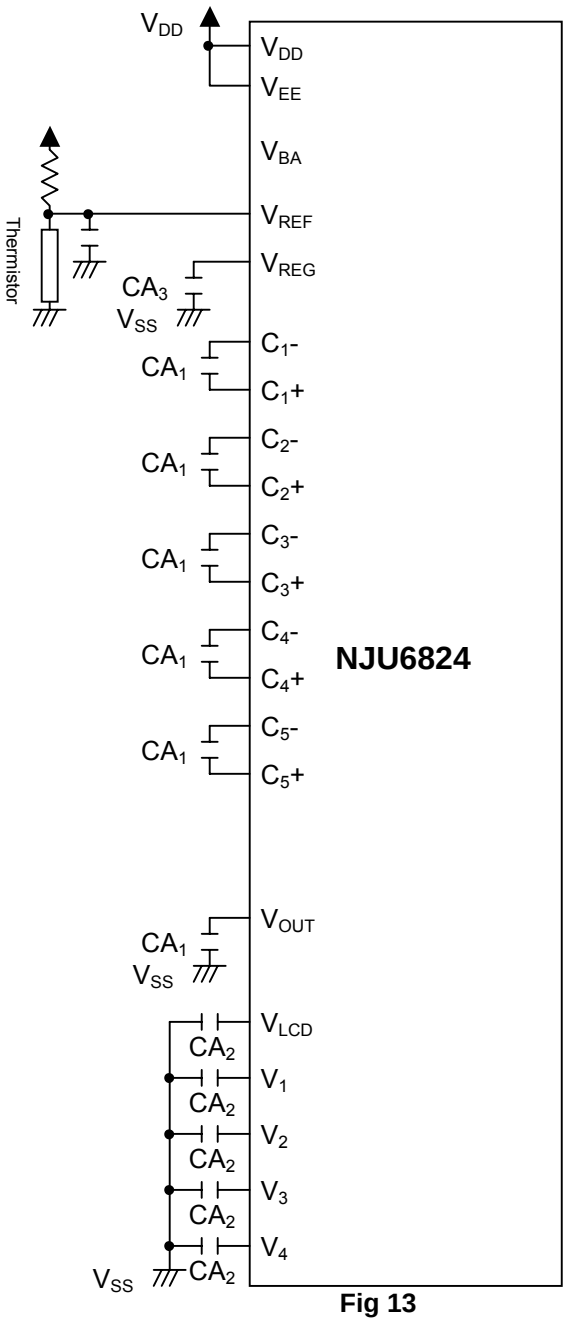


Fig 13

Reference value

CA_1	1.0 to 4.7μF
CA_2	1.0 to 2.2μF
CA_3	0.1μF

Note) B grade capacitors are required.

Using internal power supply circuits
Without the voltage booster

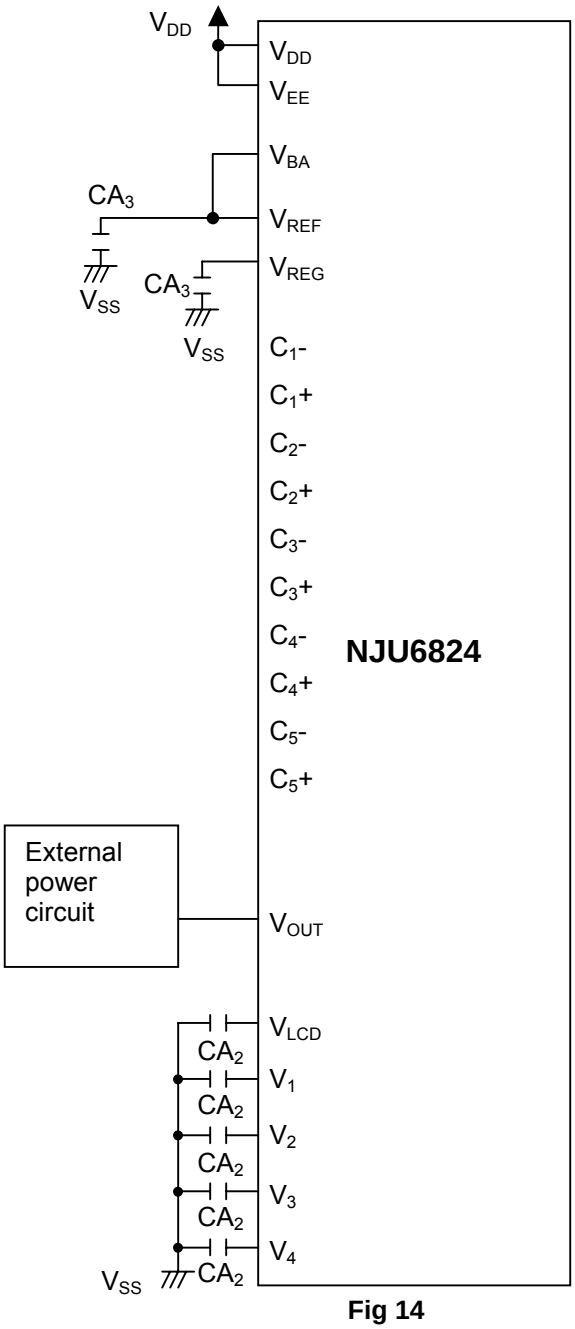


Fig 14

Reference value

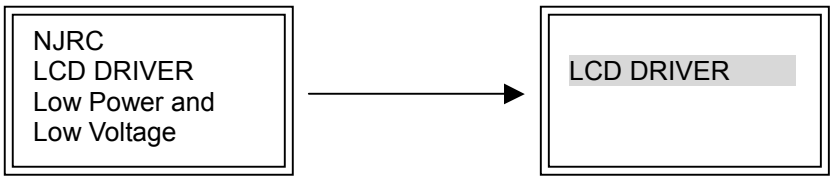
CA_1	1.0 to 4.7µF
CA_2	1.0 to 2.2µF
CA_3	0.1µF

Note) B grade capacitors are required.

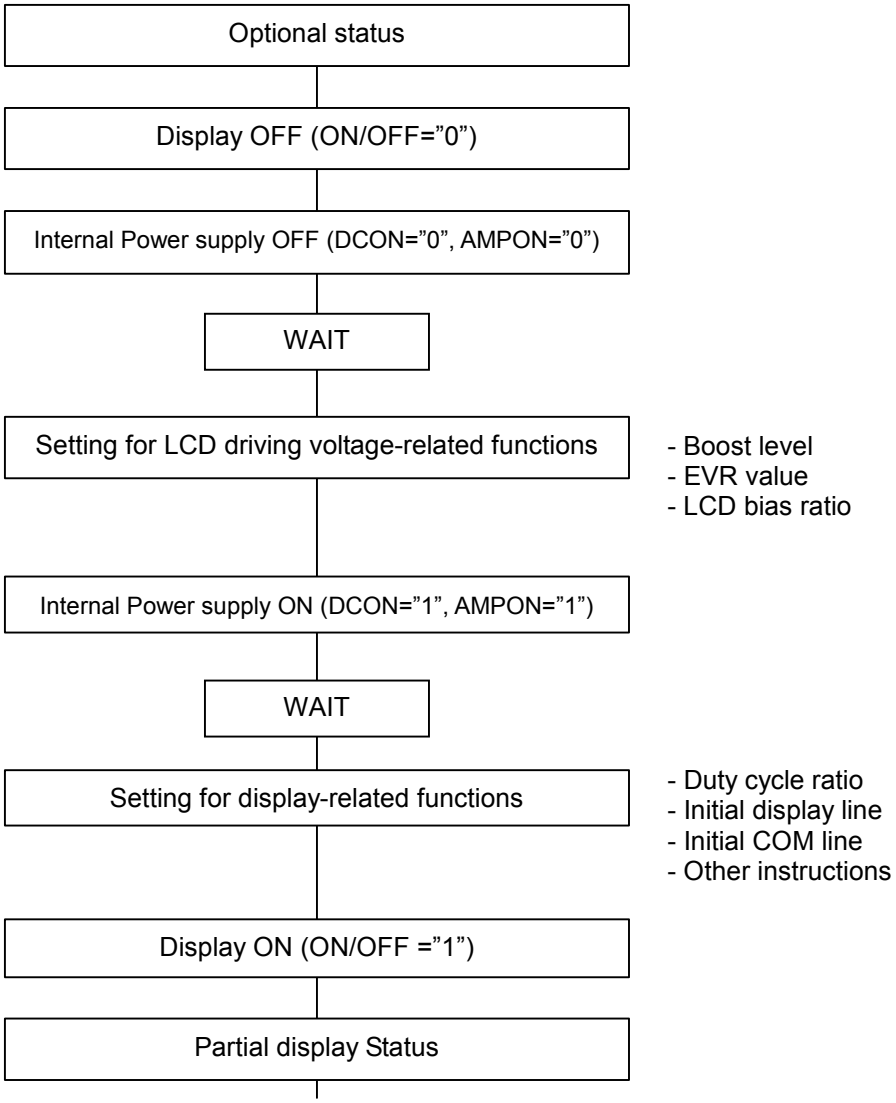
(26) Partial display function

The partial display function is used to partially specify some parts of display area on LCD panels. By using this function, LCD modules can work in lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. It is usually used to display a time and calendar, and is also used to optimize the LSI condition in accordance with the display size. It can be programmed to select the duty cycle ratio (1/17, 1/25, 1/33, 1/41, 1/49, 1/57, 1/65, 1/73, 1/81, 1/89, 1/97, 1/105, 1/113, 1/121, 1/129, in DSE=0), the LCD bias ratio, the boost level and the EVR value by the instructions.

Partial display image



Partial display sequence



(27) Discharge circuit

Discharge circuit is used to discharge the electric charge of the capacitors on the V_1 to V_4 and V_{LCD} terminals. This circuit is activated by setting “0” to the “DIS” register of the “Discharge” instruction or by setting “RESb” terminal to ”0” level. The “Discharge ON/OFF” instruction is usually required just after the internal power supply is turned off by setting “0” into the “DCON” and “AMPON” registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

(28) Reset circuit

The reset circuit initializes the LSI into the following default status. It is activated by setting the RESb terminal to “0”. The RESb terminal is usually required to connect to MPU reset terminal in order that the LSI can be initialized at the same timing of the MPU.

- Default status

1. DDRAM display data :Undefined
2. column address :$(00)_H$
3. row address :$(00)_H$
4. Initial display line :$(0)_H$ (1st line)
5. Display ON/OFF :OFF
6. Reverse display ON/OFF :OFF (normal)
7. Duty cycle ratio :1/129 duty(DSE=0)
8. N-line Inversion ON/OFF :OFF
9. COM scan direction :$COM_0 \rightarrow COM_{127}$
10. Address direction of RAM :(HV, XD, YD) = (0, 0, 0)
11. Read modify write :OFF (AIM=0)
12. SWAP mode :OFF (normal)
13. EVR value :(0, 0, 0, 0, 0, 0, 0)
14. Internal power supply :OFF
15. Display mode :Gradation display mode
16. LCD bias ratio :1/9 bias
17. Gradation Palette 0 :(0, 0, 0, 0, 0)
18. Gradation Palette 1 :(0, 0, 0, 1, 1)
19. Gradation Palette 2 :(0, 0, 1, 0, 1)
20. Gradation Palette 3 :(0, 0, 1, 1, 1)
21. Gradation Palette 4 :(0, 1, 0, 0, 1)
22. Gradation Palette 5 :(0, 1, 0, 1, 1)
23. Gradation Palette 6 :(0, 1, 1, 0, 1)
24. Gradation Palette 7 :(0, 1, 1, 1, 1)
25. Gradation Palette 8 :(1, 0, 0, 0, 1)
26. Gradation Palette 9 :(1, 0, 0, 1, 1)
27. Gradation Palette 10 :(1, 0, 1, 0, 1)
28. Gradation Palette 11 :(1, 0, 1, 1, 1)
29. Gradation Palette 12 :(1, 1, 0, 0, 1)
30. Gradation Palette 13 :(1, 1, 0, 1, 1)
31. Gradation Palette 14 :(1, 1, 1, 0, 1)
32. Gradation Palette 15 :(1, 1, 1, 1, 1)
33. Gradation mode control :Variable gradation mode
34. Data bus length :8-bit data bus length
35. Discharge circuit :(DIS, DIS2)=(0,0)

(29) Power supply ON/OFF sequences

The following paragraphs describe power supply ON/OFF sequences, which are to protect the LSI from over current.

(29-1) Using an external power supply

- Power supply ON sequence

  Logic voltage (V_{DD}) must be always input first, and next the LCD driving voltages (V_1 to V_4 and V_{LCD}) are turned on. In using the external V_{OUT}, the V_{DD} must be input first, next the reset operation must be performed, and finally the V_{OUT} can be input.

- Power supply OFF sequence

  Either the reset operation, cutting off the V_1 to V_4 and V_{LCD} from the LSI by the RESb terminal or the "Power control" instruction must be performed first, and next the V_{DD} is turned off. It is recommended that a series-resister between 50Ω and 100Ω is added on the V_{LCD} line (or V_{OUT} line in using only the external V_{OUT} voltage) in order to protect the LSI from the over current.

(29-2) Using the internal power supply circuits

- Power supply ON sequence

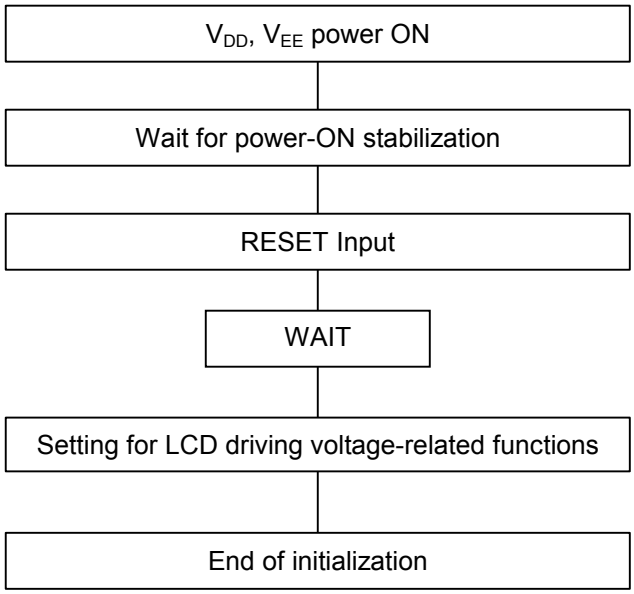
  The V_{DD} must be input first, next the reset operation must be performed, and finally the V_1 to V_4 and V_{LCD} can be turned on by setting "1" to the "DCON" and "AMPON" registers of the "Power control" instruction.

- Power supply OFF sequence

  Either the reset operation by the RESb terminal or the "Power control" instruction must be performed first, and next the input voltage for the voltage booster (V_{EE}) and the V_{DD} can be turned off. If the V_{EE} is supplied from different power sources for V_{DD}, the V_{EE} is turned off first, and next the V_{DD} is turned off.

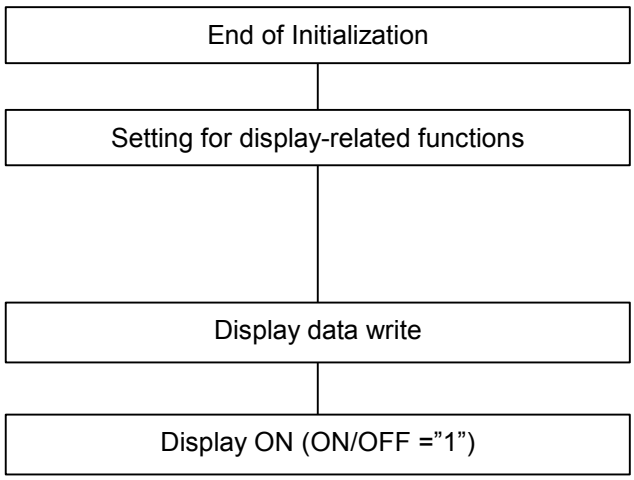
(30) Referential instruction sequences

(30-1) Initialization in using the internal power supply circuits



- EVR value
- LCD bias ratio
- Power control (DCON="1", AMPON="1")

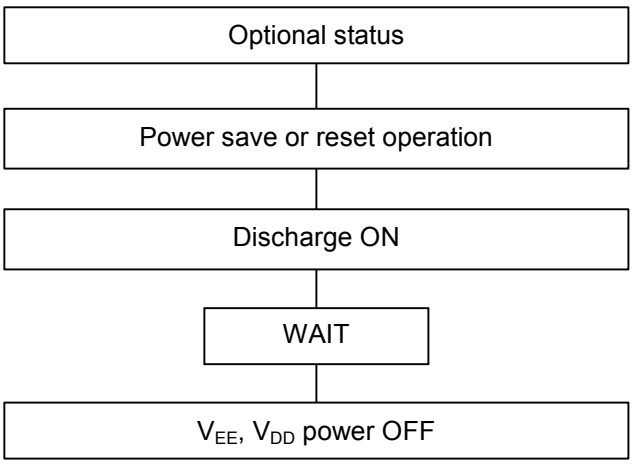
(30-2) Display data writing



- Initial display line
- Address direction of RAM (HV, XD, YD)
- Column address / -Row address (Start)
- Column address / -Row address (End)

*: Before display data write / read operation, the address directions should be set first , then Column address set / Row address set of start point and end are set in order. (Display data write / read for whole display area or a portion requires the same procedure as above.)
To avoid incorrect data writing into registers by noise and so forth, the written data from registers should be checked after write operation.

(30-3) Power OFF



- All COM/SEG output V_{SS} level.

(31) Instruction table

Instruction Table (1)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display data write	0	0	1	0	0/1	0/1	0/1	Write Data								Write display data to DDRAM
Display data read	0	0	0	1	0/1	0/1	0/1	Read Data								Read display data from DDRAM
column address (Lower) [0_H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	DDRAM column address
column address (Upper) [1_H]	0	1	1	0	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	DDRAM column address
row address (Lower) [2_H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	DDRAM row address
row address (Upper) [3_H]	0	1	1	0	0	0	0	0	0	1	1	*	AY6	AY5	AY4	DDRAM row address
Initial display line (Lower) [4_H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Row address for an initial COM line (Scan start line)
Initial display line (Upper) [5_H]	0	1	1	0	0	0	0	0	1	0	1	*	LA6	LA5	LA4	Row address for an initial COM line (Scan start line)
N-line inversion (Lower) [6_H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	The number of N-line inversion
N-line inversion (Upper) [7_H]	0	1	1	0	0	0	0	0	1	1	1	*	N6	N5	N4	The number of N-line inversion
Display control (1) [8_H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF	SHIFT: Common direction MON: Gradation or B/W display mode ALLON: All pixels ON/OFF ON/OFF: Display ON/OFF
Display control (2) [9_H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	*	REV: Reverse display ON/OFF NLIN: N-line inversion ON/OFF, SWAP: SWAP mode ON/OFF
Increment control [A_H]	0	1	1	0	0	0	0	1	0	1	0	AIM	HV	XD	YD	AIM: Read-modify-write ON/OFF HV: Increment / Decrement direction XD: Column Increment / Decrement set YD: Row Increment / Decrement set
Power control [B_H]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON: Voltage followers ON/OFF HALT: Power save ON/OFF DCON: Voltage booster ON/OFF ACL: Reset
Duty cycle ratio [C_H]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Sets LCD duty cycle ratio
Boost level [D_H]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	Sets boost level
LCD bias ratio [E_H]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Sets LCD bias ratio
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.
Note 2) [N_H] : Address of instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (2)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette A0/A8 (Lower) [0_H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A0/A8 (Upper) [1_H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A1/A9 (Lower) [2_H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A1/A9 (Upper) [3_H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A2/A10 (Lower) [4_H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A2/A10 (Upper) [5_H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A3/A11 (Lower) [6_H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A3/A11 (Upper) [7_H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A4/A12 (Lower) [8_H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A4/A12 (Upper) [9_H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A5/A13 (Lower) [A_H]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A5/A13 (Upper) [B_H]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A6/A14 (Lower) [C_H]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
Gradation palette A6/A14 (Upper) [D_H]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (3)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette A7/A15 (Lower) [0_H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette A7/A15 (Upper) [1_H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette B0/B8 (Lower) [2_H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B0/B8 (Upper) [3_H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PB84	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B1/B9 (Lower) [4_H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B1/B9 (Upper) [5_H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B2/B10 (Lower) [6_H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B2/B10 (Upper) [7_H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B3/B11 (Lower) [8_H]	0	1	1	0	0	1	0	1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B3/B11 (Upper) [9_H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B4/B12 (Lower) [A_H]	0	1	1	0	0	1	0	1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B4/B12 (Upper) [B_H]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B5/B13 (Lower) [C_H]	0	1	1	0	0	1	0	1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
Gradation palette B5/B13 (Upper) [D_H]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.
Note 2) [N_H] : Address of Instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (4)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette B6/B14 (Lower) [0_H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B6/B14 (Upper) [1_H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B7/B15 (Lower) [2_H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette B7/B15 (Upper) [3_H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette C0/C8 (Lower) [4_H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C0/C8 (Upper) [5_H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C1/C9 (Lower) [6_H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C1/C9 (Upper) [7_H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C2/C10 (Lower) [8_H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C2/C10 (Upper) [9_H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C3/C11 (Lower) [A_H]	0	1	1	0	0	1	1	1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C3/C11 (Upper) [B_H]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C4/C12 (Lower) [C_H]	0	1	1	0	0	1	1	1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
Gradation palette C4/C12 (Upper) [D_H]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC44/ PC124	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.
Note 2) [N_H] : Address of Instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (5)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette C5/C13 (Lower) [0_H]	0	1	1	0	1	0	0	0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C5/C13 (Upper) [1_H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/ PC134	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C6/C14 (Lower) [2_H]	0	1	1	0	1	0	0	0	0	1	0	PC63/P C143	PC62/ PC142	PC61/ PC141	PC60/ PC140	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C6/C14 (Upper) [3_H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/ PC154	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C7/C15 (Lower) [4_H]	0	1	1	0	1	0	0	0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Gradation palette C7/C15 (Upper) [5_H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/ PC154	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Initial COM line [6_H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Sets scan-starting common driver
Display control Signal/ Duty Select [7_H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display clock ON/OFF DSE : Duty-1 ON/OFF
Gradation mode control [8_H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	FDC1	FDC2	PWM : Variable/Fixed gradation mode C256 : 256-Color Mode ON/OFF FDC : Boost Clock
Data bus length [9_H]	0	1	1	0	1	0	0	1	0	0	1	*	ABS	CKS	WLS	ABS : ABS mode ON/OFF CKS : Internal/external oscilation WLS : Display data Length
EVR control (Lower) [A_H]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Sets EVR level (Lower bit)
EVR control (Upper) [B_H]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Sets EVR level (Upper bit)
Frequency control [D_H]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Oscillation frequency
Discharge ON/OFF [E_H]	0	1	1	0	1	0	0	1	1	1	0	*	*	DIS2	DIS	Discharge the electric charge in capacitors on V_1 to V_4 and V_{LCD}
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag
Instruction register address [C_H]	0	1	1	0	1	0	0	1	1	0	0	Reading address				Sets instruction register address
Instruction register read	0	1	0	1	0/1	0/1	0/1	*	*	*	*	Read Data				Read out instruction register data

Note 1) * : Don't care.
Note 2) [N_H] : Address of Instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.
Note 4) CKS=0: Internal oscillation mode (default)
CKS=1: External oscillation mode

Instruction Table (6)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Window end column address (Lower) [0_H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Sets column address for end point
Window end column address (Upper) [1_H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Sets column address for end point
Window end row address (Lower) [2_H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Sets row address for end point
Window end row address (Upper) [3_H]	0	1	1	0	1	0	1	0	0	1	1	*	EY6	EY5	EY4	Sets row address for end point
Initial reverse line (Lower) [4_H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Sets address for reverse line
Initial reverse line (Upper) [5_H]	0	1	1	0	1	0	1	0	1	0	1	*	LS6	LS5	LS4	Sets address for reverse line
Last reverse line (Lower) [6_H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Sets address for reverse line
Last reverse line (Upper) [7_H]	0	1	1	0	1	0	1	0	1	1	1	*	LE6	LE5	LE4	Sets address for reverse line
Reverse line display ON/OFF [8_H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink type setting LREV : Reverse line display ON/OFF
Gradation palette setting control / Icon SEG address set [9_H]	0	1	1	0	1	0	1	1	0	0	1	*	*	DMY	PS	PS : gradation setting DMY : Icon SEG address set
PWM control [A_H]	0	1	1	0	1	0	1	1	0	1	0	PWM S	PWM A	PWM B	PWM C	Sets PWM mode
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag

Note 1) * : Don't care.
Note 2) [N_H] : Address of Instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

(32) Instruction descriptions

This chapter provides detail descriptions and instruction registers. Nonexistent instruction codes must not be set into the LSI.

(32-1) Display data write

The “Display data write” instruction is used to write 8-bit display data into the DDRAM.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	0	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display data							

(32-2) Display data read

The “Display data read” instruction is used to read out 8-bit display data from the DDRAM, where the column address and row address must be specified beforehand by the “column address” and “row address” instructions. The dummy read is required just after the “column address” and “row address” instructions.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	0	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display data							

(32-3) Column address

The “column address” instruction is used to specify the column address for the display data’s reading and writing operations. It requires dual bytes for lower 4-bit and upper 4-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for the upper 4-bit.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	AX_3	AX_2	AX_1	AX_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	AX_7	AX_6	AX_5	AX_4

(32-4) Row address

The “row address” instruction is used to specify the row address for the display data read and write operations. It requires dual bytes for lower 4-bit and upper 3-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for upper 3-bit. The row address is specified in between 00_H and $7F_H$. The setting for nonexistent row address between 80_H and FF_H is prohibited.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	AY_3	AY_2	AY_1	AY_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	AY_6	AY_5	AY_4

(32-5) Initial display line

The “Initial display line” instruction is used to specify the line address corresponding to the initial COM line. The initial COM line specified by the “Initial COM line” instruction and indicates the common driver that starts scanning data.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LA_3	LA_2	LA_1	LA_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	LA_6	LA_5	LA_4

LA_6	LA_5	LA_4	LA_3	LA_2	LA_1	LA_0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
1	1	1	1	1	1	1	127

(32-6) N-line inversion

The “N-line inversion” instruction is used to control the alternate rates of the liquid crystal direction. It is programmed to select the N value between 2 and 128, and the FR signal toggles once every N lines by setting “1” into the “NLIN” register of the “Display control (2)” instruction. When the N-line inversion is disabled by setting “0” into the “NLIN” register, the FR signal toggles by the frame.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	N3	N2	N1	N0

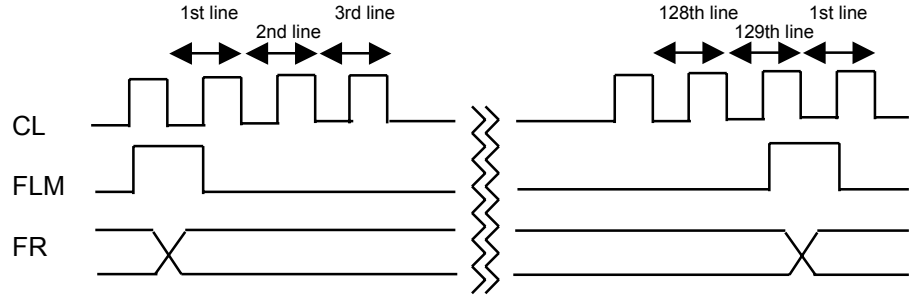
CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	N6	N5	N4

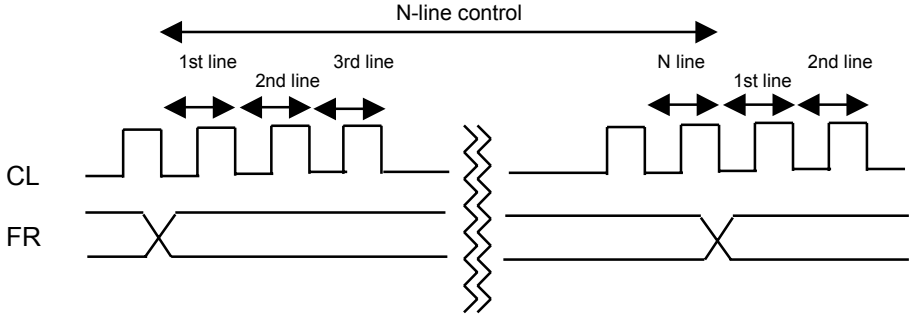
N6	N5	N4	N3	N2	N1	N0	N value
0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	1	2
			:				:
0	1	0	0	0	0	0	128

● N-line Inversion Timing (1/129 duty cycle ratio)

N-line inversion OFF



N-line inversion ON



(32-7) Display control (1)

The “Display control (1)” instruction is used to control display conditions by setting the “Display ON/OFF”, “All pixels ON/OFF”, “Display mode” and “Common direction” registers.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SHIFT	MON	ALLON	ON/OFF

● ON/OFF register

ON/OFF=0 : Display OFF (All COM/SEG output Vss level.)
ON/OFF=1 : Display ON

● All ON register

The “All pixels ON/OFF” register is used to turn on all pixels without changing display data of the DDRAM. The setting for the “All pixels ON/OFF” register has a priority over the “Reverse display ON/OFF” register.

ALLON=0 : Normal
ALLON=1 : All pixels turn on.

● MON register

MON=0 : Gradation mode
MON=1 : B&W mode

● SHIFT register

SHIFT=0 : $COM_0 \rightarrow COM_{127}$
SHIFT=1 : $COM_{127} \rightarrow COM_0$

(32-8) Display control (2)

The “Display control (2)” instruction is used to control display conditions by setting the “SWAP mode ON/OFF”, “N-line inversion ON/OFF” and “Reverse display ON/OFF” registers.

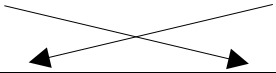
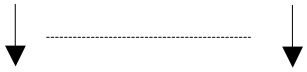
CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	REV	NLIN	SWAP	*

● SWAP register

The “SWAP” register is used to reverse the arrangement of display data in the DDRAM.

SWAP=0 : SWAP mode OFF (Normal)
SWAP=1 : SWAP mode ON

	SWAP=”0”	SWAP=”1”
Write data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
		
RAM data	D7 d6 d5 d4 d3 d2 d1 d0	d0 d1 d2 d3 d4 d5 d6 d7
		
Read data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

● NLIN register

The “NLIN” is used to enable or disable the N-line inversion.

NLIN=0 : N-line inversion OFF (The FR signal toggles by the flame.)
NLIN=1 : N-line inversion ON (The FR signal toggles once every N frames.)

● REV register

The “REV” register is used to enable or disable the reverse display mode that reverses the polarity of display data without changing display data of the DDRAM.

REV=0 : Reverse display mode OFF
REV=1 : Reverse display mode ON

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(32-9) Increment control

The “Increment control” instruction is used for the increment mode. In using the auto-increment mode, DDRAM address automatically increments (+1) whenever the DDRAM is accessed by the “Display data write” or “Display data read” instruction. Therefore, once “Display data write” or “Display data read” instruction is established, it is possible to continuously access to the DDRAM without the “column address” and “row address” instructions. The settings for the “AIM”, “HV”, “XD” and “YD” registers are listed in the following tables.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	AIM	HV	XD	YD

● AIM, HV, XD and YD registers

AIM	Increment mode	Note
0	Auto-increment for both of the display data read and write operations	1
1	Auto-increment for the display write operation (Read modify write)	2

Note 1) It is effective for usual operations accessing successive addresses.

Note 2) It is effective for the read-modify-write operation.

HV	XD	YD	Increment / Decrement mode / Scanning Direction
0	0	0	Column increment / Row increment / Horizontal direction
0	0	1	Column increment / Row decrement / Horizontal direction
0	1	0	Column decrement / Row increment / Horizontal direction
0	1	1	Column decrement / Row decrement / Horizontal direction
1	0	0	Column increment / Row increment / Vertical direction
1	0	1	Column increment / Row decrement / Vertical direction
1	1	0	Column decrement / Row increment / Vertical direction
1	1	1	Column decrement / Row decrement / Vertical direction

For the window area designation, the address directions of RAM (HV, XD, YD) must be set first, and Column address and Row of Start point must be set second, Column address and Row of Stop point must be set third, then RAM should be accessed. Low address must be set first and High address must be set second in all of addresses. The directions of HV, XD, YD should be check to keep the area in RAM.

(32-10) Power control

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	AMPON	HALT	DCON	ACL

● ACL register

The “ACL” register is used to initialize the internal power supply circuits.

ACL=0 : Initialization OFF (Normal)
ACL=1 : Initialization ON

When the data of the “ACL register” is read out by the “Instruction register read” instruction, the read-out data is “1” during the initialization and “0” after the initialization. This initialization is performed by using the signal produced by 2 clocks on the OSC_1. For this reason, the wait time for 2 clocks of the OSC_1 is necessary until next instruction.

● DCON register

The “DCON” register is used to enable or disable the voltage booster.

DCON=0 : Voltage booster OFF
DCON=1 : Voltage booster ON

● HALT register

The “HALT” register is used to enable or disable the power save mode. It is possible to reduce operating current down to stand-by level. The internal status in the power save mode is listed below.

HALT=0 : Power save OFF (Normal)
HALT=1 : Power save ON

Internal status in the power save mode

- The oscillation circuits and internal power supply circuits are halted.
- All segment and common drivers output V_{SS} level.
- The clock input into the OSC_1 is inhibited.
- The display data in the DDRAM is maintained.
- The operational modes before the power save mode are maintained.
- The V_1 to V_4 and V_{LCD} are in the high impedance.

As a power save ON sequence, the “Display OFF” must be executed first, next the “Power save ON” instruction, and then all common and segment drivers output the V_{SS} level. And as power save OFF sequence, the “Power save OFF” instruction is executed first, next the “Display ON” instruction. If the “Power save OFF” instruction is executed in the display ON status, unexpected pixels may instantly turn on.

● AMPON register

The “AMPON” register is used to enable or disable the voltage followers, voltage regulator and EVR.

AMPON=0 : The voltage followers, voltage regulator and the EVR OFF
AMPON=1 : The voltage followers, voltage regulator and the EVR ON

(32-11) Duty cycle ratio

The “Duty cycle ratio” instruction is used to select LCD duty cycle ratio for the partial display function. The partial display function specifies some parts of display area on a LCD panel in the condition of lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. Therefore, it is possible to optimize the LSI’s conditions with extremely low power consumption.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	DS_3	DS_2	DS_1	DS_0

DS_3	DS_2	DS_1	DS_0	Duty cycle ratio		Row way displays
				DSE=0	DSE=1	
0	0	0	0	1/129	1/128	128 commons
0	0	0	1	1/121	1/120	120 commons
0	0	1	0	1/113	1/112	112 commons
0	0	1	1	1/105	1/104	104 commons
0	1	0	0	1/97	1/96	96 commons
0	1	0	1	1/89	1/88	88 commons
0	1	1	0	1/81	1/80	80 commons
0	1	1	1	1/73	1/72	72 commons
1	0	0	0	1/65	1/64	64 commons
1	0	0	1	1/57	1/56	56 commons
1	0	1	0	1/49	1/48	48 commons
1	0	1	1	1/41	1/40	40 commons
1	1	0	0	1/33	1/32	32 commons
1	1	0	1	1/25	1/24	24 commons
1	1	1	0	1/17	1/16	16 commons
1	1	1	1	Inhibited		

The duty cycle ratio is controlled by the “DS_3 to DS_0” registers of the “Duty cycle ratio” instruction and the “DSE” register of the “Display Clock / Duty-1” instruction.

DSE=”0” : The number of commons + 1 (Duty cycle ratio in the default setting)
DSE=”1” : The number of commons (Duty-1)

When the “DSE” is “0”, all common drivers output non-selective levels in period of last common. And the segment drivers output the same data for the last line as the data for previous line: For instance they output the same data for the 128^{th} and 129^{th} lines when the duty cycle ratio is set to 1/129. For the setting of the “DSE” register, see (32-17) “Display clock / Duty-1”.

(32-12) Boost level

The “Boost level” is used to select the multiple of the voltage booster for the partial display function.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	VU_2	VU_1	VU_0

VU_2	VU_1	VU_0	Boost level
0	0	0	1-time (No boost)
0	0	1	2-time
0	1	0	3-time
0	1	1	4-time
1	0	0	5-time
1	0	1	6-time
1	1	0	Inhibited
1	1	1	Inhibited

(32-13) LCD bias ratio

The “LCD bias ratio” is used to select the LCD bias ratio for the partial display function.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	B_2	B_1	B_0

B_2	B_1	B_0	LCD bias ratio
0	0	0	1/9
0	0	1	1/8
0	1	0	1/7
0	1	1	1/6
1	0	0	1/5
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

(32-14) RE flag

The “RE flag” registers are used to determine the contents for the RE registers (RE_2, RE_1 and RE_0) and it is possible to access to the instruction registers.

The data in the “TST_0” register must be “0”, and it is used maker tests only.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	1	TST_0	RE_2	RE_1	RE_0

(32-15) Gradation palette A, B and C

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	0	0	PA_{03}/ PA_{83}	PA_{02}/ PA_{82}	PA_{01}/ PA_{81}	PA_{00}/ PA_{80}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA_{04}/ PA_{84}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	1	0	PA_{13}/ PA_{93}	PA_{12}/ PA_{92}	PA_{11}/ PA_{91}	PA_{10}/ PA_{90}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA_{14}/ PA_{94}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	0	0	PA_{23}/ PA_{103}	PA_{22}/ PA_{102}	PA_{21}/ PA_{101}	PA_{20}/ PA_{100}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA_{24}/ PA_{104}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	1	0	PA_{33}/ PA_{113}	PA_{32}/ PA_{112}	PA_{31}/ PA_{111}	PA_{30}/ PA_{110}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA_{34}/ PA_{114}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	1	0	0	0	PA_{43}/ PA_{123}	PA_{42}/ PA_{122}	PA_{41}/ PA_{121}	PA_{40}/ PA_{120}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PA_{44}/ PA_{124}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PA_{53}/ PA_{133}	PA_{52}/ PA_{132}	PA_{51}/ PA_{131}	PA_{50}/ PA_{130}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PA_{54}/ PA_{134}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PA_{63}/ PA_{143}	PA_{62}/ PA_{142}	PA_{61}/ PA_{141}	PA_{60}/ PA_{140}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PA_{64}/ PA_{144}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PA_{73}/ PA_{153}	PA_{72}/ PA_{152}	PA_{71}/ PA_{151}	PA_{70}/ PA_{150}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PA_{74}/ PA_{154}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB_{03}/ PB_{83}	PB_{02}/ PB_{82}	PB_{01}/ PB_{81}	PB_{00}/ PB_{80}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB_{04}/ PB_{84}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PB_{13}/ PB_{93}	PB_{12}/ PB_{92}	PB_{11}/ PB_{91}	PB_{10}/ PB_{90}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PB_{14}/ PB_{94}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PB_{23}/ PB_{103}	PB_{22}/ PB_{102}	PB_{21}/ PB_{101}	PB_{20}/ PB_{100}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PB_{24}/ PB_{104}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PB_{33}/ PB_{113}	PB_{32}/ PB_{112}	PB_{31}/ PB_{111}	PB_{30}/ PB_{110}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PB_{34}/ PB_{114}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PB_{43}/ PB_{123}	PB_{42}/ PB_{122}	PB_{41}/ PB_{121}	PB_{40}/ PB_{120}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PB_{44}/ PB_{124}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PB_{53}/ PB_{133}	PB_{52}/ PB_{132}	PB_{51}/ PB_{131}	PB_{50}/ PB_{130}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PB_{54}/ PB_{134}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PB_{63}/ PB_{143}	PB_{62}/ PB_{142}	PB_{61}/ PB_{141}	PB_{60}/ PB_{140}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PB_{64}/ PB_{144}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB_{73}/ PB_{153}	PB_{72}/ PB_{152}	PB_{71}/ PB_{151}	PB_{70}/ PB_{150}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB_{74}/ PB_{154}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC_{03}/ PC_{83}	PC_{02}/ PC_{82}	PC_{01}/ PC_{81}	PC_{00}/ PC_{80}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC_{04}/ PC_{84}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PC_{13}/ PC_{93}	PC_{12}/ PC_{92}	PC_{11}/ PC_{91}	PC_{10}/ PC_{90}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PC_{14}/ PC_{94}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PC_{23}/ PC_{103}	PC_{22}/ PC_{102}	PC_{21}/ PC_{101}	PC_{20}/ PC_{100}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PC_{24}/ PC_{104}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PC_{33}/ PC_{113}	PC_{32}/ PC_{112}	PC_{31}/ PC_{111}	PC_{30}/ PC_{110}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PC_{34}/ PC_{114}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PC_{43}/ PC_{123}	PC_{42}/ PC_{122}	PC_{41}/ PC_{121}	PC_{40}/ PC_{120}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PC_{44}/ PC_{124}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PC_{53}/ PC_{133}	PC_{52}/ PC_{132}	PC_{51}/ PC_{131}	PC_{50}/ PC_{130}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PC_{54}/ PC_{134}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PC_{63}/ PC_{143}	PC_{62}/ PC_{142}	PC_{61}/ PC_{141}	PC_{60}/ PC_{140}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PC_{64}/ PC_{144}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC_{73}/ PC_{153}	PC_{72}/ PC_{152}	PC_{71}/ PC_{151}	PC_{70}/ PC_{150}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC_{74}/ PC_{154}

Gradation Palette Table (Variable gradation mode, PWM="0" and MON="0")

(Palette Aj, Palette Bj, Palette Cj, (j=0 to 15))

Palette Value	Gradation Level	Note	Palette Value	Gradation Level	Note
0 0 0 0 0	0/31	Gradation Palette 0 Initial Value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Gradation Palette 8 Initial Value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Gradation Palette 1 Initial Value	1 0 0 1 1	19/31	Gradation Palette 9 Initial Value
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Gradation Palette2 Initial Value	1 0 1 0 1	21/31	Gradation Palette 10 Initial Value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Gradation Palette 3 Initial Value	1 0 1 1 1	23/31	Gradation Palette 11 Initial Value
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Gradation Palette 4 Initial Value	1 1 0 0 1	25/31	Gradation Palette 12 Initial Value
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Gradation Palette 5 Initial Value	1 1 0 1 1	27/31	Gradation Palette 13 Initial Value
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Gradation Palette 6 Initial Value	1 1 1 0 1	29/31	Gradation Palette 14 Initial Value
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Gradation Palette 7 Initial Value	1 1 1 1 1	31/31	Gradation Palette 15 Initial Value

(32-16) Initial COM line

The “Initial COM line” instruction is used to specify the common driver that starts scanning the display data. The line address, corresponding to the initial COM line, is specified by the “Initial display line” instruction.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	SC_3	SC_2	SC_1	SC_0

SC3	SC2	SC1	SC0	Initial COM line (SHIFT=0)	Initial COM line (SHIFT=1)
0	0	0	0	COM_0	COM_{127}
0	0	0	1	COM_4	COM_{123}
0	0	1	0	COM_8	COM_{119}
0	0	1	1	COM_{16}	COM_{111}
0	1	0	0	COM_{24}	COM_{103}
0	1	0	1	COM_{32}	COM_{95}
0	1	1	0	COM_{40}	COM_{87}
0	1	1	1	COM_{48}	COM_{79}
1	0	0	0	COM_{56}	COM_{71}
1	0	0	1	COM_{64}	COM_{63}
1	0	1	0	COM_{72}	COM_{55}
1	0	1	1	COM_{80}	COM_{47}
1	1	0	0	COM_{88}	COM_{39}
1	1	0	1	COM_{96}	COM_{31}
1	1	1	0	COM_{104}	COM_{23}
1	1	1	1	COM_{112}	COM_{15}

SHIFT=0: Positive scan direction (for instance, $COM_0 \rightarrow COM_{127}$)
SHIFT=1: Negative scan direction (for instance, $COM_{127} \rightarrow COM_0$)

(32-17) Display clock / Duty-1

The “Display clock / Duty-1” instruction is used to enable or disable the display clocks (CL, FLM, FR, and CLK), and to control ON/OFF of the “Duty-1”. For more detail about the “Duty-1”, see (32-11) “Duty cycle ratio”.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	DSE	SON

SON=0: CL, FLM, FR, and CLK outputs level “0”.
SON=1: CL, FLM, FR, and CLK outputs are active.

DSE=0: Duty -1 OFF
DSE=1: Duty -1 ON

(32-18) Gradation mode control

The “Gradation mode control” is used to select display mode as follows.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PWM	C256	FDC1	FDC2

● PWM register

PWM=0: Variable gradation mode
(Variable 16-gradation levels out of 32-gradation level of the gradation palette)
PWM=1: Fixed gradation mode
(Fixed 8-gradation levels)

● C256 register

C256=0 256-color mode OFF (4,096-color in the default setting)
C256=1 256-color mode ON

● FDC1 and FDC2 register

FDC1	FDC2	Boost Clock
0	0	×1
0	1	×2
1	0	×4
1	1	×1/2

(32-19) Data bus length

The “Data bus length” instruction is used to select the 8- or 16- bit data bus length and determine the internal or external oscillation. In the 16-bit data bus mode, instruction data must be 16-bit (D_{15} to D_0) as well as display data. However, for the access to the instruction registers, the lower 8-bit data (D_7 to D_0) of the 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	ABS	CKS	WLS

- ABS register

  ABS=0: ABS mode OFF (normal)
  ABS=1: ABS mode ON

- WLS register

  WLS=0: 8-bit data bus length
  WLS =1: 16-bit data bus length

- CKS register

  CKS =0: Internal oscillation
  (The OSC_1 terminal must be fixed “1” or “0”.)
  CKS =1: External oscillation
  (By the external clock into the OSC_1 or external resister between the OSC_1 and OSC_2. OSC_2 should be open when clock is inputted from OSC_1.)

(32-20) EVR control

The “EVR control” instruction is used to fine-tune the LCD driving voltage (V_{LCD}) so that it is possible to optimize the contrast level for a LCD panel.

This instruction must be programmed by upper 3-bit data first, next lower 4-bit data. And it becomes enabled when the lower 4-bit data is programmed, so that it can prevent unexpected high voltage for the VLCD from being generated.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	DV_3	DV_2	DV_1	DV_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	DV_6	DV_5	DV_4

DV_6	DV_5	DV_4	DV_3	DV_2	DV_1	DV_0	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
1	1	1	1	1	1	1	High

The formula of the V_{LCD} is shown below.

V_{LCD} [V] = 0.5 x V_{REG} + M (V_{REG} − 0.5 x V_{REG}) / 127

$V_{BA} = V_{EE} \times 0.9$
$V_{REG} = V_{REF} \times N$

V_{BA} : Output voltage of the reference voltage generator
V_{REF} : Input voltage of the voltage regulator
V_{REG} : Output voltage of the voltage regulator
N : Register value for the voltage booster
M : Register value for the EVR

(32-21) Frequency control

The “Frequency control” instruction is used to control the frame frequency for a LCD panel.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	Rf_2	Rf_1	Rf_0

● Rfx register (x=0, 1, 2)

The “Rfx” register is used to determine the feed back resister value for the internal oscillator and it is possible to adjust the frame frequency for the LCD modules.

Rf 2	Rf 1	Rf 0	Feedback resistor value
0	0	0	Reference value
0	0	1	0.8 x reference value
0	1	0	0.9 x reference value
0	1	1	1.1 x reference value
1	0	0	1.2 x reference value
1	0	1	0.7 x reference value
1	1	0	1.3 x reference value
1	1	1	Inhibited

(32-22) Discharge ON/OFF

Discharge circuit is used to discharge the electric charge of the capacitors on the V_1 to V_4 and the V_{LCD} terminals. The “Discharge ON/OFF” instruction is usually required just after the internal power supply is turned off by setting “0” into the “DCON” and “AMPON” registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	*	DIS2	DIS

DIS=0: Discharge OFF (Capacitors on the V_{LCD}, V_1, V_2, V_3 and V_4)
DIS=1: Discharge ON (Capacitors on the V_{LCD}, V_1, V_2, V_3 and V_4)

DIS2=0: Discharge OFF (Resistance between V_{OUT} and V_{EE})
DIS2=1: Discharge ON (Resistance between V_{OUT} and V_{EE})

Note) V_{OUT} and V_{EE} are internally connected with the resistor (100kΩ typical) in the power-ON.

(32-23) Instruction register address

The “Instruction register address” is used to specify the instruction register address, so that it is possible to read out the contents of the instruction registers in combination with the “Instruction register read” instruction.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	RA_3	RA_2	RA_1	RA_0

(32-24) Instruction register read

The “Instruction register read” instruction is used to read out the contents of the instruction register in combination with the “Instruction register address” instruction.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
*	*	*	*	Internal register data read			

(32-25) Window end column address

The “Window end column address” is used to specify the column address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 4-bit data can be programmed.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	EX_3	EX_2	EX_1	EX_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	EX_7	EX_6	EX_5	EX_4

(32-26) Window end row address set

The “Window end row address” is used to specify the row address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 4-bit data can be programmed.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	EY_3	EY_2	EY_1	EY_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	EY_6	EY_5	EY_4

(32-27) Initial reverse line

The “Initial reverse line” instruction is used to specify the initial reverse line address for the reverse line display. Lower 4-bit data must be programmed first, next upper 3-bit data. It is programmed in between 00_H and $7F_H$ and the line address beyond $7F_H$ is inhibited. The address relation: LSi < LEi (i=7 to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LS_3	LS_2	LS_1	LS_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	LS_6	LS_5	LS_4

(32-28) Last reverse line

The “Last reverse line” instruction is used to specify the last reverse line address for the reverse line display. Lower 4-bit must be programmed first, next upper 3-bit data. It is programmed in between 00_H and $7F_H$ and the line address beyond $7F_H$ is inhibited. The address relation: LSi < LEi (i=7 to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	LE_3	LE_2	LE_1	LE_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	LE_6	LE_5	LE_4

(32-29) Reverse line display ON/OFF

The “Reverse line display ON/OFF” is used to enable or disable the reverse line display for the blink operation and determine the reverse line display mode.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	*	*	BT	LREV

- LREV register

The “LREV” register is used to enable or disable the reverse line display.

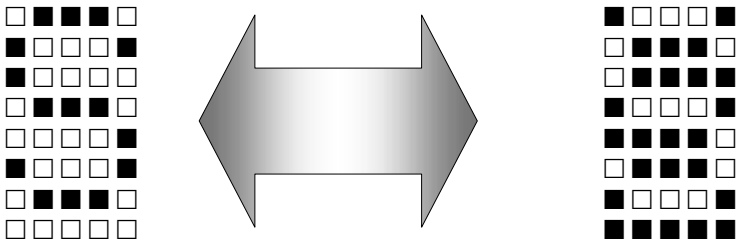
LREV =0: Reverse line display OFF (Normal)
LREV =1: Reverse line display ON

● BT register

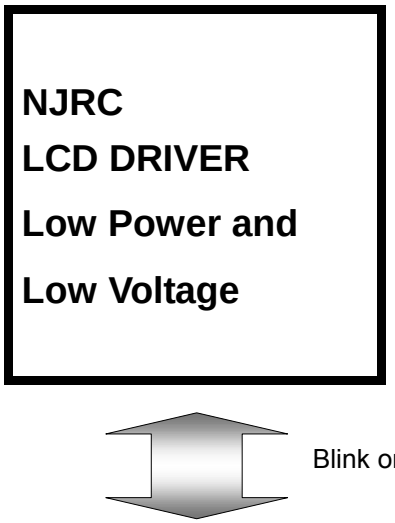
The “BT” register is used to determine the reverse line display mode in the reverse line display ON (LREV=1) status.

BT =0: Normal reverse line display
BT =1: Blink once every 32 frames

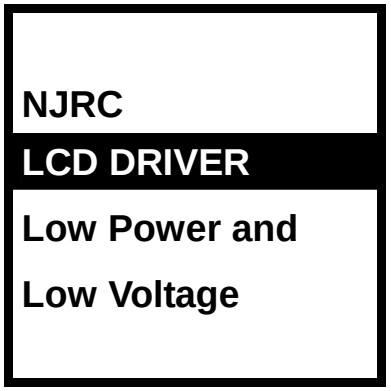
Display examples in the LREV=”1” and BT=”1”



Blink once every 32 frames



Blink once every 32 frames



←Initial reverse line address

←Last reverse line address

(32-30) Gradation palette setting control / Icon SEG address set

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	DMY	PS

- PS register
  PS=0: Lower 8 Gradation setting
  PS=1: Upper 8 Gradation setting

- DMY register
  Although segment drivers in normal condition output LCD driving voltage corresponding to data in Display data RAM, Icon segment driver output LCD driving voltage corresponding to registers. The 24 bits register corresponds to SEGSA0 ~ SEGSA1, SEGSB0 ~ SEGSB1, SEGSC0 ~ SEGSC1.

  DMY=0: Normal RAM access
  DMY=1: Icon segment driver RAM access

(32-31) PWM control

The “PWM control” is used to determine the PWM type for the segment waveforms, where the type can be specified for each of the SEGAi, SEGBi and SEGCi (i=0-127) drivers.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PWMS	PWMA	PWMB	PWMC

● PWMS register

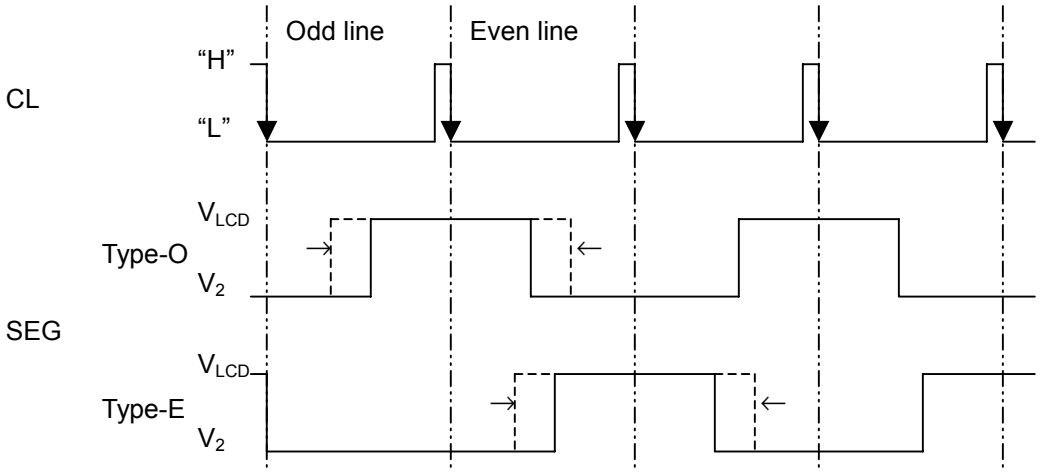
PWMS=0: Type 1
PWMS=1: Type 2

● PWMA, B and C registers

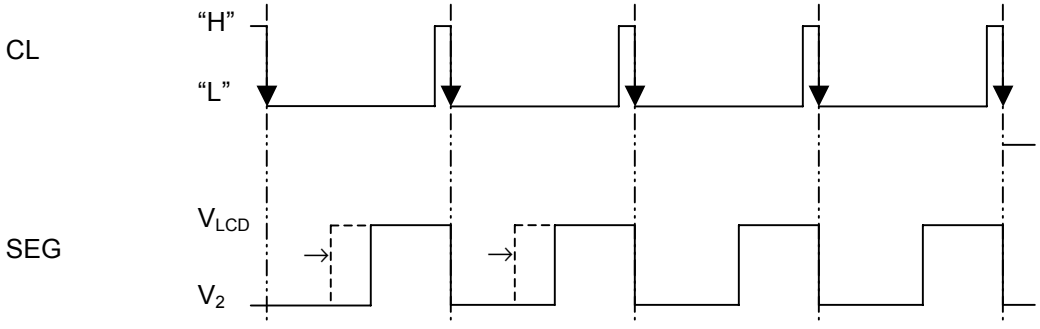
The “PWMA, PWMB and PWMC” registers are used to select the type 1-O or type 1-E.

PWMZ=0 (Z=A, B and C): Type 1-O
PWMZ=1 (Z=A, B and C): Type 1-E

PWM type1 (PWMS=”0”)



PWM type2 (PWMS=”1”)



(33) The relationship between Common drivers and row addresses

Row address assignment of common drivers is programmed by the " SHIFT " register of the " Display control (1) " , " Duty cycle ratio ", " Internal display line " and " Initial COM line " instructions.

- When initial display line is "0"

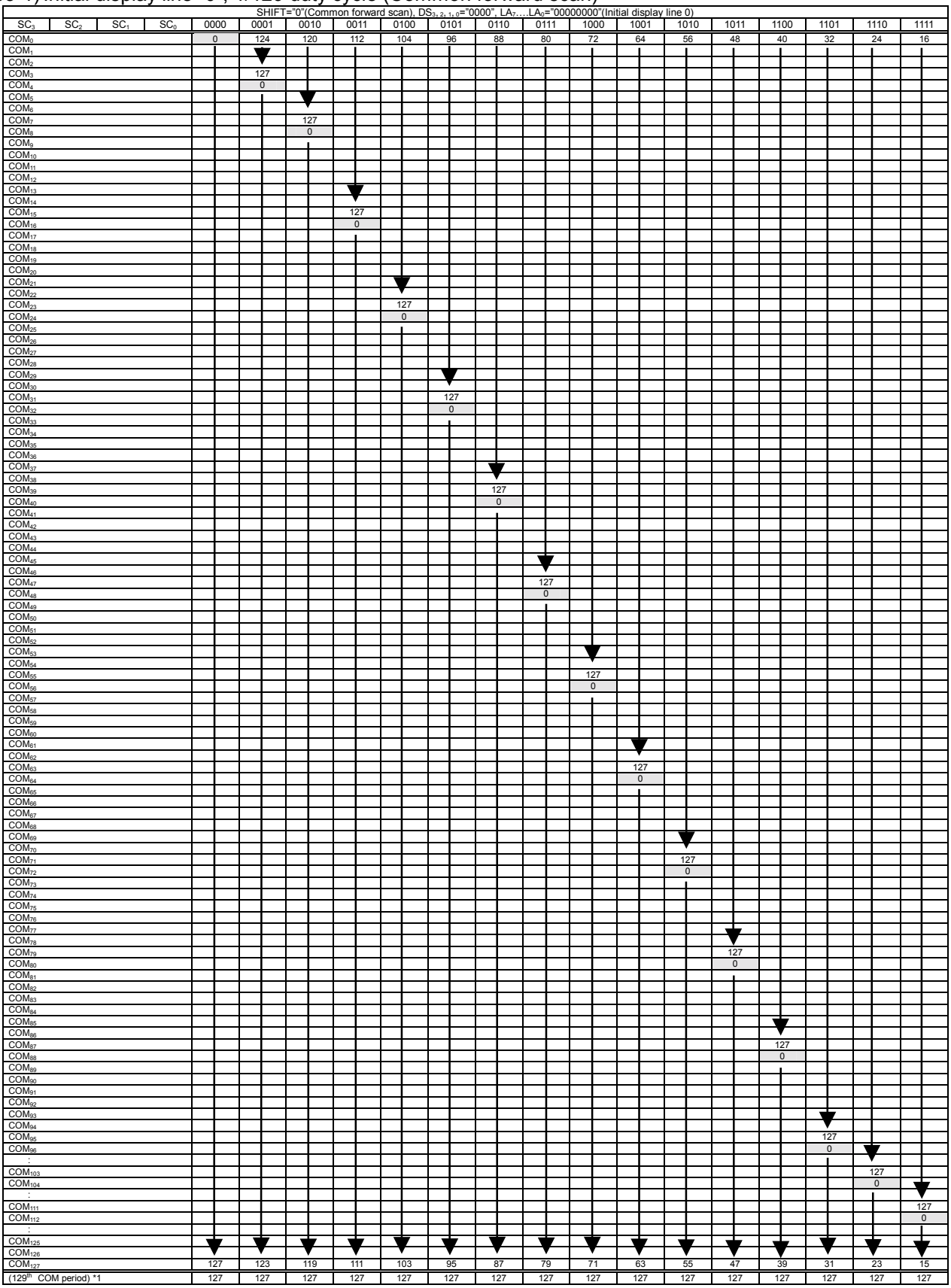
  If the " SHIFT " is " 0 ", the scan direction is normal. When the " LA_0 to LA_6 " registers of the " Initial display line "instruction is " 0 ", the " MY " corresponding to the initial COM line is " 0 " and is increasing during display.

- When initial display line is not "0"

  If the " SHIFT " is " 1 ", the scan direction is inversed. When the " LA_0 to LA_6 " registers of the " Initial display line "instruction is not " 0 ", the " MY " corresponding to the initial COM line is this setting value and is increasing during display.

The following are examples of setting the start-line 0 or 5 at 1/129, 1/128, or 1/17 duty.

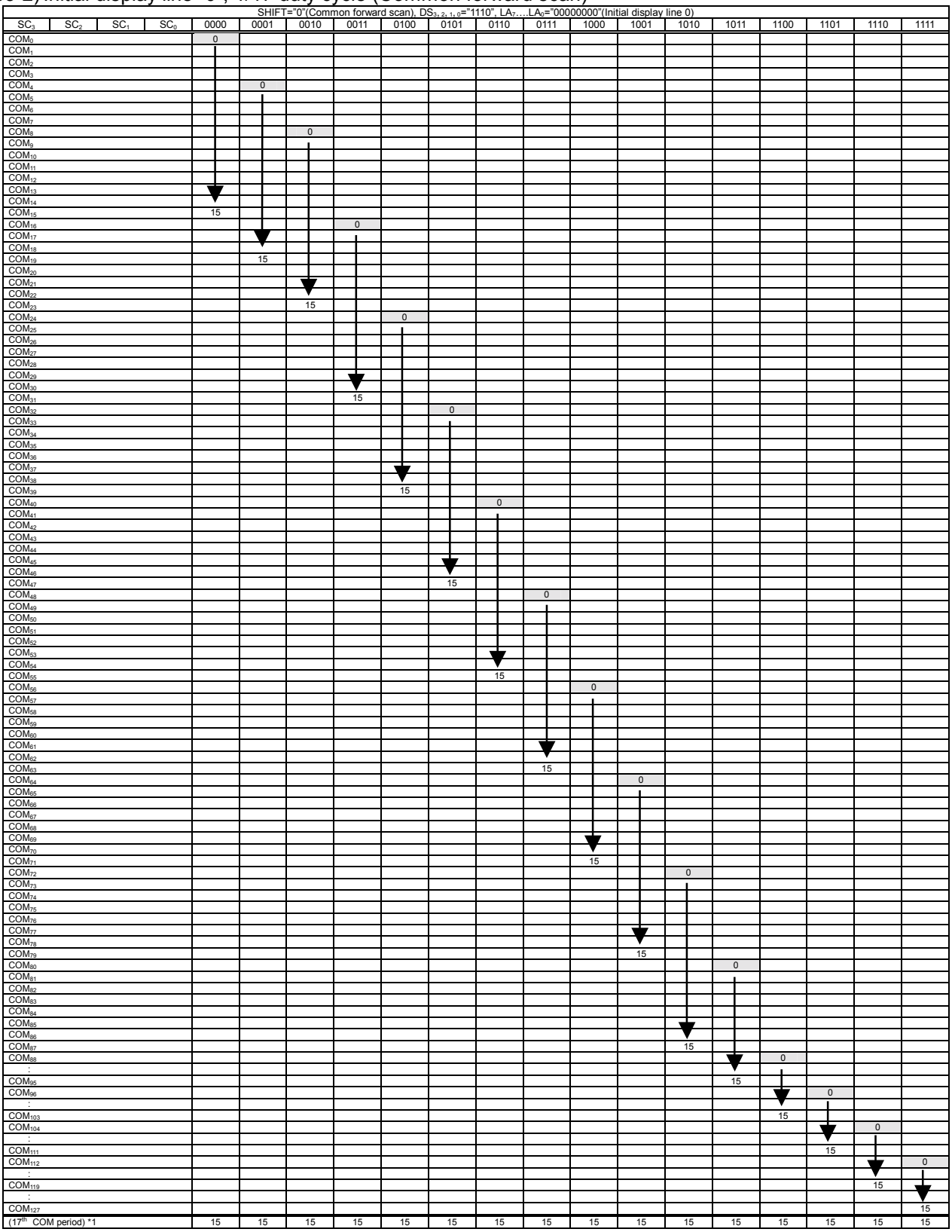
(33-1) Initial display line “0”, 1/129 duty cycle (Common forward scan)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 129th COM period is not selected.

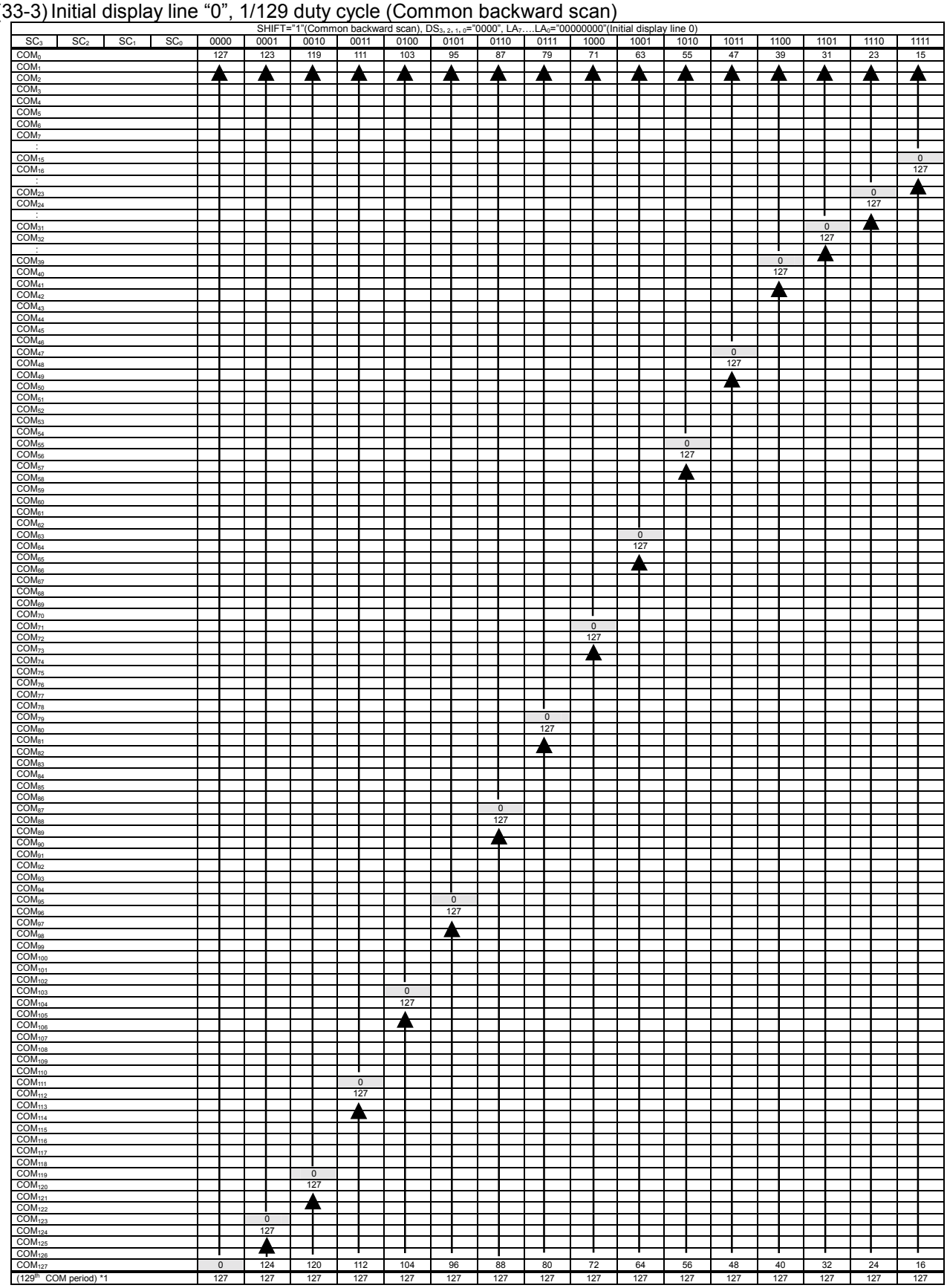
(33-2) Initial display line “0”, 1/17 duty cycle (Common forward scan)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 17th COM period is not selected.

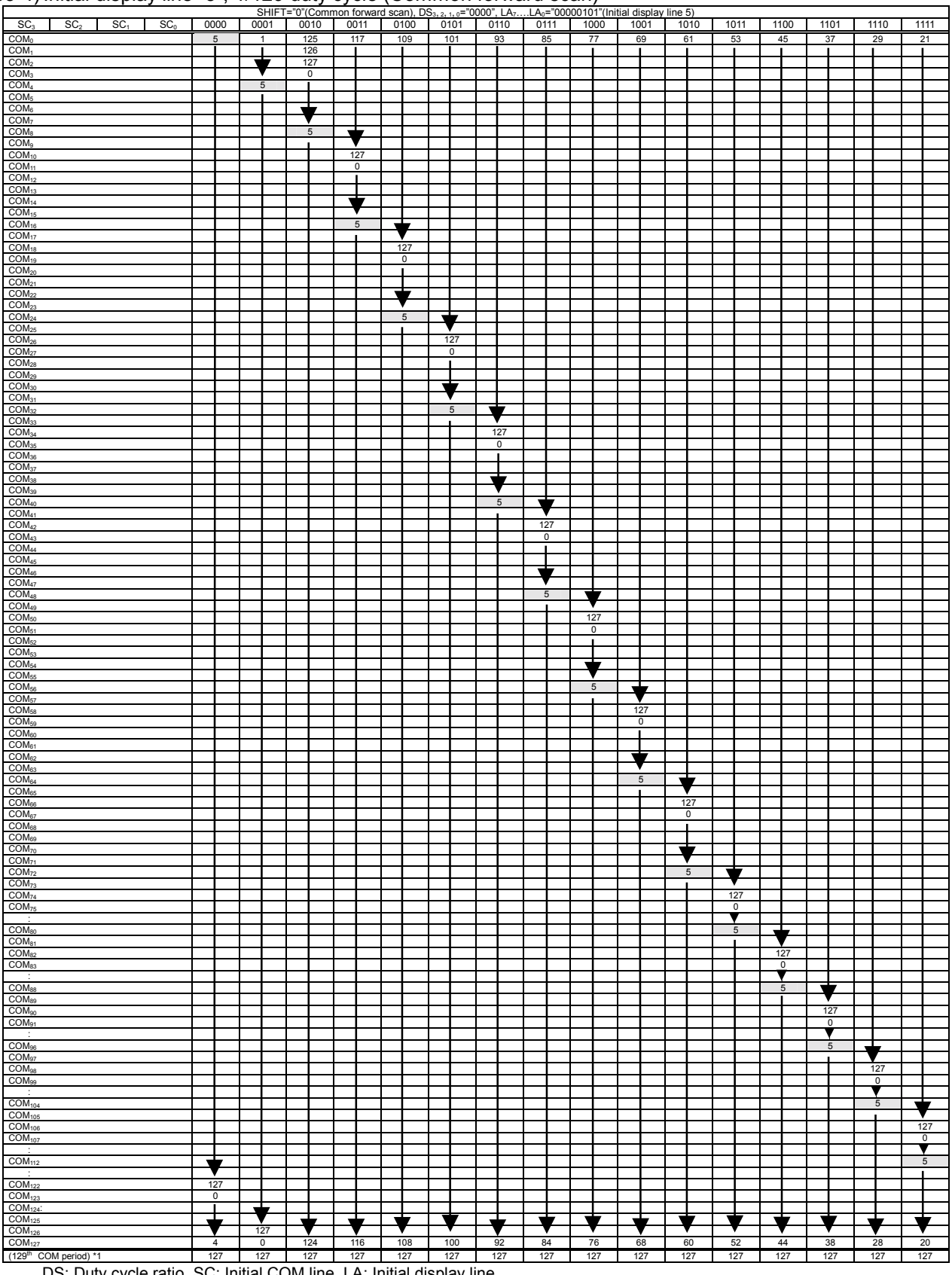
(33-3) Initial display line “0”, 1/129 duty cycle (Common backward scan)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 129th COM period is not selected.

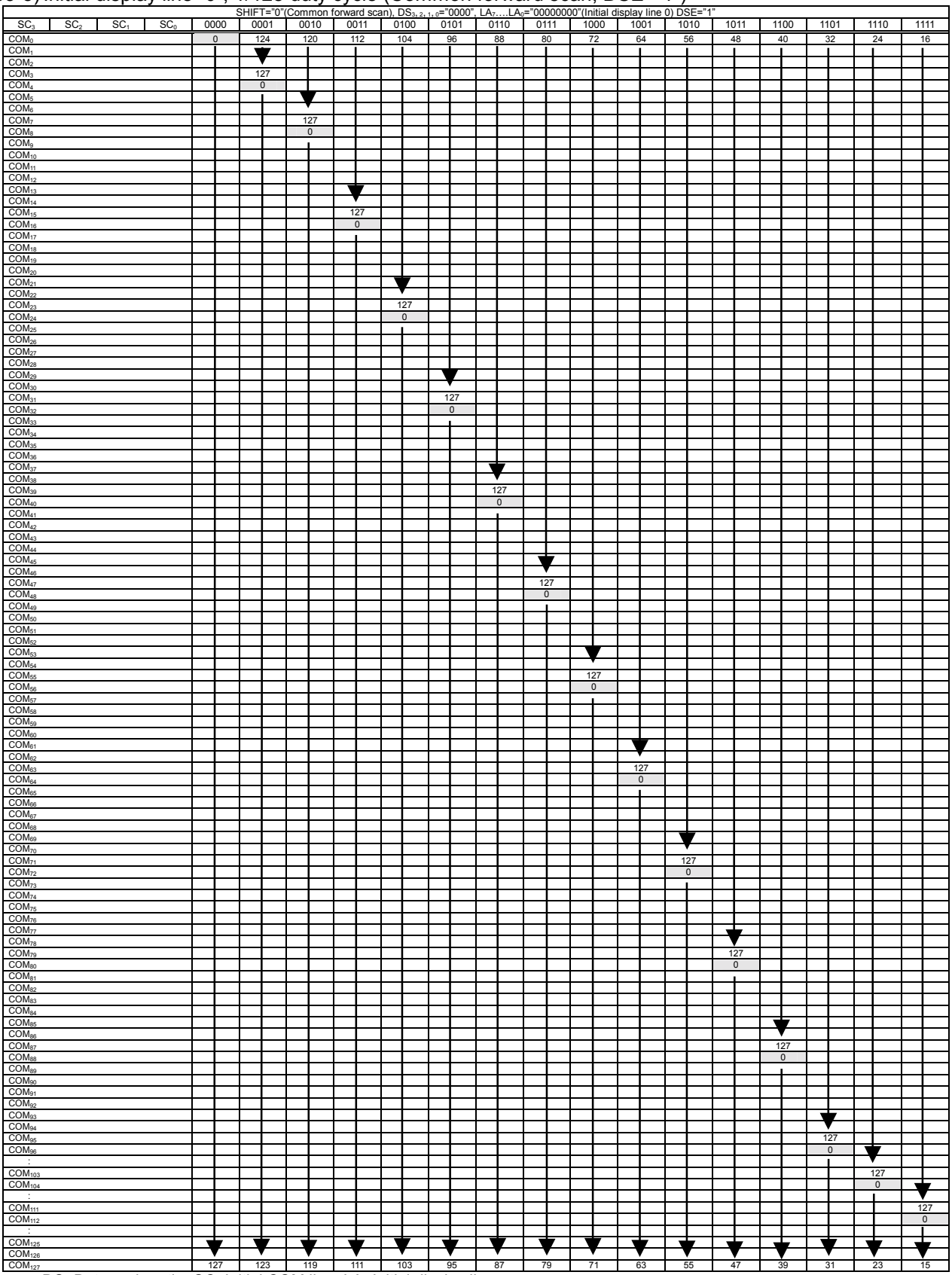
(33-4) Initial display line “5”, 1/129 duty cycle (Common forward scan)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 129th COM period is not selected.

(33-5) Initial display line “0”, 1/128 duty cycle (Common forward scan, DSE=”1”)



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	V_{SS}=0V Ta = +25°C	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +20.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +20.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +20.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to V_{LCD} + 0.3	V
Input Voltage	V_I		*1	-0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{stg}			-45 to +125	°C

Note 1) D_0 to D_{15}, CSb, RS, RDb, WRb, OSC_1, RESb terminals.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	*1
	V_{DD2}		2.4		3.3	V	*2
	V_{EE}	V_{EE}	2.4		3.3	V	*3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	*4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	*5
Operating Temperature	T_{opr}		-30		85	°C	

Note1) Applies to the condition when the reference voltage generator is not used.
Note2) Applies to the condition when the reference voltage generator is used.
Note3) Applies to the condition when the voltage booster is used.
Note4) The following relationship among the supply voltages must be maintained.
$V_{SS}<V_4<V_3<V_2<V_1<V_{LCD}\leq V_{OUT}$
Note5) The relationship: $V_{REF}<V_{EE}$ must be maintained.

■ DC CHARACTERISTICS 1

V_{SS} = 0V, V_{DD} = +1.7 to +3.3V, Ta = -30 to +85°C

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}			0.8 V_{DD}		V_{DD}	V	*1
Low level input voltage	V_{IL}			0		0.2V_{DD}	V	*1
High level output voltage	V_{OH1}	I_{OH} = -0.4mA		V_{DD} - 0.4			V	*2
Low level output voltage	V_{OL1}	I_{OL} = 0.4mA				0.4	V	*2
High level output voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DD} - 0.4			V	*3
Low level output voltage	V_{OL2}	I_{OL} = 0.1mA				0.4	V	*3
Input leakage current	I_{LI}	V_I = V_{SS} or V_{DD}		-10		10	µA	*4
Output leakage current	I_{LO}	V_I = V_{SS} or V_{DD}		-10		10	µA	*5
Driver ON-resistance	R_{ON1}	$\|\Delta V_{ON}\|$ = 0.5V	V_{LCD} = 10V		1	2	kΩ	*6
			V_{LCD} = 6V		2	4		
Stand-by current	I_{STB}	CS=V_{DD}, Ta=25°C	V_{DD} = 3V			15	µA	*7
Internal oscillation Frequency	f_{OSC1}	V_{DD} = 3V Ta = 25°C		490	600	710	kHz	*8
	f_{OSC2}			110	135.5	160		*9
	f_{OSC3}			15.9	19.4	22.9		*10
External oscillation Frequency	f_{r1}	Rf=15kΩ			575		kHz	*11
	f_{r2}	Rf=68kΩ			135			
	f_{r3}	Rf=510kΩ			19.6			
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 6) RL = 500kΩ (V_{OUT} - V_{SS})		(N x V_{EE}) x 0.95			V	*12
Supply current (1)	I_{DD1}	V_{DD} = 3V, 6-time booster Whole ON pattern			760	1140	µA	*13
Supply current (2)	I_{DD2}	V_{DD} = 3V, 6-time booster Checker pattern			930	1400		
Supply current (3)	I_{DD3}	V_{DD} = 3V, 5-time booster Whole ON pattern			520	780		
Supply current (4)	I_{DD4}	V_{DD} = 3V, 5-time booster Checker pattern			650	980		
Supply current (5)	I_{DD5}	V_{DD} = 3V, 4-time booster Whole ON pattern			360	540		
Supply current (6)	I_{DD6}	V_{DD} = 3V, 4-time booster Checker pattern			450	680		
V_{BA} Operating voltage	V_{BA}	V_{EE} = 2.4 to 3.3V		(0.9 V_{EE}) x 0.98	0.9 V_{EE}	(0.9 V_{EE}) x 1.02	V	*14
V_{REG} Operating voltage	V_{REG}	V_{EE} = 2.4 to 3.3V V_{REF} = 0.9 x V_{EE} N-time booster (N=2 to 6)		(V_{REF} x N) x 0.97	(V_{REF} x N)	(V_{REF} x N) x 1.03	V	*15
Output Voltage	V_2			-100	0	+100	mV	*16
	V_3			-100	0	+100		
	V_{D12}			-30	0	+30		
	V_{D34}			-30	0	+30		
	V_{D24}			-30	0	+30		

■ CLOCK and FRAME FREQUENCY

PARAMETER	SYMBOL	Display mode	Display duty cycle ratio (1/D) <DSE=0>				NOTE
			1/129 to 1/81	1/73 to 1/41	1/33 to 1/25	1/17	
Internal clock	f_{OSC}	16 Gradation mode	f_{OSC} / (62xD)	f_{OSC} / (62xDx2)	f_{OSC} / (62xDx4)	f_{OSC} / (62xDx8)	FLM
		Simplified 8 gradation mode	f_{OSC} / (14xD)	f_{OSC} / (14xDx2)	f_{OSC} / (14xDx4)	f_{OSC} / (14xDx8)	
		B&W mode	f_{OSC} / (2xD)	f_{OSC} / (2xDx2)	f_{OSC} / (2xDx4)	f_{OSC} / (2xDx8)	
External clock	f_{CK}	16 Gradation mode	f_{CK} / (62xD)	f_{CK} / (62xDx2)	f_{CK} / (62xDx4)	f_{CK} / (62xDx8)	
		Simplified 8 gradation mode	f_{CK} / (14xD)	f_{CK} / (14xDx2)	f_{CK} / (14xDx4)	f_{CK} / (14xDx8)	
		B&W mode	f_{CK} / (2xD)	f_{CK} / (2xDx2)	f_{CK} / (2xDx4)	f_{CK} / (2xDx8)	

APPLIED TERMINALS and CONDITIONS

Note 1) D_0-D_{15}, CSb, RS, RDb, WRb, P/S, SEL68, RESb
Note 2) D_0-D_{15}
Note 3) CL, FLM, FR, CLK
Note 4) CSb, RS, SEL68, RDb, WRb, P/S, RESb, OSC_1
Note 5) D_0-D_{15} in the high impedance

Note 6) - $SEGA_0$-$SEGA_{127}$, $SEGB_0$-$SEGB_{127}$, $SEGC_0$-$SEGC_{127}$, COM_0-COM_{127} and $SEGSA_0$-$SEGSA_1$, $SEGSB_0$-$SEGSB_1$, $SEGSC_0$-$SEGSC_1$
- Defines the resistance between the COM/SEG terminals and the power supply terminals (V_{LCD}, V_1, V_2, V_3 and V_4) at the condition of 0.5V deference and 1/9 LCD bias ratio.

Note 7) V_{DD}
- The oscillator is halted, CSb="1" (disabled), No-load on the COM/SEG drivers

Note 8) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,0,0) in the variable gradation mode.

Note 9) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,0,0) in the fixed gradation mode.

Note 10) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,0,0) in the Black & White mode.

Note 11) V_{DD}=3V, Ta=25°C

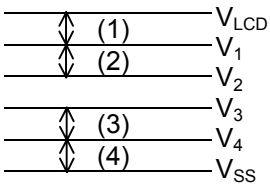
Note 12) V_{OUT}
- Applies to the condition when the internal voltage booster, the internal oscillator and the internal power circuits are used.
- V_{EE}=2.4V to 3.3V, EVR= (1,1,1,1,1,1,1), 1/5 to 1/12 LCD bias, 1/129 duty cycle, No-load on COM/SEG drivers.
- RL=500KΩ between the V_{OUT} and the V_{SS}, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="1", AMPON="1"

Note 13) V_{DD}
- Applies to the condition using the internal oscillator and internal power circuits, no access between the LSI and MPU.
- EVR= (1,1,1,1,1,1,1), All pixels turned-on or checkerboard display in gradation mode. No-load on the COM/SEG drivers.
- V_{DD}=V_{EE}, V_{REF}=0.9V_{EE}, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="1", AMPON="1", NLIN="0", 1/129 Duty cycle, Ta=25°C

Note 14) V_{BA}
- Applies to the condition that V_{BA}=V_{REF} and voltage booster N= 1. DCON="0", V_{OUT}=13.5V input.

Note 15) V_{REG}
- V_{EE}=2.4V to 3.3V, V_{REF}=0.9V_{EE}, V_{OUT}=18V, 1/5 to 1/12 LCD bias ratio, 1/129 duty cycle, EVR=(1,1,1,1,1,1,1)
- Checkerboard display, No-load on the COM/SEG drivers, the voltage booster N=2 to 6, V_1A_1, V_1A_2, V_4A_1, V_4A_2 = "0". CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="0", AMPON="1", NLIN="0"

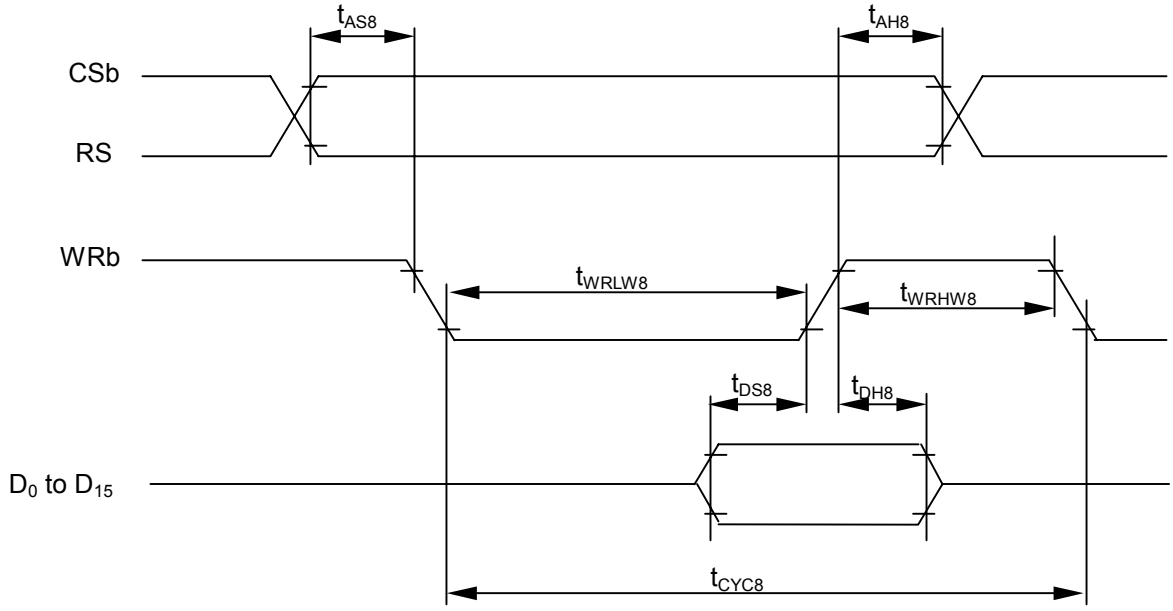
Note 16) V_{LCD}, V_1, V_2, V_3, V_4
- V_{EE}=3.0V, V_{REF}=0.9V_{EE}, V_{OUT}=15V, 1/5 to 1/12 LCD Bias, EVR= (1,1,1,1,1,1,1), Display OFF, No-load on the COM/SEG drivers, voltage booster N=5, V_1A_1, V_1A_2, V_4A_1, V_4A_2 = "0". CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="0", AMPON="1"



V_{D12}: (1)-(2)
V_{D34}: (3)-(4)
V_{D24}: (2)-(4)

■ AC CHARACTERISTICS

- Write operation (80-type MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		90 35 35		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		30 5		ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

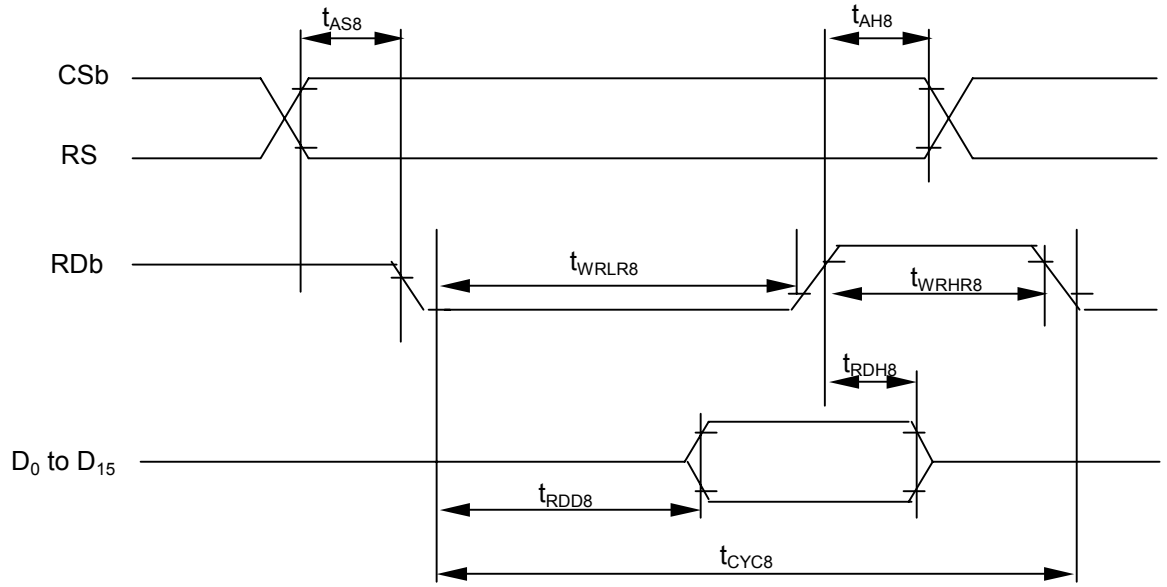
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		160 70 70		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		180 80 80		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		70 10		ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Read operation (80-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDb
Read Data delay time Read Data hold time	T_{RDD8} T_{RDH8}	CL=15pF	 0	60	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

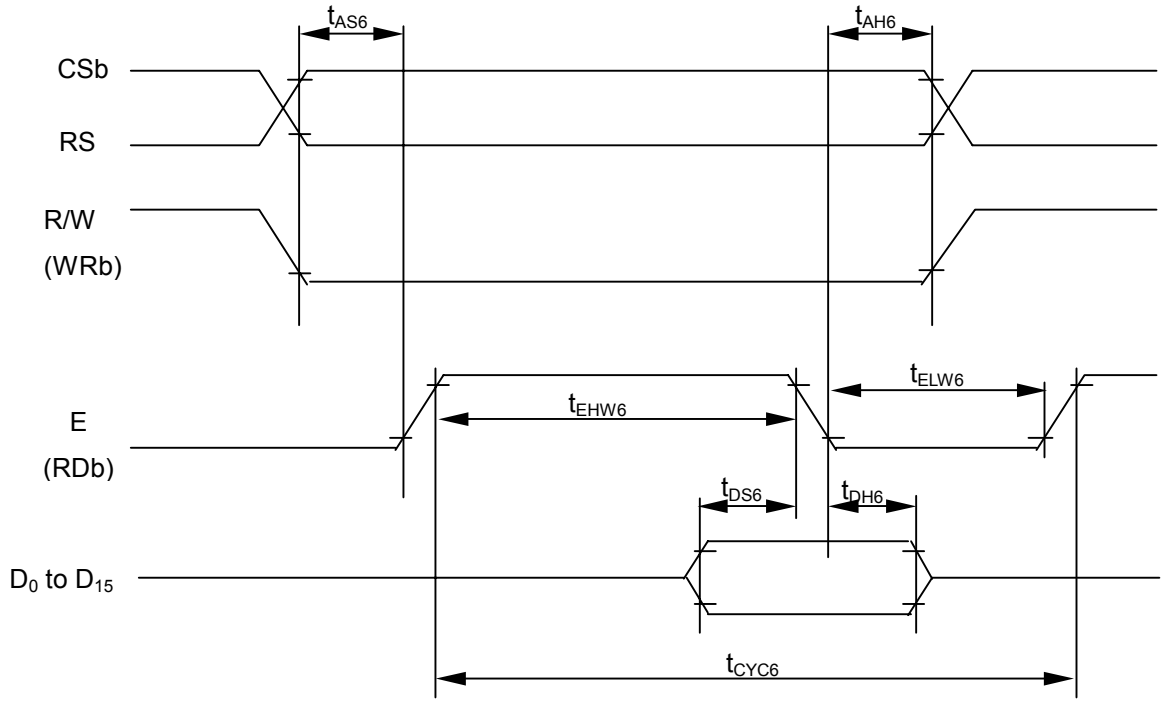
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDb
Read Data delay time Read Data hold time	T_{RDD8} T_{RDH8}	CL=15pF	 0	60	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		250 120 120		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	110	ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Write operation (68-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		90		ns	E
Enable "L" level pulse width	t_{ELW6}		35		ns	
Enable "H" level pulse width	t_{EHW6}		35		ns	
Data setup time	t_{DS6}		40		ns	D_0 to D_{15}
Data hold time	t_{DH6}		5		ns	

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

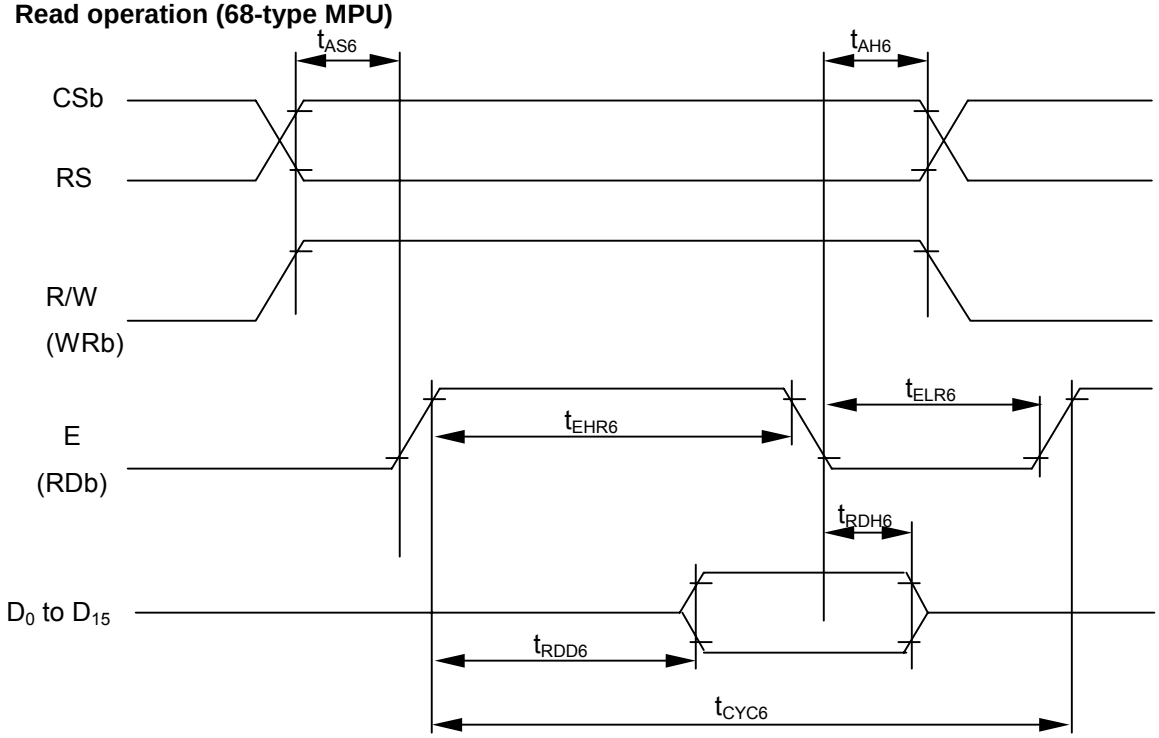
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		160		ns	E
Enable "L" level pulse width	t_{ELW6}		70		ns	
Enable "H" level pulse width	t_{EHW6}		70		ns	
Data setup time	t_{DS6}		50		ns	D_0 to D_{15}
Data hold time	t_{DH6}		5		ns	

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELW6}		80		ns	
Enable "H" level pulse width	t_{EHW6}		80		ns	
Data setup time	t_{DS6}		70		ns	D_0 to D_{15}
Data hold time	t_{DH6}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Read operation (68-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	70	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

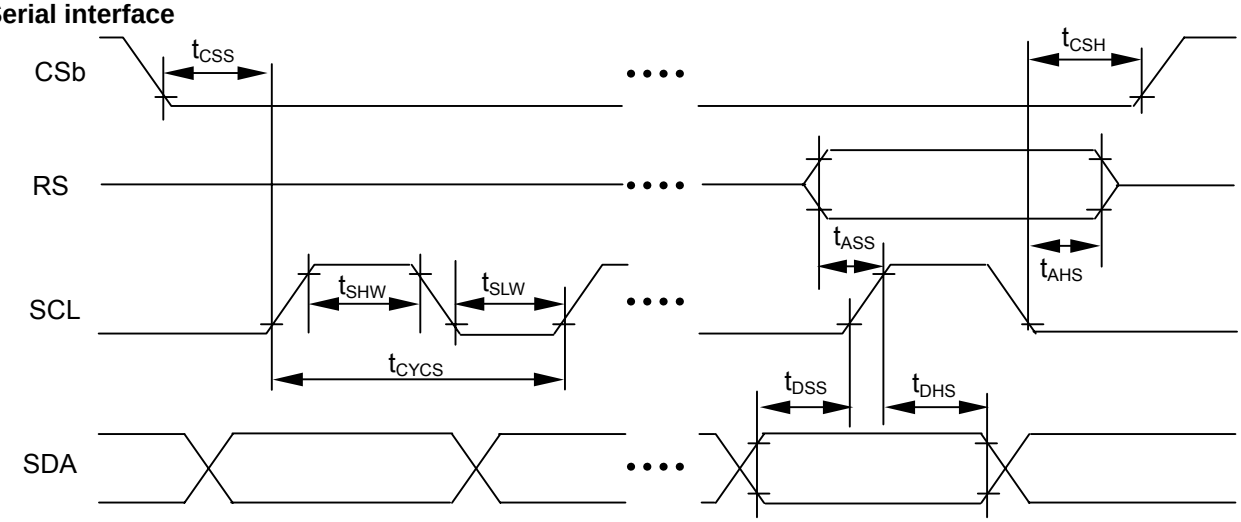
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	70	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		250 120 120		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	110	ns ns	D0 to D15

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Serial interface**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		100		ns	SCL
SCL "H" level pulse width	t_{SHW}		45		ns	
SCL "L" level pulse width	t_{SLW}		45		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

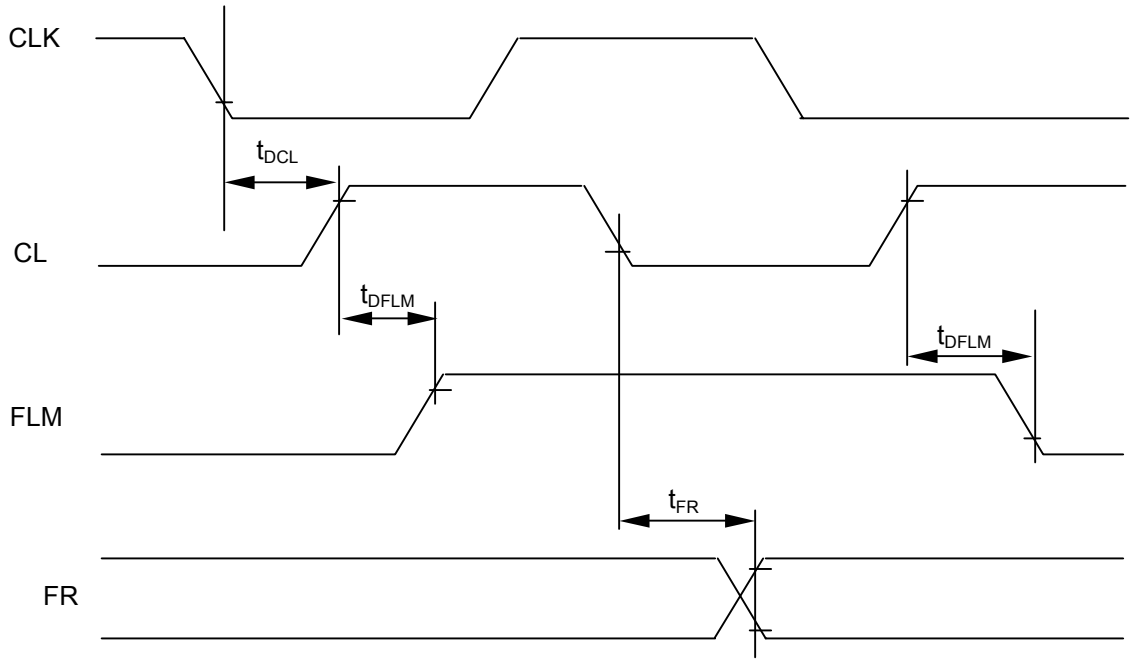
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		100		ns	SCL
SCL "H" level pulse width	t_{SHW}		45		ns	
SCL "L" level pulse width	t_{SLW}		45		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		160		ns	SCL
SCL "H" level pulse width	t_{SHW}		75		ns	
SCL "L" level pulse width	t_{SLW}		75		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Display control timing**



Output timing (V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

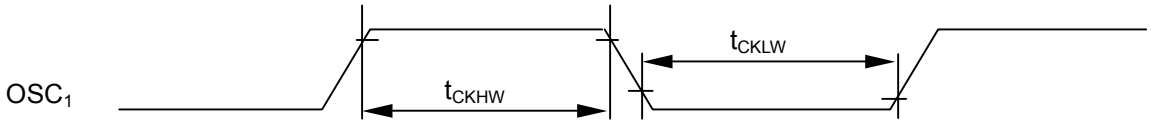
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Output timing (V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Input clock timing**

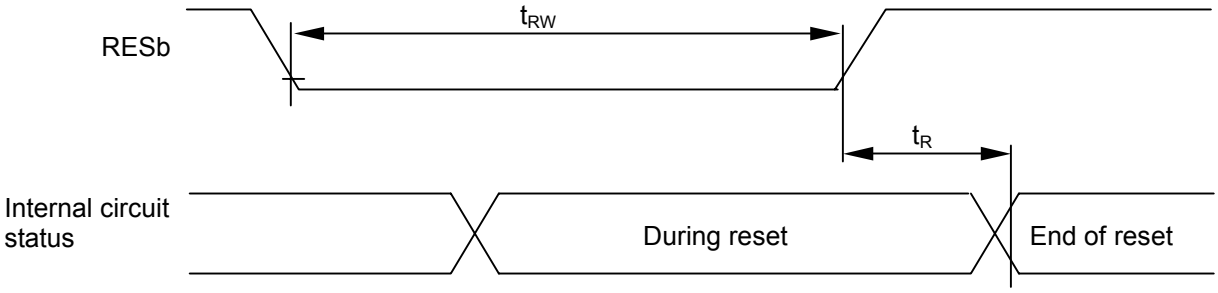


(V_{DD}=1.7 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC_1 "H" level pulse width (1)	t_{CKHW1}		0.70	1.02	μs	OSC_1 ∗1
OSC_1 "L" level pulse width (1)	t_{CKLW1}		0.70	1.02	μs	
OSC_1 "H" level pulse width (2)	t_{CKHW2}		3.13	4.55	μs	OSC_1 ∗2
OSC_1 "L" level pulse width (2)	t_{CKLW2}		3.13	4.55	μs	
OSC_1 "H" level pulse width (3)	t_{CKHW3}		21.8	31.4	μs	OSC_1 ∗3
OSC_1 "L" level pulse width (3)	t_{CKLW3}		21.8	31.4	μs	

Note) Each timing is specified based on 20% and 80% of V_{DD}.
Note 1) Applied to the variable gradation mode / MON="0",PWM="0"
Note 2) Applied to the fixed gradation mode / MON="0",PWM="1"
Note 3) Applied to the B&W mode / MON="1"

- Reset input timing



(V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	µs	
RESb "L" level pulse width	t_{RW}		10.0		µs	RESb

(V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	µs	
RESb "L" level pulse width	t_{RW}		10.0		µs	RESb

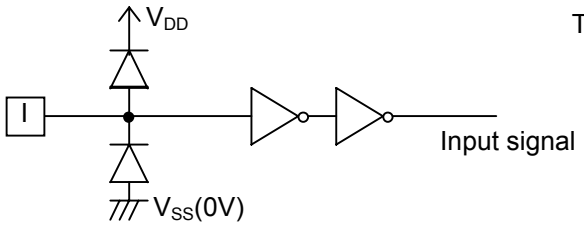
Note) Each timing is specified based on 20% and 80% of V_{DD}.

- Typical characteristic

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Basic delay time of gate	Ta=+25°C, V_{SS}=0V, V_{DD}=3.0V		10		ns

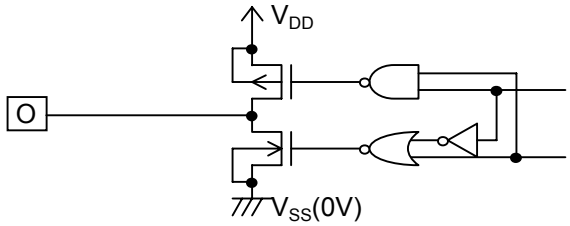
- Input output terminal type

(a) Input circuit



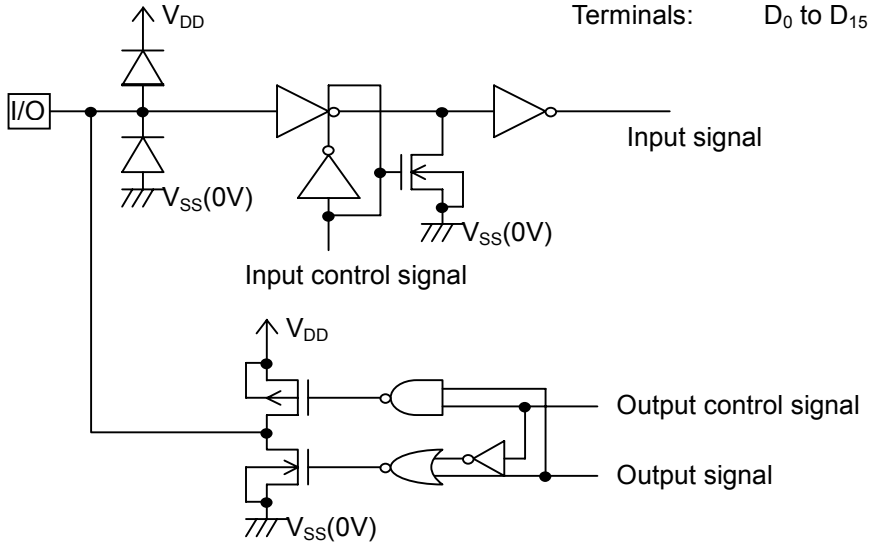
Terminals: CSb, RS, RDb, WRb, SEL68, P/S, RESb

(b) Output circuit



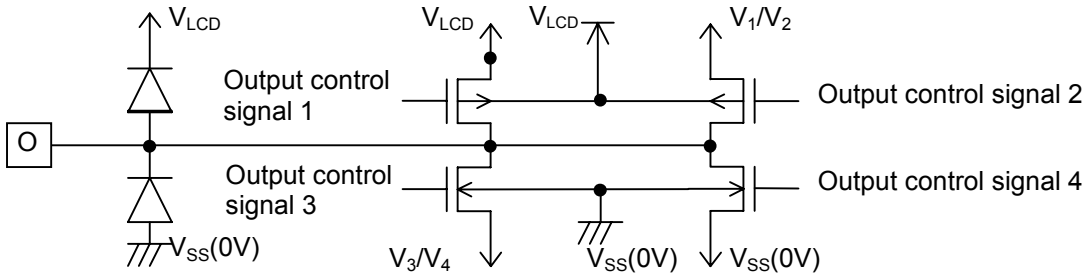
Terminals: FLM, CL, FR, CLK

(c) Input/Output circuit



Terminals: D_0 to D_{15}

(d) Display output circuit

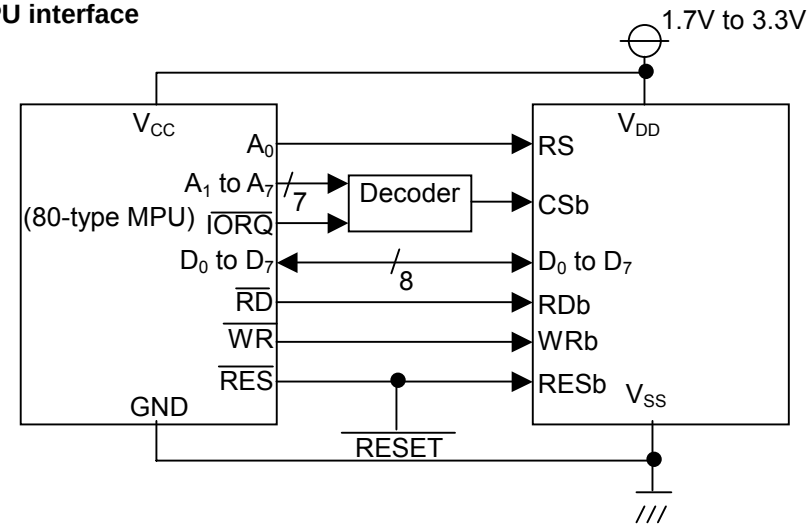


Terminals: $SEGA_0$ to $SEGA_{127}$
$SEGB_0$ to $SEGB_{127}$
$SEGC_0$ to $SEGC_{127}$
COM_0 to COM_{127}
$SEGSA_0$ to $SEGSA_1$
$SEGSB_0$ to $SEGSB_1$
$SEGSC_0$ to $SEGSC_1$

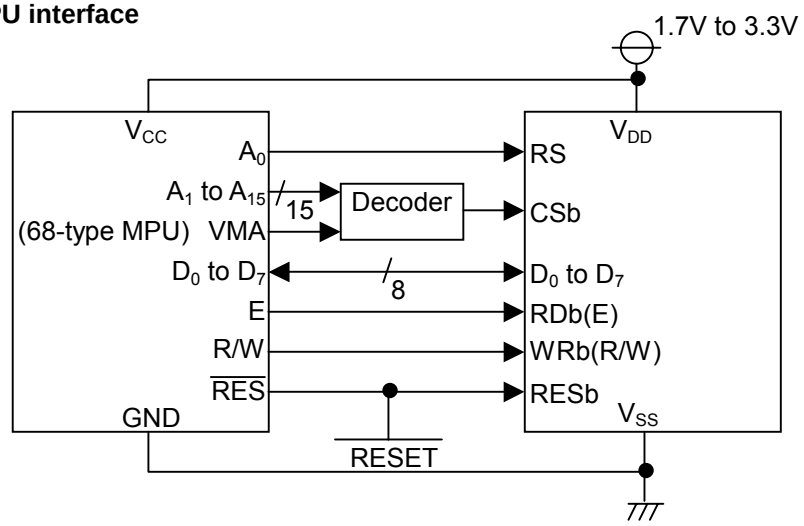
■ APPLICATION CIRCUIT EXAMPLES

(1) MPU Connections

80-type MPU interface



68-type MPU interface



Serial interface