Integrated Device Technology, Inc.

FAST CMOS 32-BIT BUFFER/LINE DRIVER AND BIDIRECTIONAL TRANSCEIVER MODULES

IDT7MP9244T/AT/CT
IDT7MP9245T/AT/CT

FEATURES:

- High density 32-bit FCT Logic modules
- Equivalent to FAST™ speed and drive
- Low profile module 75-pin ZIP (Zig-zag In-line vertical Package)
- Uses 70 mil pitch leads for maximum density
- Surface mount components on a multilayer epoxy laminate (FR-4) substrate
- True TTL input and output compatible
  - — V_{OH} = 3.3V (typ.)
  - — V_{OL} = 0.3V (typ.)
  - — I_{OL} = 64mA
- CMOS power levels (10mW typ. static)
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity

DESCRIPTION:

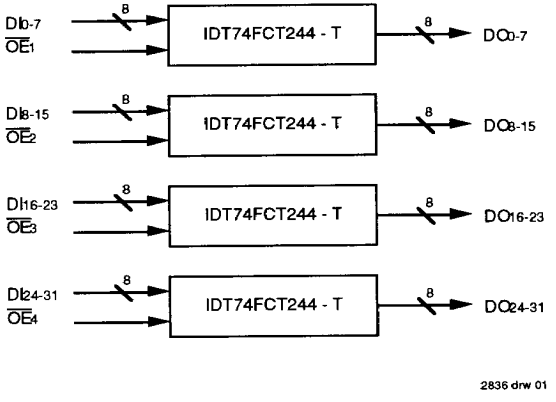
The IDT7MP9244T/AT/CTand IDT7MP9245T/AT/CT logic modules are designed to be employed as 32-bit memory and address drivers, clock drivers and bus-oriented transmitter/receivers which require maximum board packing density. The IDT FCT logic components are built using advanced CEMOS™, a dual metal CMOS technology.

The IDT7MP9244T/AT/CT has byte output enable control and the IDT7MP9245T/AT/CT has word output enable and transmit/receive control.

The IDT7MP9244T/AT/CT and IDT7MP9245T/AT/CT are packaged in a 75 pin ZIP (Zig-zag In-line vertical Package) module offering the optimum in packing density. The dual row (70 mil lead pitch) vertical configuration allows 75 pins to be placed on a package 2.65 inches long, 510 mils tall and only 180 mils thick, resulting in a three-fold density improvement over an equivalent monolithic though-hole implementation.

FUNCTIONAL BLOCK DIAGRAMS

IDT7MP9244



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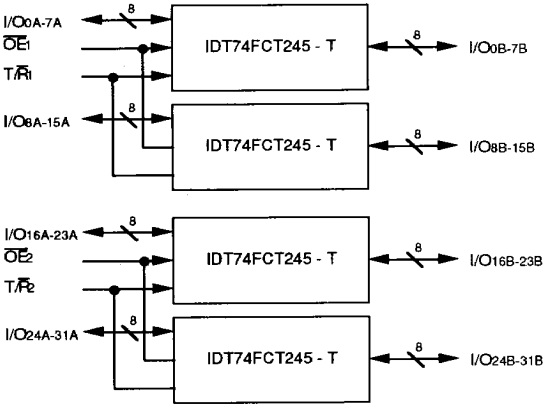
IDT7MP9245



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FAST is a trademark of National Semiconductor Co.

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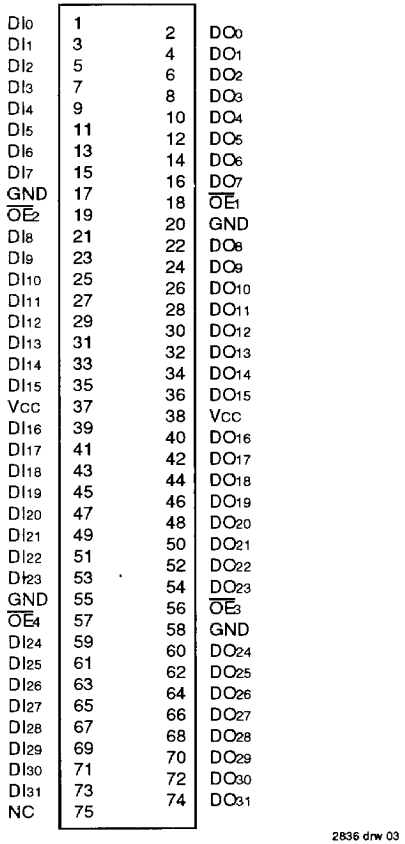
PIN CONFIGURATION

IDT7MP9244



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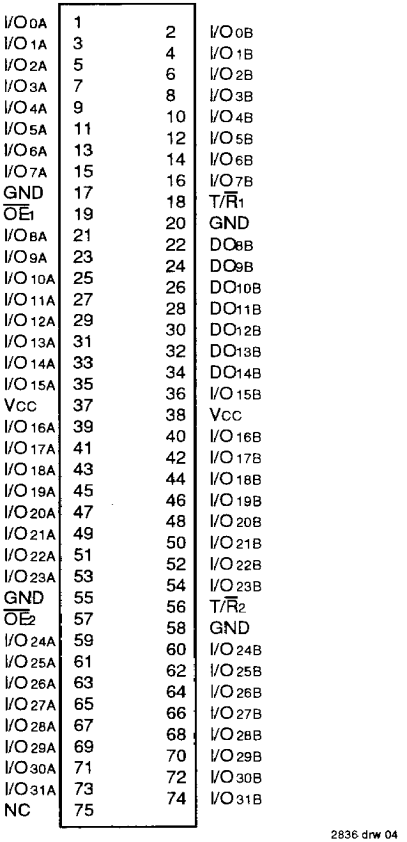
ZIP
TOP VIEW

IDT7MP9245



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ZIP
TOP VIEW

PIN DESCRIPTION - 7MP9244

Pin Names	Description
$\overline{OE}_1$- $\overline{OE}_4$	3–State Output Enable Inputs (Active LOW)
DI0-31	Inputs
DO0-31	Outputs

2836 tbl 01

PIN DESCRIPTION - 7MP9245

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3–State Output Enable Inputs (Active LOW)
T/$\overline{R}_1$, T/$\overline{R}_2$	Transmit/Receive Inputs
I/O0A-31A	Side A Inputs or 3-State Outputs
I/O0B-31B	Side BInputs or 3-State Outputs

2836 tbl 02

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTES: 2836 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

FUNCTION TABLE(1)

7MP9244			7MP9245		
Inputs		Outputs	Inputs		
$\overline{OE}$	D	O	$\overline{OE}$	T/$\overline{R}$	Outputs
L	L	L	L	L	Bus I/OB Data to Bus I/OA
L	H	H	L	H	Bus I/OB Data to Bus I/OA
H	X	Z	H	X	High-Z State

NOTE: 2836 tbl 04
1. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   Z = High Impedance

CAPACITANCE (T_A = +25°C, F = 1.0MHZ)

Symbol	Parameter(1)	Conditions	Max.	Unit
$C_{I/O}$	Input Capacitance (I/O)	V_{IN} = 0V	15	pF
C_{CTRL}	Input Capacitance ($\overline{OE}$, T/$\overline{R}$)	V_{IN} = 0V	30	pF

NOTE: 2836 tbl 05
1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS(4)

(T_A = 0°C TO +70°C, V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	Except I/O Pins	—	—	5	µA
		V_I = 2.7V	I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max.	Except I/O Pins	—	—	–5	µA
		V_I = 0.5V	I/O Pins	—	—	–15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O= 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –8mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	—	0.3	0.55	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	2.0	6.0	mA

NOTES: 2836 tbl 06
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Gross functional testing is performed on the IDT modules; power supply characteristics of the IDT modules are guaranteed by design but not tested.

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POWER SUPPLY CHARACTERISTICS(7)

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open $\overline{OE}$ = T/$\overline{R}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current(5, 6)	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.5	8.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	3.8	9.5	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND 32 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	12.8	26.0	
			V_{IN} = 3.4V V_{IN} = GND	—	20.8	58.0	

2836 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
7. Gross functional testing is performed on the IDT modules; power supply characteristics of the IDT modules are guaranteed by design but not tested.

7-43-4

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR IDT7MP9244[1]

Symbol	Parameter	Condition[2]	7MP9244T		7MP9244AT		7MP9244CT		Unit
			Min.[3]	Max.	Min.[3]	Max.	Min.[3]	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	6.2	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	5.6	1.5	5.2	ns

NOTES: 2836 tbl 08
1. Specifications given are for the IDT74FCT244-T components used on the IDT7MP9244. Functional testing is performed on the IDT7M9244 module; switching characteristics for this module is guaranteed by design but not tested.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR IDT7MP9245[1]

Symbol	Parameter	Condition[2]	7MP9245T		7MP9245AT		7MP9245CT		Unit
			Min.[3]	Max.	Min.[3]	Max.	Min.[3]	Max.	
t_{PLH} t_{PHL}	Propagation Delay I/O_A to I/O_B, I/O_B to I/O_A	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_A or I/O_B		1.5	9.5	1.5	6.2	1.5	5.8	ns
t_{PZH} t_{PZL}	Output Disable Time $\overline{OE}$ to I/O_A or I/O_B		1.5	7.5	1.5	5.0	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time $T/\overline{R}$ to I/O_A or I/O_B		1.5	9.5	1.5	6.2	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time $T/\overline{R}$ to I/O_A or I/O_B		1.5	7.5	1.5	5.0	1.5	4.8	ns

NOTES: 2836 tbl 09
1. Specifications given are for the IDT74FCT245-T components used on the IDT7MP9245. Functional testing is performed on the IDT7M9245 module; switching characteristics for this module is guaranteed by design but not tested.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.

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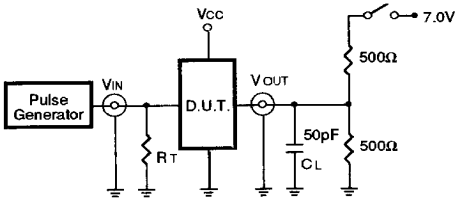
7-43-5

TEST CIRCUITS AND WAVEFORMS (FOR ALL OUTPUTS)



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SWITCH POSITION

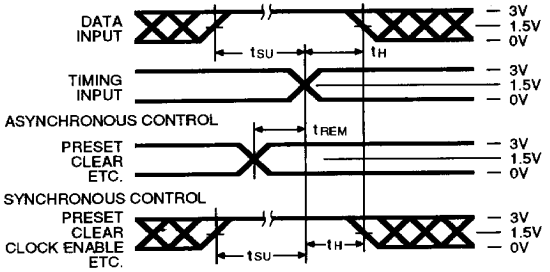
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2836 tbl 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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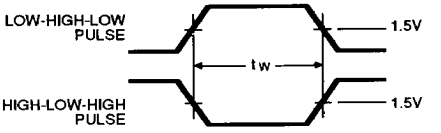
PULSE WIDTH



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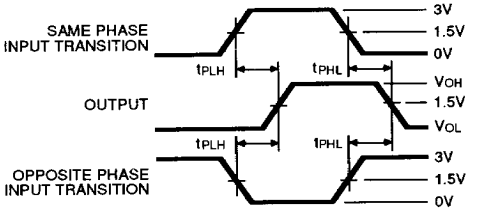
PROPAGATION DELAY



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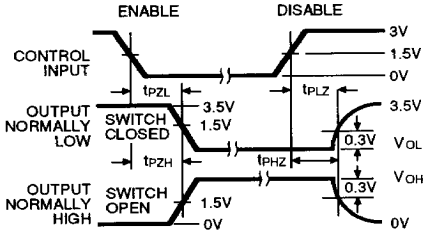
ENABLE AND DISABLE TIMES



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NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

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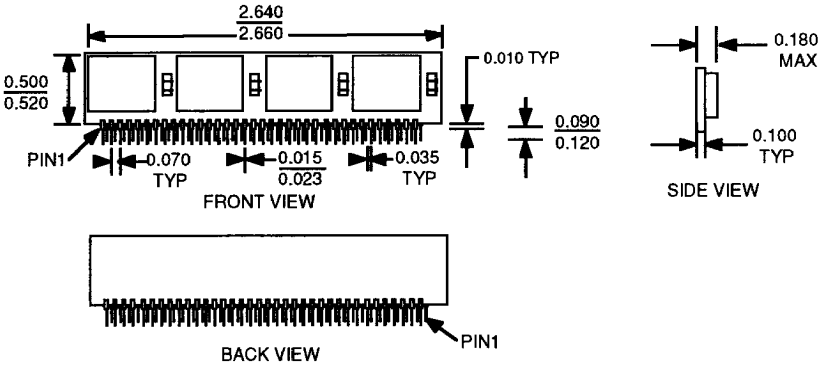
PACKAGE DIMENSIONS



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