

## Low Charge Injection, 8-Channel High Voltage Analog Switch

### Features

- ▶ HVCMOS technology for high performance
- ▶ 3.3V or 5.0V CMOS input logic level
- ▶ 20MHz data shift clock frequency
- ▶ Very low quiescent power dissipation - 10µA
- ▶ Low parasitic capacitance
- ▶ DC to 10MHz analog signal frequency
- ▶ -60dB typical off-isolation at 5MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ Cascadable serial data register with latches
- ▶ Flexible operating supply voltages

### Applications

- ▶ Medical ultrasound imaging
- ▶ NDT metal flaw detection
- ▶ Piezoelectric transducer drivers
- ▶ Inkjet printer heads
- ▶ Optical MEMS modules

### General Description

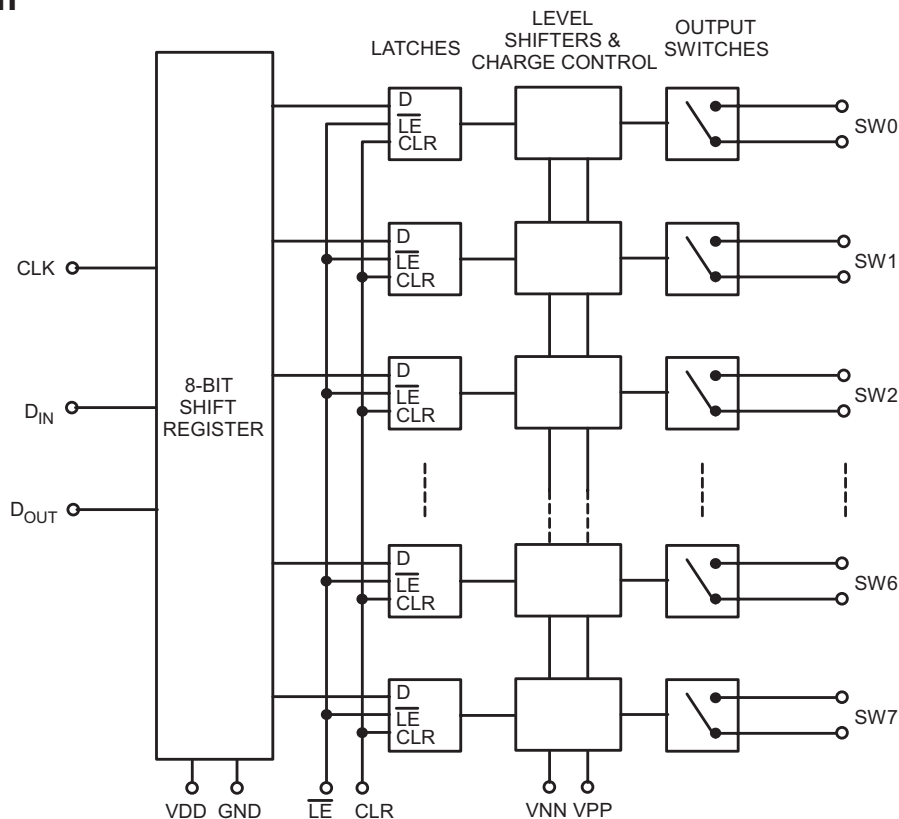
The Supertex HV2203 is a low charge injection 8-channel high voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage signals, such as medical ultrasound imaging, piezoelectric transducer driver, and printers.

Data is input into an 8-bit shift register that can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, the latch enable bar should be left high until all bits are clocked in. Data is clocked in during the rising edge of the clock.

Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g.,  $V_{PP}/V_{NN}$ : +40V/-120V, +80V/-80V, and +120V/-40V.

### Block Diagram



## Ordering Information

Device	Package Options	
	48-Lead LQFP	28-Lead PLCC
HV2203	HV2203FG-G	HV2203PJ-G

-G indicates package is RoHS compliant ("Green")



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## Absolute Maximum Ratings

Parameter	Value
V <sub>DD</sub> logic supply	-0.5V to +6.5V
V <sub>PP</sub> -V <sub>NN</sub> differential supply	170V
V <sub>PP</sub> positive supply	-0.5V to V <sub>NN</sub> +170V
V <sub>NN</sub> negative supply	+0.5V to -170V
Logic input voltage	-0.5V to V <sub>DD</sub> +0.3V
Analog signal range	V <sub>NN</sub> to V <sub>PP</sub>
Peak analog signal current/channel	1.0A
Storage temperature	-65°C to 150°C
Thermal resistance ( $\theta_{ja}$ ): 48-Lead LQFP (FG)	61°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

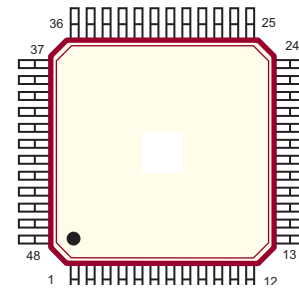
## Operating Conditions

Sym	Parameter	Value
V <sub>DD</sub>	Logic power supply voltage	3.0V to 5.5V
V <sub>PP</sub>	Positive high voltage supply	40V to V <sub>NN</sub> +160V
V <sub>NN</sub>	Negative high voltage supply	-40V to -120V
V <sub>IH</sub>	High level input voltage	0.9V <sub>DD</sub> to V <sub>DD</sub>
V <sub>IL</sub>	Low-level input voltage	0V to 0.1V <sub>DD</sub>
V <sub>SIG</sub>	Analog signal voltage peak-to-peak	V <sub>NN</sub> +10V to V <sub>PP</sub> -10V
T <sub>A</sub>	Operating free air temperature	0°C to 70°C

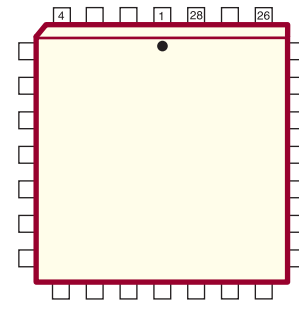
### Notes:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V<sub>SIG</sub> must be V<sub>NN</sub> ≤ V<sub>SIG</sub> ≤ V<sub>PP</sub> or floating during power up/down transition.
3. Rise and fall times of power supplies V<sub>DD</sub>, V<sub>PP</sub> and V<sub>NN</sub> should not be less than 1.0msec.

## Pin Configurations



48-Lead LQFP (FG)



28-Lead PLCC (PJ)

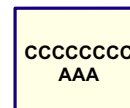
## Product Marking

### Top Marking



YY = Year Sealed  
WW = Week Sealed  
L = Lot Number  
C = Country of Origin\*

### Bottom Marking

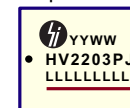


A = Assembler ID\*  
— = "Green" Packaging

\*May be part of top marking

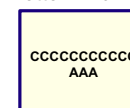
48-Lead LQFP (FG)

### Top Marking



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### Bottom Marking



A = Assembler ID\*  
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\*May be part of top marking

28-Lead PLCC (PJ)

**DC Electrical Characteristics**

(Over operating conditions unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R <sub>ONS</sub>	Small signal switch on-resistance	-	-	-	50	60	-	-	Ω	I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +40V V <sub>NN</sub> = -120V
		-	-	-	42	51	-	-		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -120V
		-	-	-	40	48	-	-		I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +80V V <sub>NN</sub> = -80V
		-	-	-	32	39	-	-		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -80V
		-	-	-	38	46	-	-		I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +120V V <sub>NN</sub> = -40V
		-	-	-	29	35	-	-		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -40V
ΔR <sub>ONS</sub>	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	I <sub>SIG</sub> = 5.0mA, V <sub>PP</sub> = +80V, V <sub>NN</sub> = -80V	
R <sub>ONL</sub>	Large signal switch on-resistance	-	-	-	30	-	-	-	Ω	V <sub>SIG</sub> = V <sub>PP</sub> -10V, I <sub>SIG</sub> = 0.5A	
I <sub>SOL</sub>	Switch off leakage per switch	-	5.0	-	1.0	10	-	15	μA	V <sub>SIG</sub> = V <sub>PP</sub> -10V, V <sub>NN</sub> +10V	
V <sub>OS</sub>	DC offset switch off	-	300	-	100	300	-	300	mV	100kΩ load	
	DC offset switch on	-	500	-	100	500	-	500			
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches off	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-	μA	All switches off	
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches on, I <sub>SW</sub> = 5.0mA	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-	μA	All switches on, I <sub>SW</sub> = 5.0mA	
I <sub>SW</sub>	Switch output peak current	-	-	-	1.0	-	-	-	A	V <sub>SIG</sub> duty cycle < 0.1%, 1.0μs	
f <sub>SW</sub>	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I <sub>PP</sub>	Average V <sub>PP</sub> supply current	-	-	1.0	1.2	1.5	-	-	mA	V <sub>PP</sub> = +40V V <sub>NN</sub> = -120V	All output switches are turning on and off at 50kHz with no load
		-	-	1.0	1.2	1.5	-	-		V <sub>PP</sub> = +80V V <sub>NN</sub> = -80V	
		-	-	1.0	1.2	1.5	-	-		V <sub>PP</sub> = +120V V <sub>NN</sub> = -40V	
I <sub>NN</sub>	Average V <sub>NN</sub> supply current	-	-	1.0	1.2	1.5	-	-	mA	V <sub>PP</sub> = +40V V <sub>NN</sub> = -120V	All output switches are turning on and off at 50kHz with no load
		-	-	1.0	1.2	1.5	-	-		V <sub>PP</sub> = +80V V <sub>NN</sub> = -80V	
		-	-	1.0	1.2	1.5	-	-		V <sub>PP</sub> = +120V V <sub>NN</sub> = -40V	
I <sub>DD</sub>	Average V <sub>DD</sub> supply current	-	4.0	-	-	4.0	-	4.0	mA	f <sub>CLK</sub> = 5.0MHz, V <sub>DD</sub> = 5.0V	
I <sub>DDQ</sub>	Quiescent V <sub>DD</sub> supply current	-	10	-	-	10	-	10	μA	All logic inputs are static	
I <sub>SOR</sub>	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V <sub>OUT</sub> = V <sub>DD</sub> -0.7V	
I <sub>SINK</sub>	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V <sub>OUT</sub> = 0.7V	
C <sub>IN</sub>	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

**AC Electrical Characteristics**

(Over recommended operating conditions:  $V_{DD} = 5.0V$ ,  $t_R = t_F \leq 5ns$ , 50% duty cycle,  $C_{LOAD} = 20pF$ , unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C			Conditions
		Min	Max	Min	Typ	Max	Min	Max		
$t_{SD}$	Set up time before $\overline{LE}$ rises	25	-	25	-	-	25	-	ns	---
$t_{WLE}$	Time width of $\overline{LE}$	56	-	-	56	-	56	-	ns	$V_{DD} = 3.0V$
		12	-	-	12	-	12	-		$V_{DD} = 5.0V$
$t_{DO}$	Clock delay time to data out	50	100	50	78	100	50	100	ns	$V_{DD} = 3.0V$
		15	40	15	30	40	15	40		$V_{DD} = 5.0V$
$t_{WCL}$	Time width of CLR	55	-	55	-	-	55	-	ns	---
$t_{SU}$	Set up time data to clock	21	-	-	21	-	21	-	ns	$V_{DD} = 3.0V$
		7.0	-	-	7.0	-	7.0	-		$V_{DD} = 5.0V$
$t_H$	Hold time data from clock	2.0	-	2.0	-	-	2.0	-	ns	$V_{DD} = 3.0$ or $5.0V$
$f_{CLK}$	Clock frequency	-	8.0	-	-	8.0	-	8.0	MHz	$V_{DD} = 3.0V$
		-	20	-	-	20	-	20		$V_{DD} = 5.0V$
$t_R, t_F$	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
$t_{ON}$	Turn on time	-	5.0	-	-	5.0	-	5.0	$\mu s$	$V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10k\Omega$
$t_{OFF}$	Turn off time	-	5.0	-	-	5.0	-	5.0	$\mu s$	$V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10k\Omega$
dv/dt	Maximum $V_{SIG}$ slew rate	-	20	-	-	20	-	20	V/ns	$V_{PP} = +40V, V_{NN} = -120V$
		-	20	-	-	20	-	20		$V_{PP} = +80V, V_{NN} = -80V$
		-	20	-	-	20	-	20		$V_{PP} = +120V, V_{NN} = -40V$
$K_O$	Off isolation	-30	-	-30	-33	-	-30	-	dB	$f = 5.0MHz, 1.0k\Omega/15pF$ load
		-58	-	-58	-	-	-58	-		$f = 5.0MHz, 50\Omega$ load
$K_{CR}$	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	$f = 5.0MHz, 50\Omega$ load
$I_{ID}$	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	-	-	-	6.5	-	-	-	pF	0V, $f = 1.0MHz$
$C_{SG(ON)}$	On capacitance SW to GND	-	-	-	21.7	-	-	-	pF	0V, $f = 1.0MHz$
$+V_{SPK}$	Output voltage spike	-	-	-	18	-	-	-	mV	$V_{PP} = +40V, V_{NN} = -120V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	60	-	-	-		
$+V_{SPK}$		-	-	-	30	-	-	-		$V_{PP} = +80V, V_{NN} = -80V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	60	-	-	-		
$+V_{SPK}$		-	-	-	33	-	-	-		$V_{PP} = +120V, V_{NN} = -40V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	60	-	-	-		
QC	Charge injection	-	-	-	270	-	-	-	pC	$V_{PP} = +40V, V_{NN} = -120V, V_{SIG} = 0V$
		-	-	-	220	-	-	-		$V_{PP} = +80V, V_{NN} = -80V, V_{SIG} = 0V$
		-	-	-	152	-	-	-		$V_{PP} = +120V, V_{NN} = -40V, V_{SIG} = 0V$

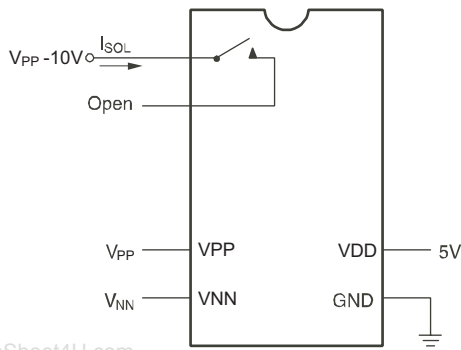
## Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	Off							
H								L	L	On							
	L							L	L		Off						
	H							L	L		On						
		L						L	L			Off					
		H						L	L			On					
			L					L	L				Off				
			H					L	L				On				
				L				L	L					Off			
				H				L	L					On			
					L			L	L						Off		
					H			L	L						On		
						L		L	L							Off	
						H		L	L							On	
							L	L	L								Off
							H	L	L								On
X	X	X	X	X	X	X	X	H	L	Hold Previous State							
X	X	X	X	X	X	X	X	X	H	All Switches Off							

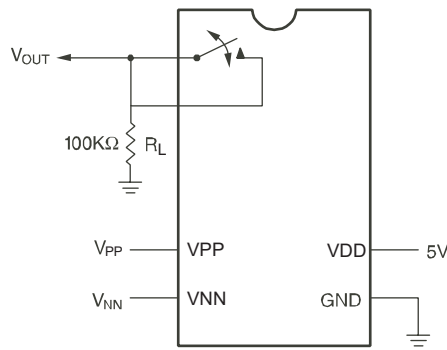
## Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. The switches go to a state retaining their present condition at the rising edge of  $\overline{LE}$ . When  $\overline{LE}$  is low the shift register data flow through the latch.
4.  $D_{OUT}$  is high when data in the shift register 7 is high.
5. Shift register clocking has no effect on the switch states if  $\overline{LE}$  is high.
6. The CLR clear input overrides all other inputs.

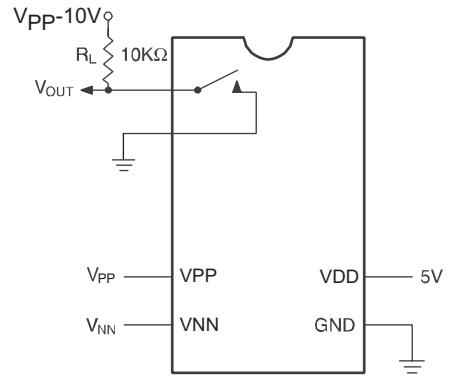
Test Circuits



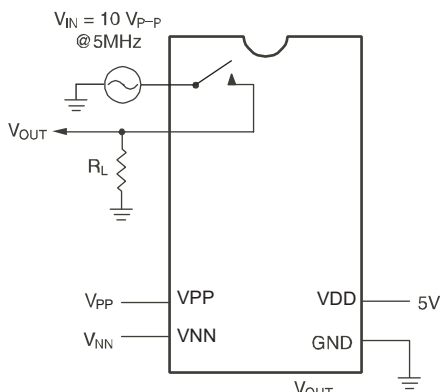
Switch OFF Leakage



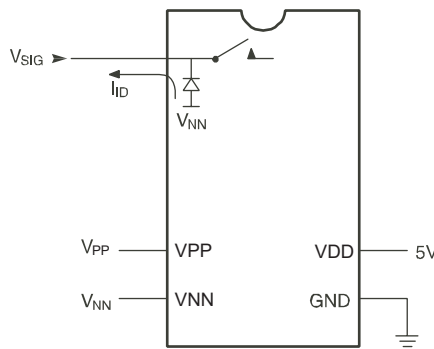
DC Offset ON/OFF



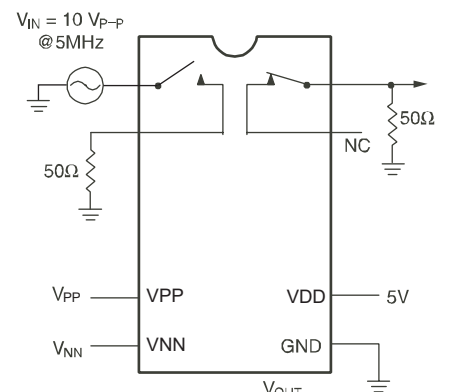
$T_{ON}/T_{OFF}$  Test Circuit



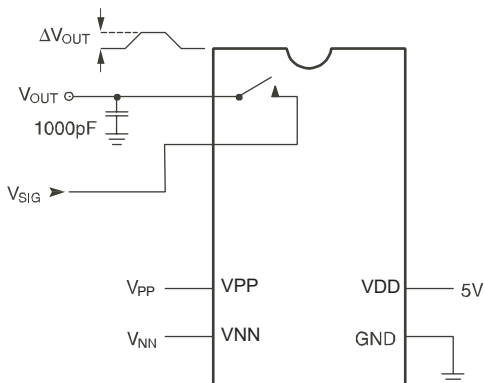
$K_O = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$   
OFF Isolation



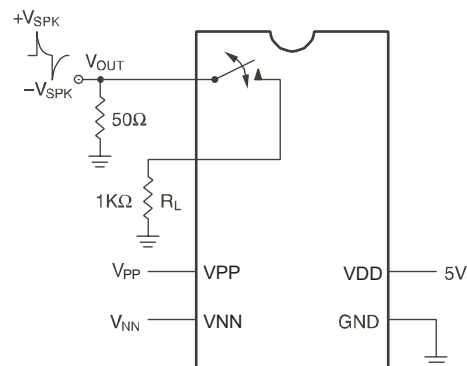
Isolation Diode Current



$K_{CR} = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$   
Crosstalk



$Q = 1000\text{pF} \times \Delta V_{OUT}$   
Charge Injection



Output Voltage Spike

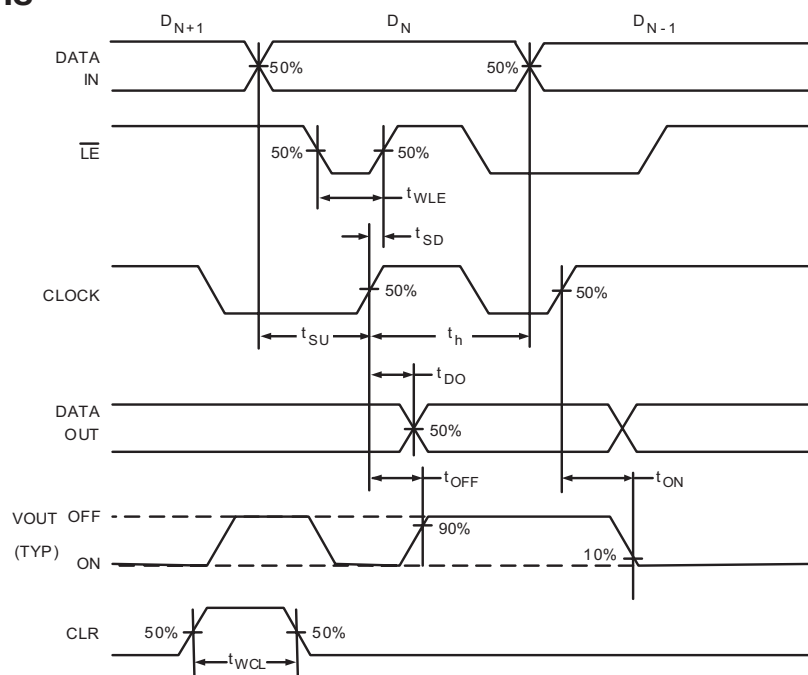
Pin Configuration - 48-Lead LQFP (FG)

Pin #	Pin Name	Pin #	Pin Name
1	SW5	25	VNN
2	NC	26	NC
3	SW4	27	NC
4	NC	28	GND
5	SW4	29	VDD
6	NC	30	NC
7	NC	31	NC
8	SW3	32	NC
9	NC	33	DIN
10	SW3	34	CLK
11	NC	35	$\overline{LE}$
12	SW2	36	CLR
13	NC	37	DOUT
14	SW2	38	NC
15	NC	39	SW7
16	SW1	40	NC
17	NC	41	SW7
18	SW1	42	NC
19	NC	43	SW6
20	SW0	44	NC
21	NC	45	SW6
22	SW0	46	NC
23	NC	47	SW5
24	VPP	48	NC

Pin Configuration - 28-Lead PLCC (PJ)

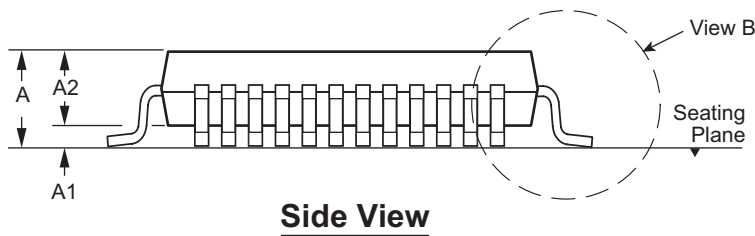
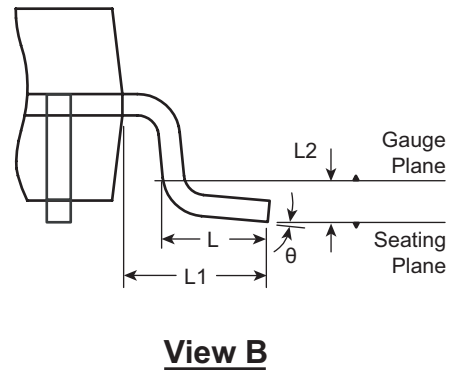
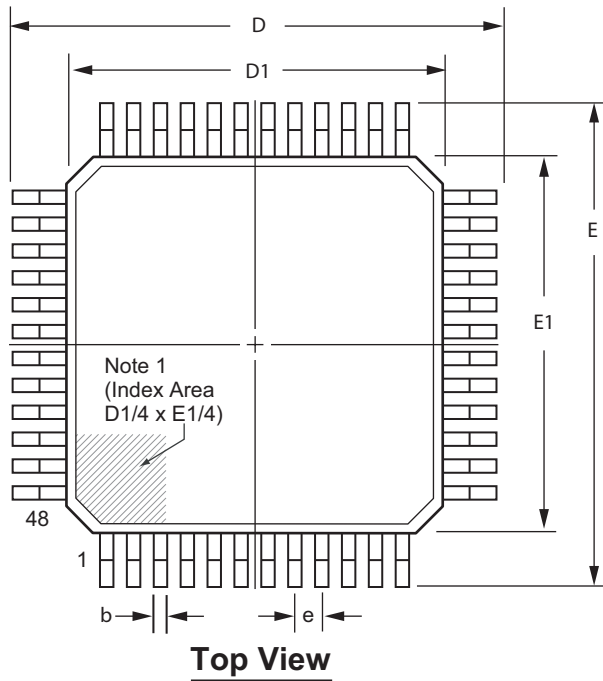
Pin #	Pin Name	Pin #	Pin Name
1	SW3	15	NC
2	SW3	16	DIN
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CLR
6	SW1	20	DOUT
7	SW0	21	SW7
8	SW0	22	SW7
9	NC	23	SW6
10	VPP	24	SW6
11	NC	25	SW5
12	VNN	26	SW5
13	GND	27	SW4
14	VDD	28	SW4

Typical Waveforms



# 48-Lead LQFP Package Outline (FG)

7x7mm body, 1.4mm height (min), 0.50mm pitch



**Note 1:**

A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40	0.05	1.35	0.17	8.80	6.80	8.80	6.80	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20	7.20	9.20	7.20		0.75			7°

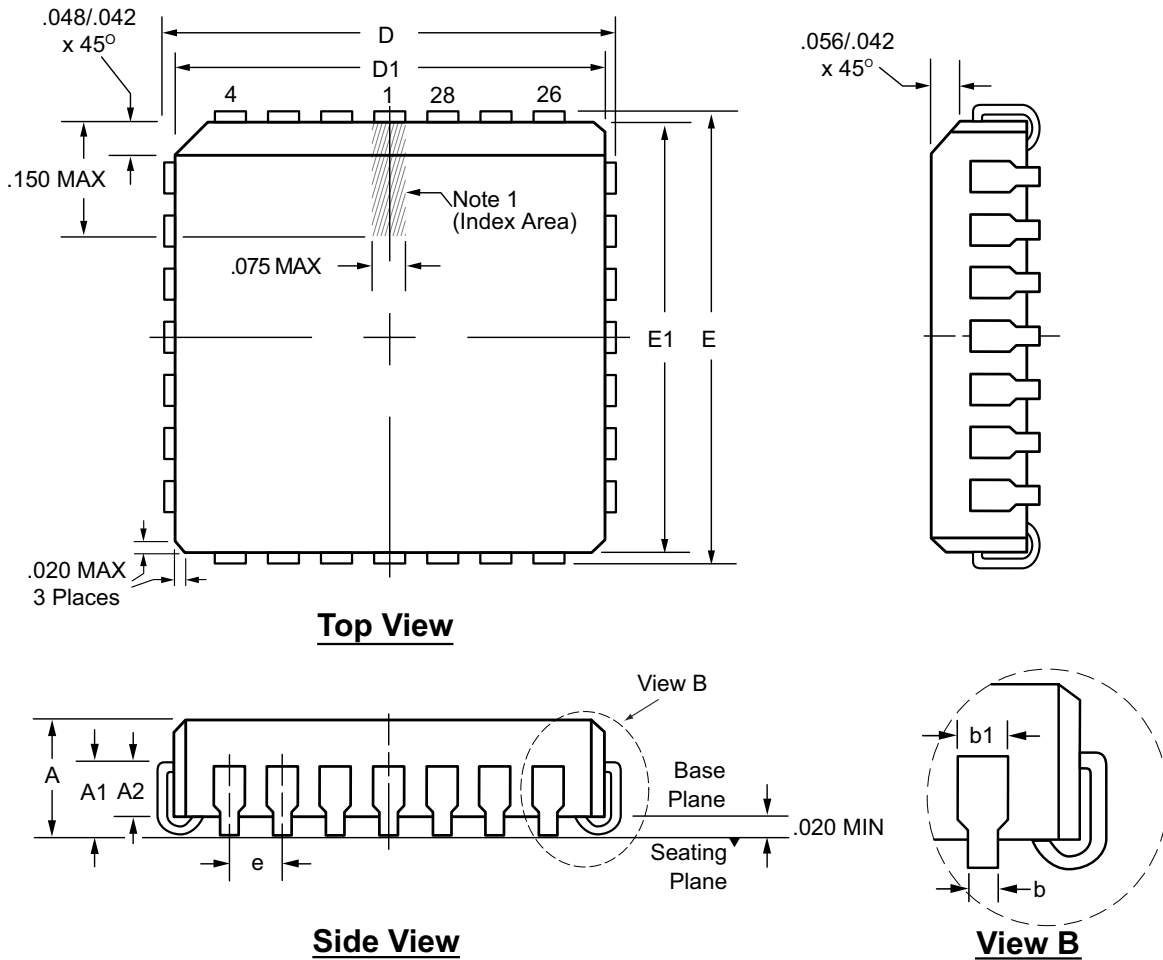
JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

Drawings not to scale.



# 28-Lead PLCC Package Outline (PJ)

.453x.453in body, .180in height (max.), .050in pitch



**Note 1:**

A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.485	.450	.485	.450	.050 BSC
	NOM	.172	.105	-	-	-	.490	.453	.490	.453	
	MAX	.180	.120	.083	.021	.032	.495	.456	.495	.456	

JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.

Drawings not to scale.

(The package drawing (s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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