ASYNCHRONOUS SRAM

64K x 16 x 2 SRAM

+3.3V SUPPLY, TWO CHIP ENABLES
REVOLUTIONARY PINOUT

FEATURES

- Fast access times: 10, 12, and 15ns
- Fast OE# access times: 5, 6, and 7ns
- Single +3.3V ±0.3V power supply
- Fully static -- no clock or timing strobes necessary
- All inputs and outputs are TTL-compatible
- Three state outputs
- Center power and ground pins for greater noise immunity
- Easy memory expansion with CE# and OE# options
- Automatic CE# power down
- High-performance, low-power consumption, CMOS triple-poly, double-metal process
- Packaged in 44-pin, 400-mil TSOP and 44-pin TQFP

OPTIONS	MARKING
• Timing	
10ns access	-10
12ns access	-12
15ns access	-15
• Packages	
44-pin TSOP (400 mil)	TS
44-pin TQFP	T
• Power consumption	
Standard	None
• Temperature	
Commercial	None (0°C to 70°C)

GENERAL DESCRIPTION

The GVT73128S16 is organized as a 65,536 x 16 x 2 SRAM using a four-transistor memory cell with a high performance, silicon gate, low-power CMOS process. Galvantech SRAMs are fabricated using triple-layer polysilicon, double-layer metal technology.

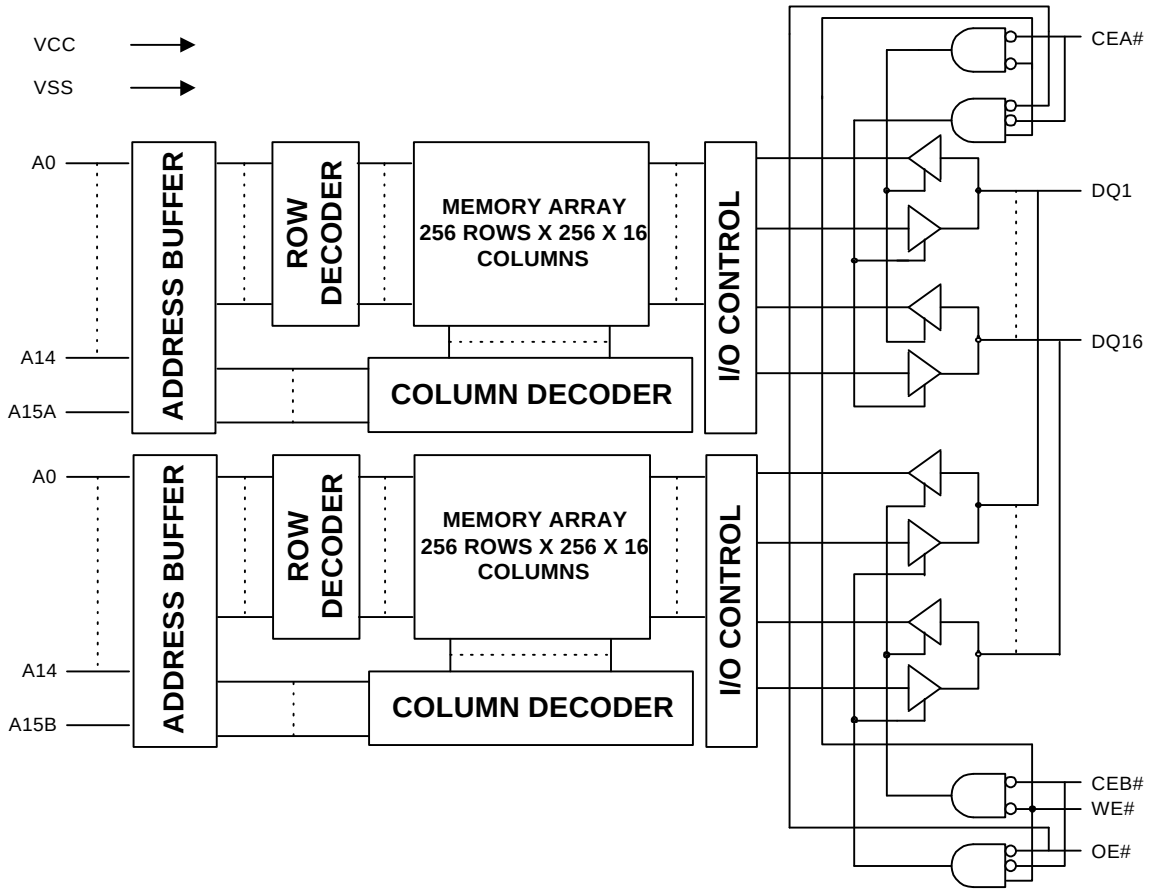
This device consists of two banks of 64K x 16 memory. Each bank of memory has its own chip enable pin and the highest order address. Memory bank A has CEA# and A15A as its chip enable and high order address. Memory bank B has CEB# and A15B as its chip enable and high order address. The other low order addresses (A0 to A14) along with the write enable (WE#) and output enable (OE#) are shared by both memory banks.

This device offers center power and ground pins for improved performance and noise immunity. Static design eliminates the need for external clocks or timing strobes. For increased system flexibility and eliminating bus contention problems, this device offers chip enables (CEA# and CEB#) and output enable (OE#) with this organization.

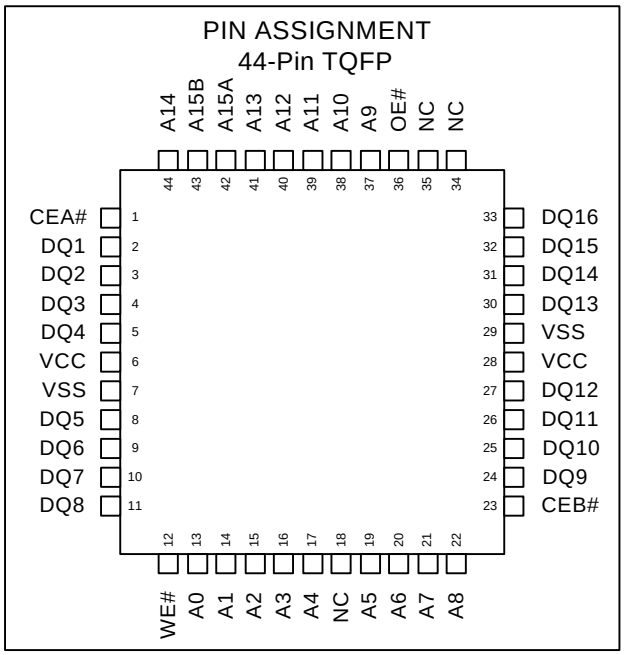
Writing to these devices is accomplished when write enable (WE#) and chip enables (CEA# and/or CEB#) inputs are both LOW. Reading is accomplished when (CEA# or CEB#) and (OE#) go LOW with (WE#) remaining HIGH.

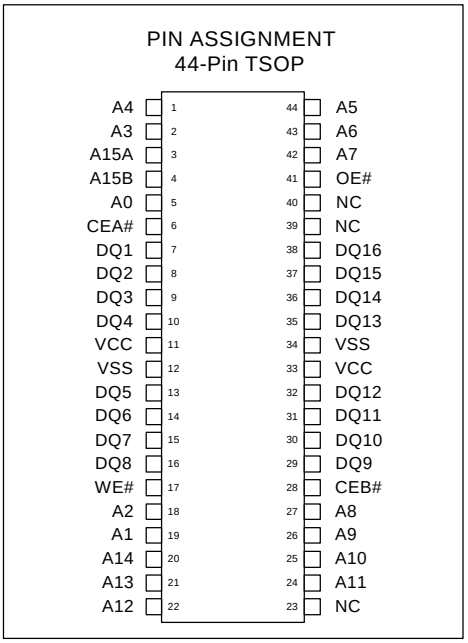
The device offers a low power standby mode when both banks of memory are not selected. This allows system designers to meet low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT





TRUTH TABLE

MODE	CEA#	CEB#	WE#	OE#	DQ1-DQ16	POWER
BANK A MEMORY READ	L	H	H	L	Q	ACTIVE
BANK B MEMORY READ	H	L	H	L	Q	ACTIVE
BANK A MEMORY WRITE	L	H	L	X	D	ACTIVE
BANK B MEMORY WRITE	H	L	L	X	D	ACTIVE
BOTH BANK MEMORY WRITE	L	L	L	X	D	ACTIVE
	L	H	H	H	HIGH-Z	ACTIVE
OUTPUT DISABLE	H	L	H	H	HIGH-Z	ACTIVE
STANDBY	H	H	X	X	HIGH-Z	STANDBY

PIN DESCRIPTIONS

TQFP Pin Numbers	TSOP Pin Numbers	SYMBOL	TYPE	DESCRIPTION
13-17, 19-22, 37-41, 44	5, 19, 18, 2, 1, 44, 43, 42, 27, 26, 25, 24, 22, 21, 20	A0-A14	Input	Low Order Addresses Inputs: These inputs, along with the high order address, determine which cell is addressed
42	3	A15A	Input	High Order Addresses Input: This input, along with A0-A14, determine which cell of bank A memory is addressed
43	4	A15B	Input	High Order Addresses Input: This input, along with A0-A14, determine which cell of bank B memory is addressed
12	17	WE#	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. WE# is LOW for a WRITE cycle and HIGH for a READ cycle.
1	6	CEA#	Input	Bank A Enable: This active LOW input is used to enable bank A of the device. When CEA# is LOW, bank A of the chip is selected. When CEA# is HIGH, bank A of the chip is disabled.
23	28	CEB#	Input	Bank B Enable: This active LOW input is used to enable bank B of the device. When CEB# is LOW, bank B of the chip is selected. When CEB# is HIGH, bank B of the chip is disabled.
36	41	OE#	Input	Output Enable: This active LOW input enables the output drivers.
2, 3, 4, 5, 8, 9, 10, 11, 24,25, 26, 27, 30, 31, 32, 33	7, 8, 9, 10, 13, 14, 15, 16, 29, 30, 31, 32, 35, 36, 37, 38	DQ1-DQ16	Input/Output	SRAM Data I/O: Data inputs and data outputs
6, 28	11, 33	VCC	Supply	Power Supply: 3.3V $\pm$0.3V
7, 29	12, 34	VSS	Supply	Ground
18, 34, 35	23, 39, 40	NC	-	N0 Connect: These signals are not internally connected

ABSOLUTE MAXIMUM RATINGS *

Voltage on VCC Supply Relative to VSS.....-0.5V to +4.6V
V_{IN} .....-0.5V to VCC+1.0V
Storage Temperature (plastic) .....-55°C to +125°
Junction Temperature .....+125°
Power Dissipation 1.0W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITION S

(All Temperature Ranges; VCC = 3.3V ±0.3V unless otherwise noted)

DESCRIPTIO N	CONDITION S	SYMBO L	MIN	MAX	UNIT S	NOTE S
Input High (Logic 1) voltage		V_{IH}	2.2	VCC+0.5	V	1, 2
Input Low (Logic 0) Voltage		V_{II}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-5	5	uA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ VCC	IL_O	-5	5	uA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		VCC	3.0	3.6	V	1

DESCRIPTIO N	CONDITION S	SYM	TYP	POWER	-10	-12	-15	UNITS	NOTES
Power Supply Current: Operating	Device selected; CEA# or CEB# ≤ V_{IL}; VCC =MAX; f=f_{MAX}; outputs open	Icc	70	standard	230	200	170	mA	3, 14
				low	210	180	150		
TTL Standby	CEA# and CEB# ≥ V_{IH}; VCC = MAX; f=f_{MAX}	I_{SB1}	10	standard	35	30	25	mA	14
				low	30	25	20		
CMOS Standby	CEA# and CEB# ≥VCC -0.2; VCC = MAX; all other inputs ≤ VSS +0.2 or ≥VCC -0.2; all inputs static; f= 0	I_{SB2}	0.02	standard	10	10	10	mA	14
				low	1.5	1.5	1.5		

CAPACITANCE

DESCRIPTIO N	CONDITION S	SYMBO L	MAX	UNIT S	NOTE S
Input Capacitance	T_A = 25°C; f = 1 MHz VCC = 3.3V	C_I	6	pF	4
Input/Output Capacitance (DQ)		$C_{I/O}$	8	pF	4

AC ELECTRICAL CHARACTERISTICS

(Note 5) (All Temperature Ranges; VCC = 3.3V ±0.3V)

DESCRIPTIO N		- 10		- 12		- 15			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	10		12		15		ns	
Address access time	^tAA		10		12		15	ns	
Chip Enable access time	^tACE		10		12		15	ns	
Output hold from address change	^tOH	3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		4		4		ns	4, 7
Chip disable to output in High-Z	^tHZCE		5		6		7	ns	4, 6, 7
Output Enable access time	^tAOE		5		6		7	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output Enable to output in High-Z	^tHZOE		5		6		7	ns	4, 6
Chip Enable to power-up time	^tPU	0		0		0		ns	4
Chip disable to power-down time	^tPD		10		12		15	ns	4
WRITE Cycle									
WRITE cycle time	^tWC	10		12		15		ns	
Chip Enable to end of write	^tCW	8		8		9		ns	
Address valid to end of write, with OE# HIGH	^tAW	8		8		9		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP2$	10		10		11		ns	
WRITE pulse width, with OE# HIGH	$^tWP1$	8		8		9		ns	
Data setup time	^tDS	5		6		7		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		4		5		ns	4, 7
Write Enable to output in High-Z	^tHZWE		5		6		7	ns	4, 6, 7

AC TEST CONDITIONS

Input pulse levels	0V to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

OUTPUT LOADS

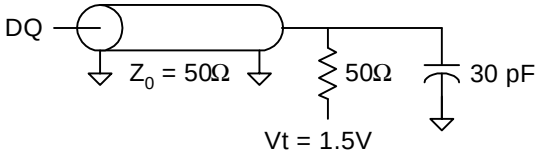


Fig. 1 OUTPUT LOAD EQUIVALENT

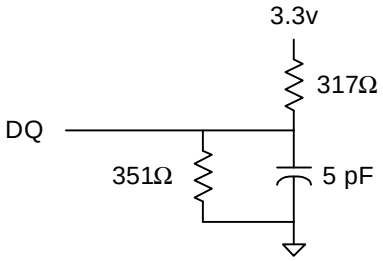
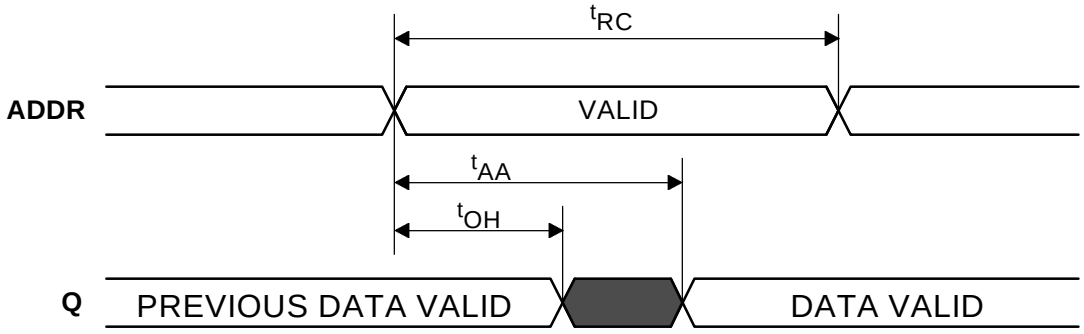


Fig. 2 OUTPUT LOAD EQUIVALENT

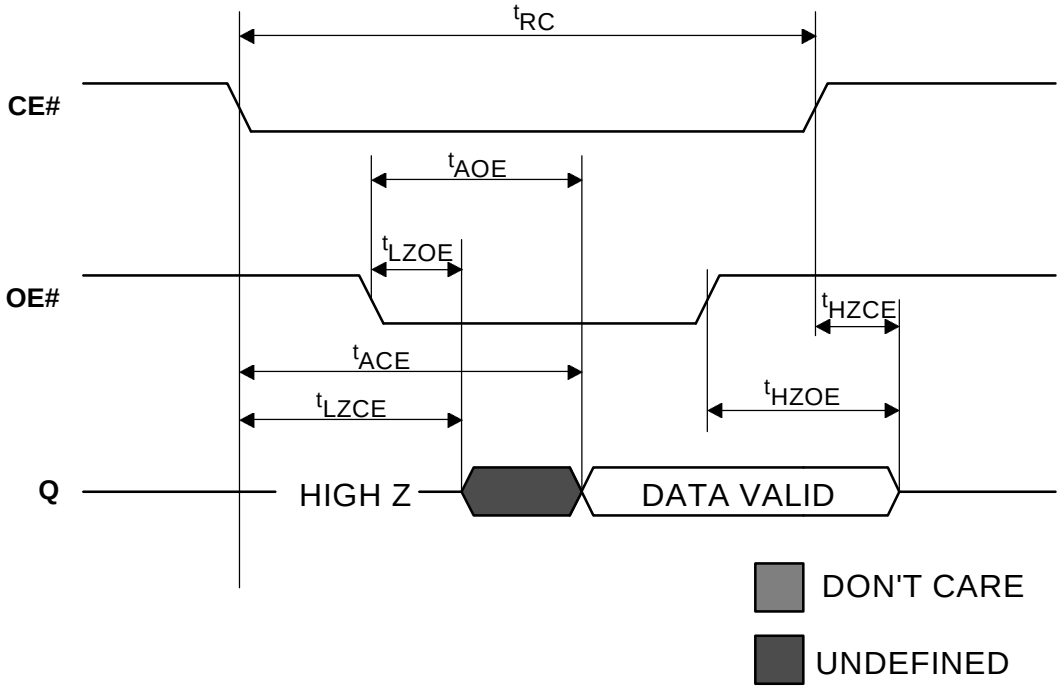
NOTES

1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$.
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tRC/2$
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L=5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. WE# is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. Chip Enable and Write Enable can initiate and terminate a WRITE cycle.
13. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.
14. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

READ CYCLE NO. 1(8, 9)

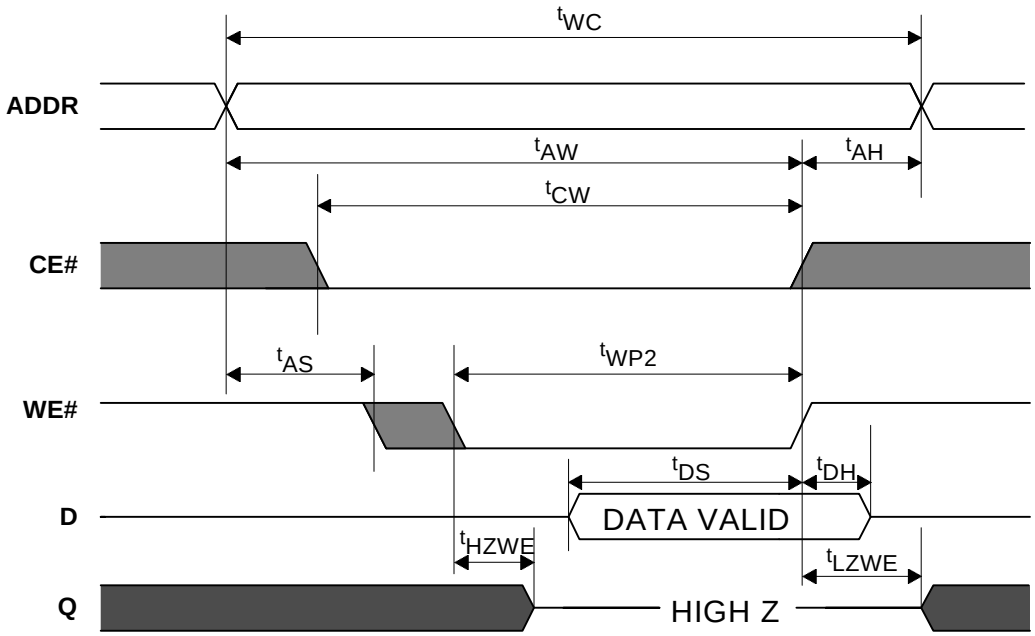


READ CYCLE NO. 2(7, 8, 10, 12)



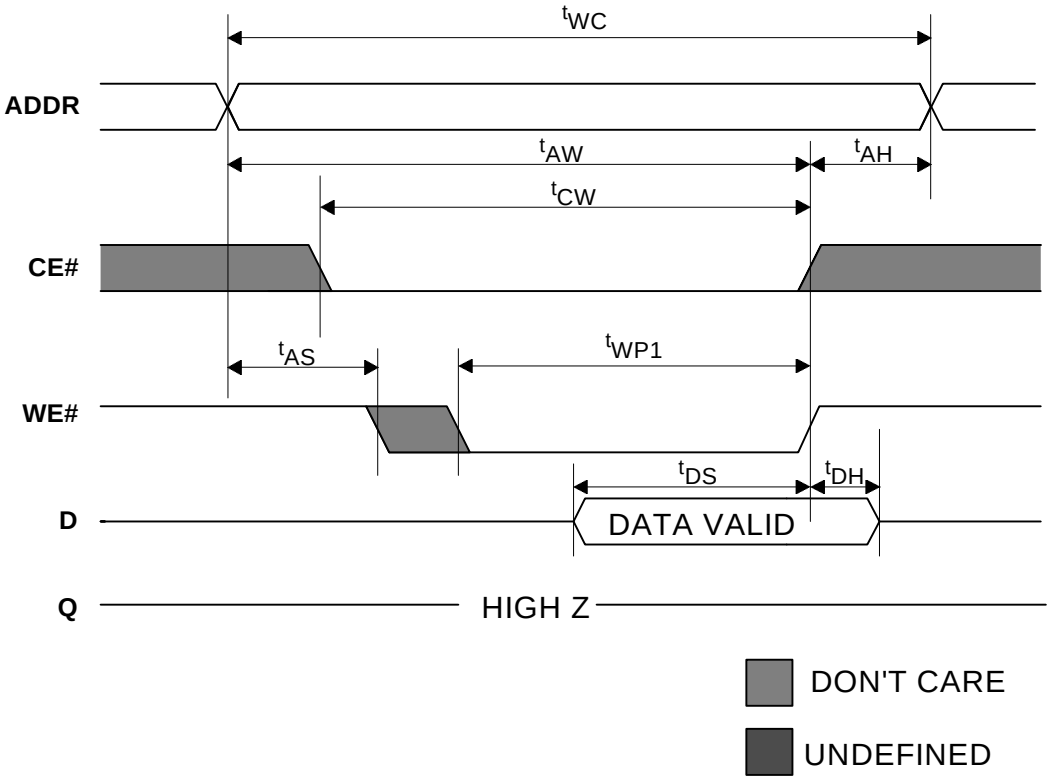
WRITE CYCLE NO. 1(7, 12, 13)

(Write Enable Controlled with Output Enable OE# active LOW)

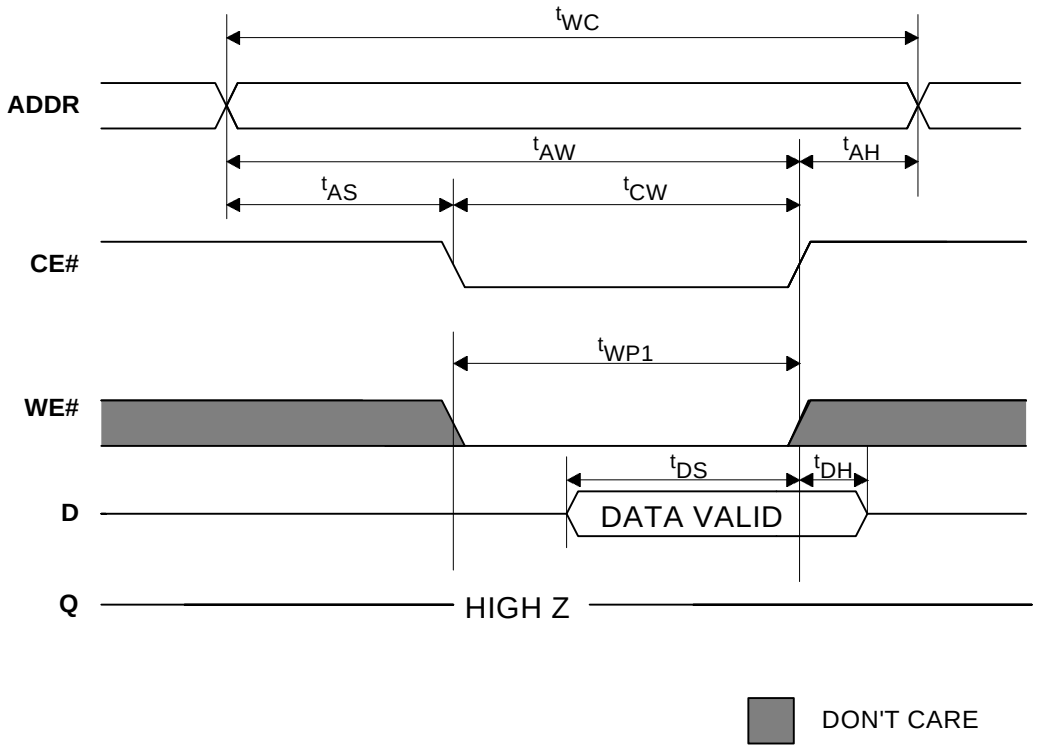


WRITE CYCLE NO. 2(12, 13)

(Write Enable Controlled with Output Enable OE# inactive HIGH)



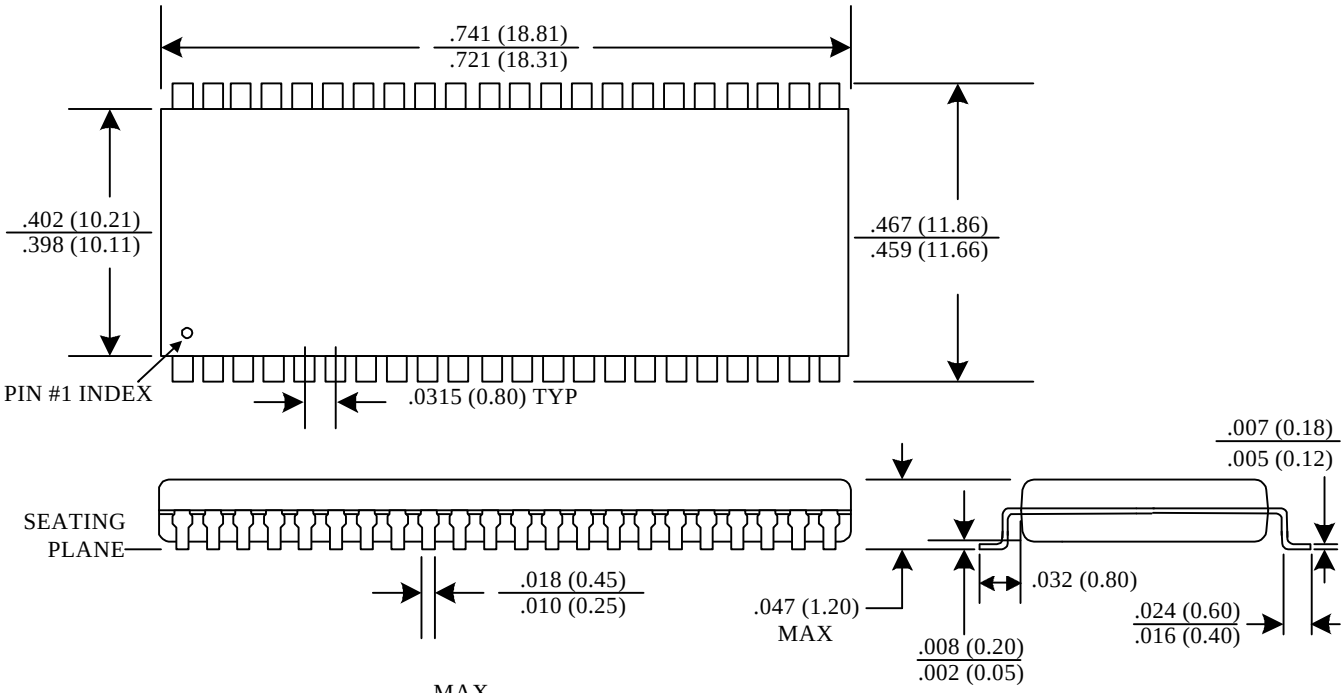
WRITE CYCLE NO. 3(12, 13)
(Chip Enable Controlled)



Note: CE# goes to LOW means CEA# or CEB# goes to LOW, namely, CE#=CEA#*CEB#

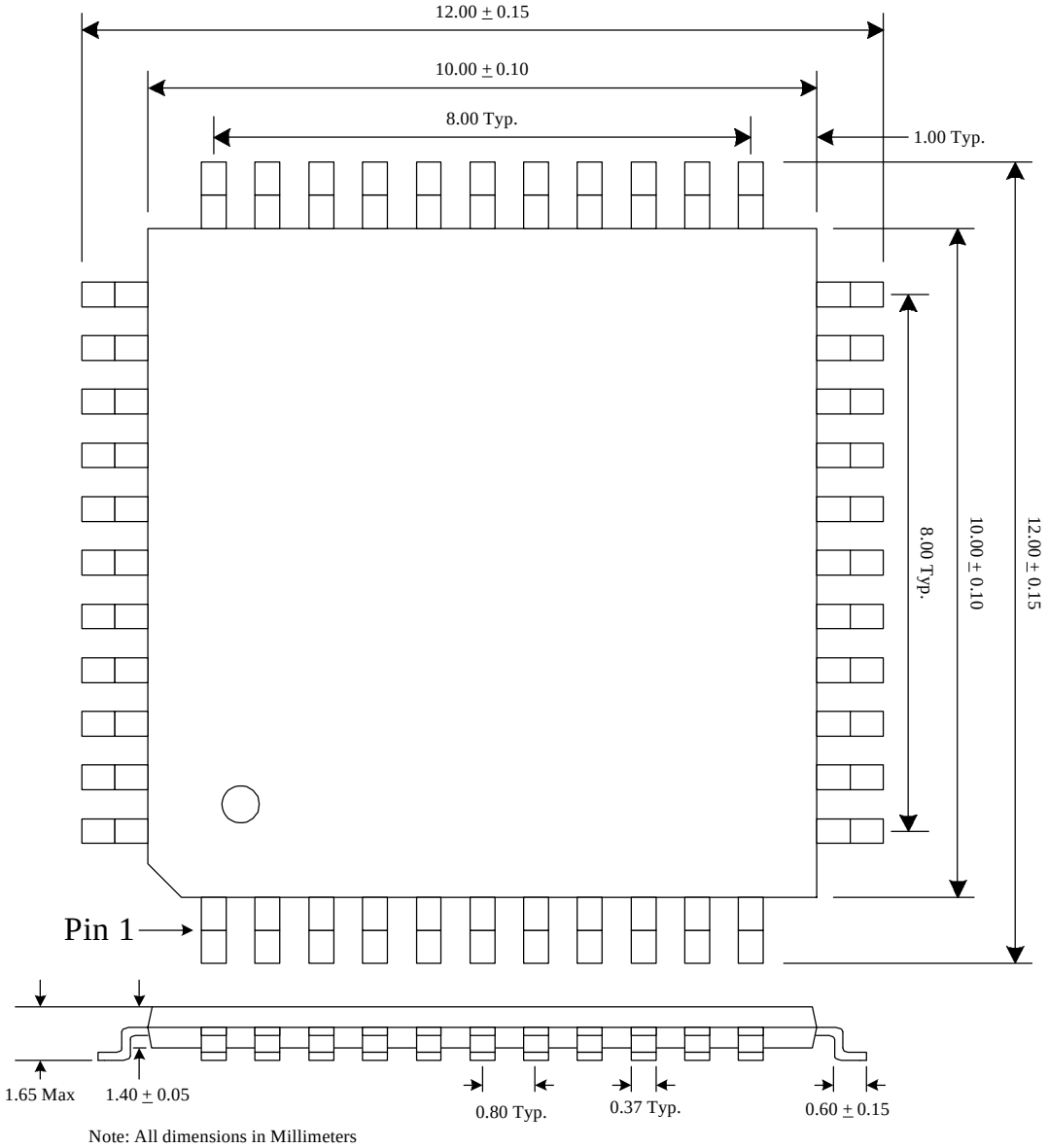
Package Dimensions

44-pin 400 Mil Plastic TSOP (TS)



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical, max where noted.

44-Pin TQFP Package Dimension s



Note: All dimensions in Millimeters

Ordering Information

GVT 73128S16 XX - XX X X

- Galvantech Prefix
- Part Number
- Temperature (Blank = Commercial)
- Power (Blank= Standard)
- Speed (10=10ns, 12=12ns, 15= 15ns)
- Package (T = 44 PIN TQFP, TS = TSOP TYPE II)