

4 Signals and DC Characteristics

4.1 Terminology

The abbreviations used in this chapter are defined below.

2S	Two-state output
3S	Tristate output
B	Bidirectional
I	Input
O	Output
OD	Open Drain
TTL	Input with TTL threshold
TTL PD	Input with TTL threshold (pull-down resistor)
TTL Sch.	TTL Schmitt trigger input

Table 4.1 DC Electrical Characteristics Non-PCI signals ($V_{DD} = 5\text{ V} \pm 5\%$)^a

Symbol	Parameter	Signal Type	Test Conditions	Tested at -40°C to 85°C	
				Min	Max
V_{IH}	Input high voltage	TTL	$V_{OUT} = 0.1\text{ V}$ or $V_{DD} - 0.1\text{ V}$; $[I_{OUT}] = 20\text{ }\mu\text{A}$	2.2V	$V_{DD} + 0.3\text{ V}$
V_{IL}	Max. low-level input	TTL	$V_{OUT} = 0.1\text{ V}$ or $V_{DD} - 0.1\text{ V}$; $[I_{OUT}] = 20\text{ }\mu\text{A}$	-0.3 V	0.8V
V_{T+}	Positive going Schmitt trigger voltage	TTL Sch	$V_{OUT} = 0.1\text{ V}$ or $V_{DD} - 0.1\text{ V}$; $[I_{OUT}] = 20\text{ }\mu\text{A}$	—	2.4 V
V_{T-}	Negative going Schmitt trigger voltage	TTL Sch	$V_{OUT} = 0.1\text{ V}$ or $V_{DD} - 0.1\text{ V}$; $[I_{OUT}] = 20\text{ }\mu\text{A}$	0.8 V	—
$V_{Hysteresis}$	Schmitt trigger hysteresis voltage	TTL Sch	V_{T+} to V_{T-}	$0.05V_{DD}$	—
I_{IN}	Maximum input leakage current	TTL	With no pull-up resistor ($V_{IN} = V_{SS}$ or V_{DD})	-5.0 μA	5.0 μA
		TTL PD	With no pull-down ($V_{IN} = V_{DD}$)	10 μA	200 μA
I_{OZ}	Maximum output leakage current	TS	($V_{OUT} = V_{SS}$ or V_{DD})	-10.0 μA	10.0 μA
		OD	($V_{OUT} = V_{DD}$)	-10.0 μA	10.0 μA
C_{IN}	Maximum input capacitance	TTL TTL PD TTL Sch		—	10.0 pF

a. V_{OL} Max and V_{OH} Min for non-PCI signals are listed as a footnote to Table 4.4 below.

Table 4.2 DC Electrical Characteristics PCI signals ($V_{DD} = 5\text{ V} \pm 5\%$)

Symbol	Parameter	Test Conditions	Tested at -40°C to 85°C	
			Min	Max
V_{IH}	Input high voltage	$V_{OUT} = 0.1\text{ V or } V_{DD} - 0.1\text{ V}; [I_{OUT}] = 20\text{ }\mu\text{A}$	2.0V	$V_{DD} + 0.5\text{ V}$
V_{IL}	Max. low-level input	$V_{OUT} = 0.1\text{ V or } V_{DD} - 0.1\text{ V}; [I_{OUT}] = 20\text{ }\mu\text{A}$	-0.5 V	0.8V
I_{IH}	Input high leakage current	$V_{IN} = 2.7\text{ V}$	-	70 μA
I_{IL}	Input low leakage current	$V_{IN} = 0.5\text{ V}$	-	-70 μA
V_{OH}	Output high voltage	$I_{OUT} = -2\text{ mA}$	2.4V	-
V_{OL}	Output low voltage	$I_{OUT} = 6\text{ mA}$	-	0.55V

Table 4.3 AC Electrical Characteristics PCI signals ($V_{DD} = 5\text{ V} \pm 5\%$)

Symbol	Parameter	Test Conditions	Tested at -40°C to 85°C	
			Min	Max
$V_{OH\ min}$	Output high voltage min	$I_{OUT} = -44\text{mA}$	1.4V	-
$V_{OH\ max}$	Output high voltage max	$I_{OUT} = -142\text{mA}$	-	3.1V
$V_{OL\ min}$	Output low voltage min	$I_{OUT} = 95\text{mA}$	0.71	-
$V_{OL\ max}$	Output low voltage max	$I_{OUT} = 206\text{mA}$	-	2.2

Table 4.4 Pin List for QSpan Signals

Pin Name	Pin Number 208-pin PQFP	Type	Input Type	Output Type	I_{OH}^n (mA)	I_{OL}^n (mA)	Interface	Signal Description
A[31:0]	See Table 4.6	B	TTL	3S	12	-12	QBus	Address lines
AD[31:0]	See Table 4.5	B	TTL	3S	-	-	PCI	Address/data lines
AS	126	B	TTL Sch.	3S	12	-12	QBus	Address strobe
BB/BGACK	33	B	TTL Sch.	3S	12	-12	QBus	Bus busy/Bus grant acknowledge
BM_EN/ FIFO_RDY	57	B	TTL Sch.	3S	-6mA	6mA	QBus	Bus master enable/FIFO ready
BDIP	127	I	TTL	-	-	-	QBus	Burst data in progress (And QSpan master mode)
BERR/TEA	125	B	TTL Sch.	3S	12	-12	QBus	Bus error/ Transfer error acknowledge
BG	128	I	TTL	-	-	-	QBus	Bus grant
BGACK	See BB/BGACK above							
BR	34	O	-	*2S	6	-6	QBus	Bus request
BURST/TIP	31	B	TTL	3S	12	-12	QBus	Burst/transaction in progress
C/BE[0]	100	B	TTL	3S	-	-	PCI	Command and byte enable
C/BE[1]	87							
C/BE[2]	75							
C/BE[3]	62							
CSPCI	118	I	TTL	-	-	-	QBus	PCI chip select
CSREG	117	I	TTL	-	-	-	QBus	QSpan register chip select
D[31:0]	See Table 4.7	B	TTL	3S	12	-12	QBus	Data lines
DACK/ SDACK	132	I	TTL	-	-	-	QBus	IDMA acknowledge
DEVSEL#	81	B	TTL	3S	-	-	PCI	Device select
DONE	133	I	TTL	-	-	-	QBus	IDMA done
DREQ	135	O	-	*2S	6	-6	QBus	IDMA request
DSACK0	19	B	TTL Sch.	3S	12	-12	QBus	Data and size acknowledge 0
DSACK1/TA	18	B	TTL Sch.	3S	12	-12	QBus	Data and size acknowledge 1/ transfer acknowledge
DS	177	O	-	3S	12	-12	QBus	Data strobe

* All outputs except for SCI are tristated when TMODE is 11 (See Table 2.46 on page 2.71.)

Table 4.4 Pin List for QSpan Signals

Pin Name	Pin Number 208-pin PQFP	Type	Input Type	Output Type	I_{OL}^{*1} (mA)	I_{OH}^{*2} (mA)	Interface	Signal Description
ENID	129	I	-	-	-	-		FOR FACTORY TESTING
FRAME#	76	B	TTL	3S	-	-	PCI	Cycle frame
GNT#	45	I	TTL	-	-	-	PCI	Grant
HALT/ TRETRY	44	B	TTL	3S	12	-12	QBus	Halt/tretry
IDSEL	101	I	TTL	-	-	-	PCI	Initialization device select
IMSEL	24	I	TTL	-	-	-	QBus	Slave image select
INT#	136	O	-	OD	24	-24	PCI	Interrupt
IRDY#	79	B	TTL	3S	-	-	PCI	Initiator ready
PAR	85	B	TTL	3S	-	-	PCI	Parity
PCLK	48	I	TTL	-	-	-	PCI	PCI clock
PERR#	84	B	TTL	3S	-	-	PCI	Parity error
-	57	-	-	-	-	-		No connect
QCLK	153	I	TTL	-	-	-	QBus	QBus clock
QINT	134	O	-	OD	6	-6	QBus	Interrupt
REQ#	35	O	-	3S	-	-	PCI	Request
RESETI	29	I	TTL Sch.	-	-	-	QBus	Reset input
RESETO	30	O	-	OD	6	-6	QBus	Reset output
RETRY	See HALT/TRETRY above							
RST#	46	I	TTL Sch.	-	-	-	PCI	Reset
R/W	17	B	TTL	3S	12	-12	QBus	Read/write
SCL	23	O	-	*2S	6	-6	EEPROM	Serial clock
SDA	22	B	TTL	OD	6	-6	EEPROM	Serial data
SDACK	See DACK/SDACK above							
SERR#	137	O	-	OD	24	-24	PCI	System error
SIZ[0]	21	B	TTL	3S	12	-12	QBus	Size
SIZ[1]	20						QBus	Size
STOP#	83	B	TTL	3S	-	-	PCI	Stop
TA	See DSACKI/TA above							
* All outputs except for SCL are tristated when TMODE is 11 (See Table 2.46 on page 2-71.)								

Table 4.4 Pin List for QSpan Signals

Pin Name	Pin Number 208-pin PQFP	Type	Input Type	Output Type	I_{OL}^a (mA)	I_{OH}^b (mA)	Interface	Signal Description
TC[0]	121	B	TTL	3S	12	-12	QBus	Transaction code
TC[1]	122							
TC[2]	123							
TC[3]	124							
TFA	See BERR/TEA above							
TIP	See BURST/TIP above							
TMODE[0]	28	I	TTL	-	-	-		Test mode
TMODE[1]	27							
TRDY#	80	B	TTL	3S	-	-	PCI	Target ready
TS	32	B	TTL Sch.	TS	12	-12	QBus	Transfer start

* All outputs except for SCL are tristated when TMODE is '1' (See Table 2.46 on page 2-71.)

* All outputs except for SCL are tristated when TMODE is 11 (See Table 2.46 on page 2-71.)

a. V_{OL} Max = 0.4 Volts for non-PCI signals.

b. V_{OH} Min = 0.8VDD for non-PCI signals.

Table 4.5 PCI Bus Address/Data Pins

Signal	PQFP	Signal	PQFP
AD0	116	AD16	74
AD1	115	AD17	72
AD2	113	AD18	71
AD3	112	AD19	70
AD4	111	AD20	67
AD5	109	AD21	66
AD6	108	AD22	65
AD7	107	AD23	63
AD8	99	AD24	61
AD9	97	AD25	59
AD10	96	AD26	58
AD11	95	AD27	43
AD12	93	AD28	42
AD13	92	AD29	40
AD14	91	AD30	39
AD15	88	AD31	38

Table 4.6 QBus Address Pins

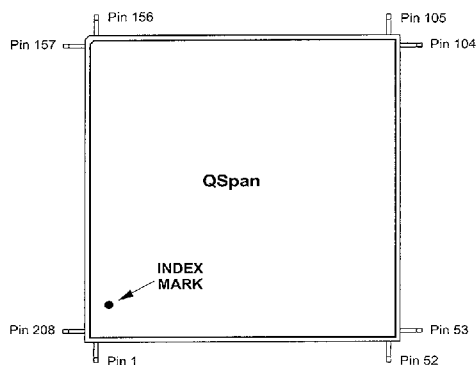
Signal	PQFP	Signal	PQFP
A0	138	A16	188
A1	139	A17	189
A2	142	A18	190
A3	143	A19	191
A4	144	A20	194
A5	145	A21	195
A6	165	A22	196
A7	166	A23	197
A8	167	A24	198
A9	168	A25	199
A10	169	A26	9
A11	170	A27	10
A12	173	A28	11
A13	174	A29	12
A14	175	A30	13
A15	176	A31	14

Table 4.7 QBus Data Pins

Signal	PQFP	Signal	PQFP
D0	146	D16	184
D1	147	D17	185
D2	148	D18	186
D3	149	D19	187
D4	150	D20	200
D5	151	D21	201
D6	159	D22	202
D7	160	D23	203
D8	161	D24	204
D9	162	D25	205
D10	163	D26	3
D11	164	D27	4
D12	178	D28	5
D13	179	D29	6
D14	180	D30	7
D15	181	D31	8

Table 4.8 Pin Assignments for Power and Ground

Power = V_{DD}			Ground = V_{SS}			
2	102	192	1	64	110	208
15	103	206	16	68	114	
26	106	207	25	73	120	
36	119		37	77	131	
50	130		41	82	141	
51	140		47	86	152	
54	154		49	89	156	
56	155		52	94	157	
69	158		53	98	172	
78	171		55	104	183	
90	182		60	105	193	



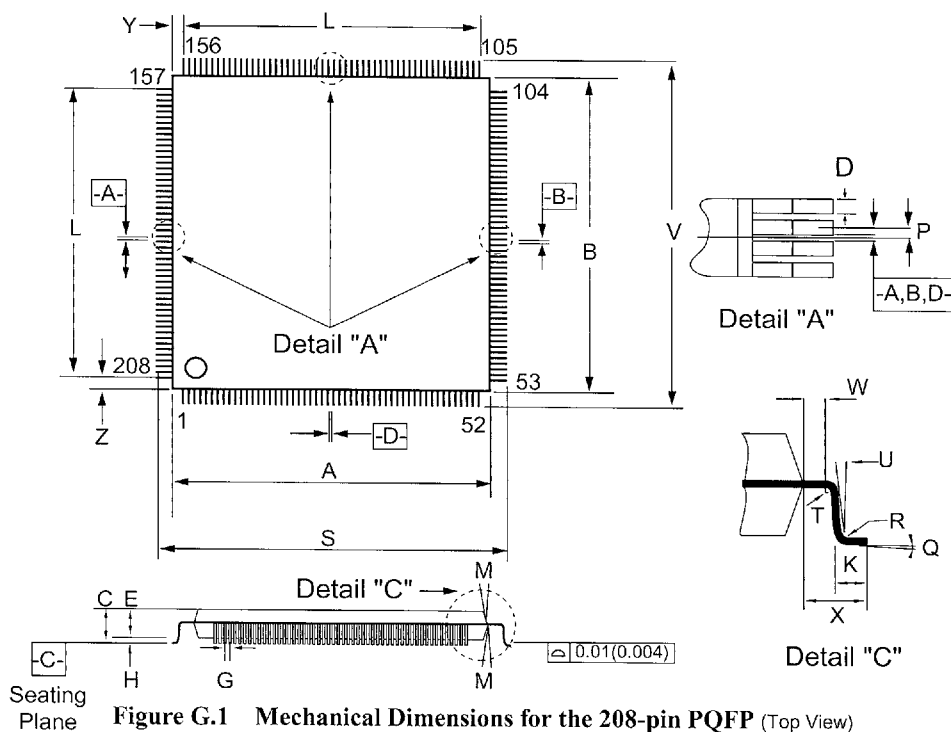
(Top View)

1. VSS	31. $\overline{\text{BURST}}/\overline{\text{TIP}}$	60. VSS	90. VDD	120. VSS	150. D[4]	180. D[14]
2. VDD	32. $\overline{\text{TS}}$	61. AD[24]	91. AD[14]	121. TC[0]	151. D[5]	181. D[15]
3. D[26]	33. $\overline{\text{BB}}/\overline{\text{BGACK}}$	62. C/BE[3]	92. AD[13]	122. TC[1]	152. VSS	182. VDD
4. D[27]	34. $\overline{\text{BR}}$	63. AD[23]	93. AD[12]	123. TC[2]	153. QCLK	183. VSS
5. D[28]	35. REQ#	64. VSS	94. VSS	124. TC[3]	154. VDD	184. D[16]
6. D[29]	36. VDD	65. AD[22]	95. AD[11]	125. $\overline{\text{BERR}}/\overline{\text{TEA}}$	155. VDD	185. D[17]
7. D[30]	37. VSS	66. AD[21]	96. AD[10]	126. $\overline{\text{AS}}$	156. VSS	186. D[18]
8. D[31]	38. AD[31]	67. AD[20]	97. AD[9]	127. $\overline{\text{BDIP}}$	157. VSS	187. D[19]
9. A[26]	39. AD[30]	68. VSS	98. VSS	128. $\overline{\text{BG}}$	158. VDD	188. A[16]
10. A[27]	40. AD[29]	69. VDD	99. AD[8]	129. ENID	159. D[6]	189. A[17]
11. A[28]	41. VSS	70. AD[19]	100. C/BE[0]	130. VDD	160. D[7]	190. A[18]
12. A[29]	42. AD[28]	71. AD[18]	101. IDSEL	131. VSS	161. D[8]	191. A[19]
13. A[30]	43. AD[27]	72. AD[17]	102. VDD	132. $\overline{\text{DACK}}/\overline{\text{SDACK}}$	162. D[9]	192. VDD
14. A[31]	44. $\overline{\text{HALT}}/\overline{\text{TRETRY}}$	73. VSS	103. VDD	133. DONE	163. D[10]	193. VSS
15. VDD	45. GNT#	74. AD[16]	104. VSS	134. $\overline{\text{QINT}}$	164. D[11]	194. A[20]
16. VSS	46. RST#	75. C/BE[2]	105. VSS	135. $\overline{\text{DREQ}}$	165. A[6]	195. A[21]
17. R/ $\overline{\text{W}}$	47. VSS	76. FRAME#	106. VDD	136. INT#	166. A[7]	196. A[22]
18. $\overline{\text{DSACKI}}/\overline{\text{TA}}$	48. PCLK	77. VSS	107. AD[7]	137. SERR#	167. A[8]	197. A[23]
19. $\overline{\text{DSACKO}}$	49. VSS	78. VDD	108. AD[6]	138. A[0]	168. A[9]	198. A[24]
20. SI[1]	50. VDD	79. IRDY#	109. AD[5]	139. A[1]	169. A[10]	199. A[25]
21. SI[0]	51. VDD	80. TRDY#	110. VSS	140. VDD	170. A[11]	200. D[20]
22. SDA	52. VSS	81. DEVSEL#	111. AD[4]	141. VSS	171. VDD	201. D[21]
23. SCL	53. VSS	82. VSS	112. AD[3]	142. A[2]	172. VSS	202. D[22]
24. IMSEL	54. VDD	83. STOP#	113. AD[2]	143. A[3]	173. A[12]	203. D[23]
25. VSS	55. VSS	84. PERR#	114. VSS	144. A[4]	174. A[13]	204. D[24]
26. VDD	56. VDD	85. PAR	115. AD[1]	145. A[5]	175. A[14]	205. D[25]
27. TMODE[1]	57. $\overline{\text{BM}}_{\text{EN}}/\overline{\text{FIFO}}_{\text{RDY}}$	86. VSS	116. AD[0]	146. D[0]	176. A[15]	206. VDD
28. TMODE[0]	58. AD[26]	87. C/BE[1]	117. $\overline{\text{CSREG}}$	147. D[1]	177. $\overline{\text{DS}}$	207. VDD
29. RESETT	59. AD[25]	88. AD[15]	118. $\overline{\text{CSPCI}}$	148. D[2]	178. D[12]	208. VSS
30. RESETO		89. VSS	119. VDD	149. D[3]		

Table 4.9 Pin-Out of QSpan 208-Pin PQFP

Appendix G Mechanical and Ordering Information

G.1 Mechanical Information



DIMENSION	208 PQFP	
	Min.	Max.
A	27.90	28.10
B	27.90	28.10
C	3.45	4.10
D	0.17	0.27
E	3.20	3.60
G	0.500 BSC	
H	0.25	0.35
K	0.75	0.95

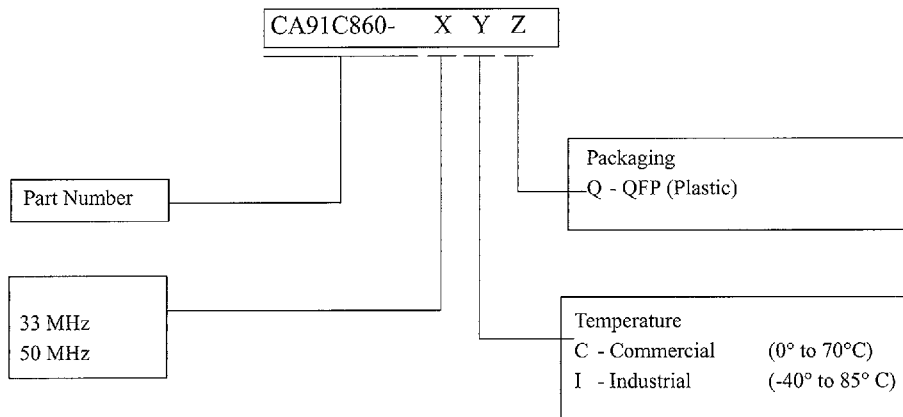
DIMENSION	208 PQFP	
	Min.	Max.
L	25.5 REF	
M	5°	16°
P	0.250 BSC	
Q	0°	7°
R	0.13	0.25
S	31.00	31.40
T	0.13	—
U	0°	—

DIMENSION	208 PQFP	
	Min.	Max.
V	31.00	31.40
W	0.20	—
X	1.60 REF	
Y	1.25 REF	
Z	1.25 REF	

Controlling dimensions in millimeters

G.2 Ordering Information

Tundra products are designated by a Product Code. When ordering, refer to products by their full code. For detailed mechanical drawings or alternative packaging requirements, please contact our factory directly



Tundra products are designated by a Product Code. When ordering, refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact our factory directly.

Table G.1 Product Code Details

Valid Suffixes			Meaning			
X	Y	Z	Temperature	QUICC	PowerQUICC	M68040
33	C	Q	0° to 70°C	25 MHz	40 MHz	40 MHz
50	C	Q	0° to 70°C	33 MHz	40 MHz	40 MHz ^a
33	I	Q	-40° to 85° C	25 MHz	40 MHz	N/A

a. The QSpan is compatible with all M68040 variants in large buffer mode up to 40MHz. The QSpan is compatible with all M68040 variants in small buffer mode up to 33MHz.