N-channel enhancement mode vertical D-MOS transistor

BSP106

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage	–	60	V
I_D	drain current	DC value	425	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	4	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	3	V

PIN CONFIGURATION

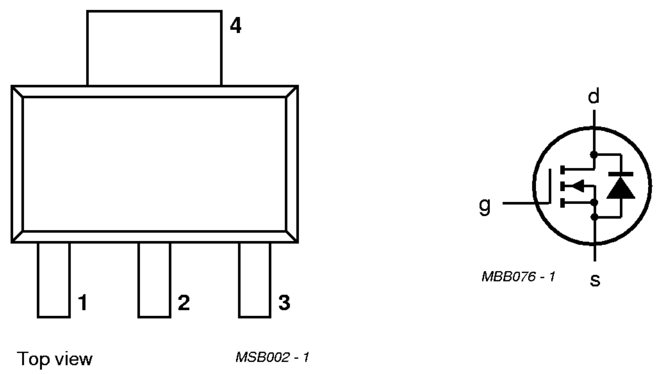


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
I_D	drain current	DC value	–	425	mA
I_{DM}	drain current	peak value	–	850	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
		V_{DS} = 25 V V_{GS} = 0	–	–	0.5	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	–	2.5	4	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10	–	10	15	ns

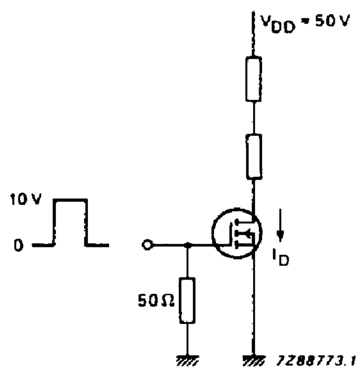


Fig.2 Switching time test circuit.

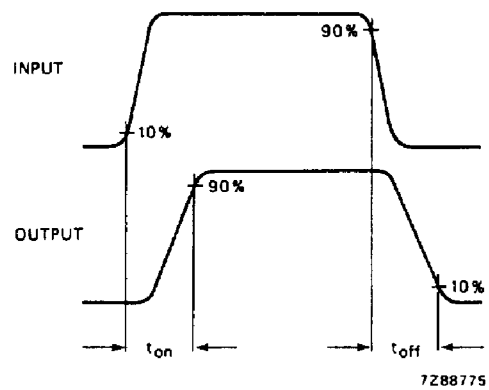


Fig.3 Input and output waveforms.

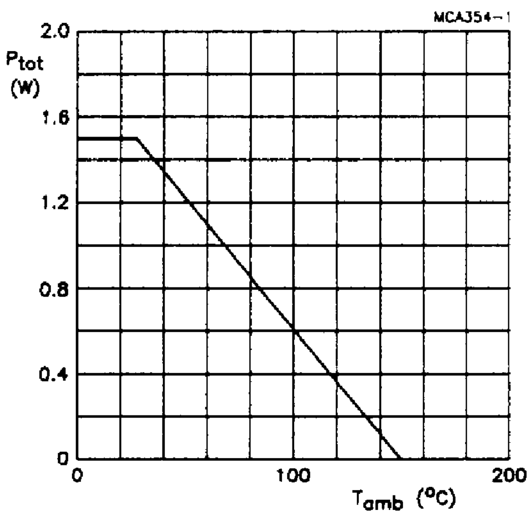


Fig.4 Power derating curve.

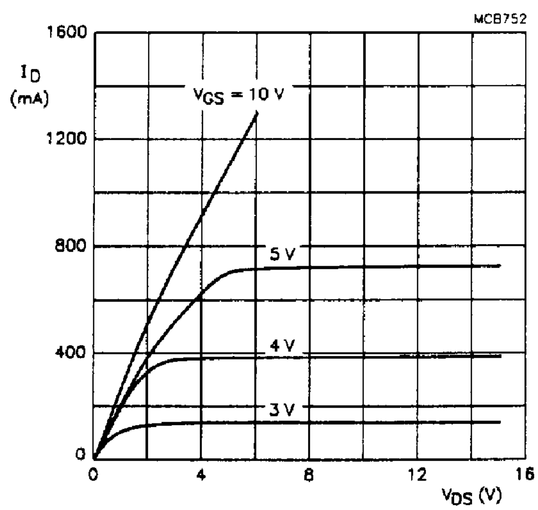


Fig.5 Typical output characteristics; T_j = 25 °C.

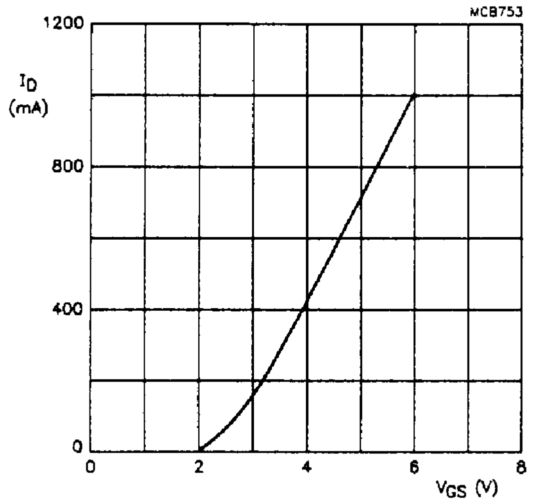


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

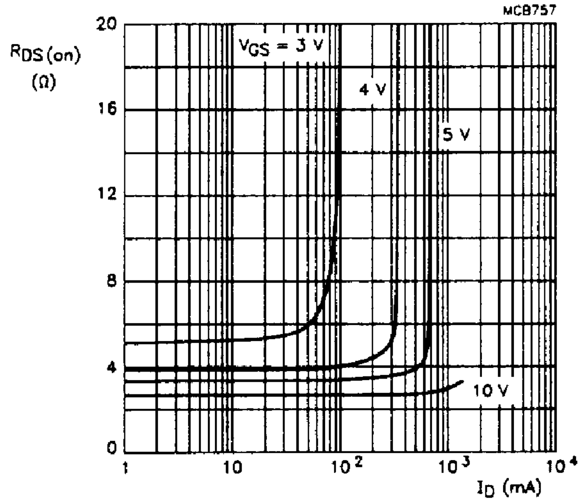


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

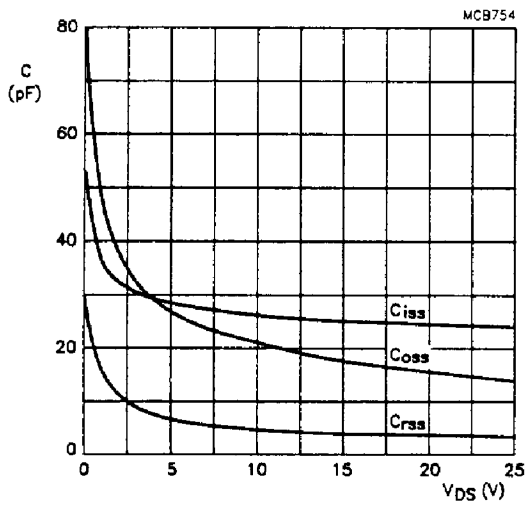


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

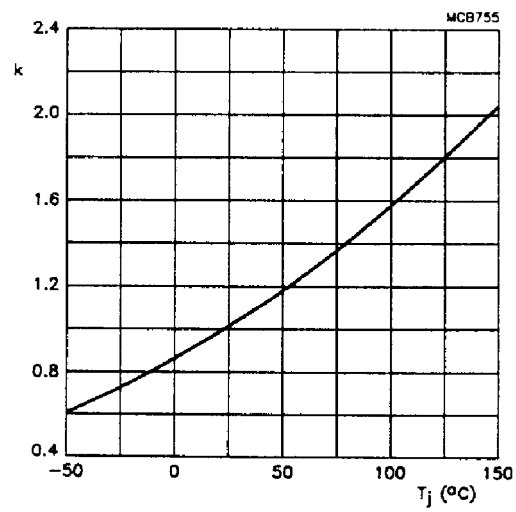


Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at 200 mA/10 V.

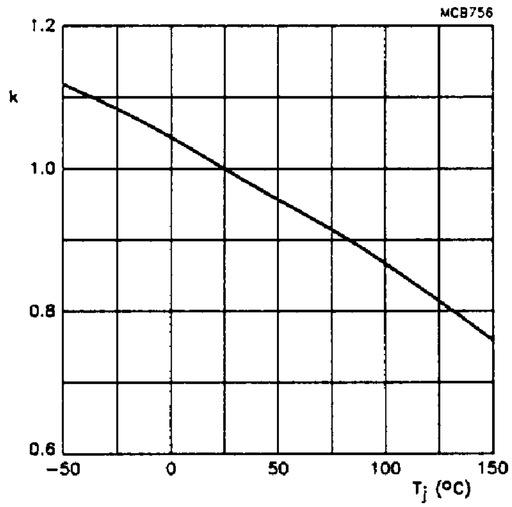


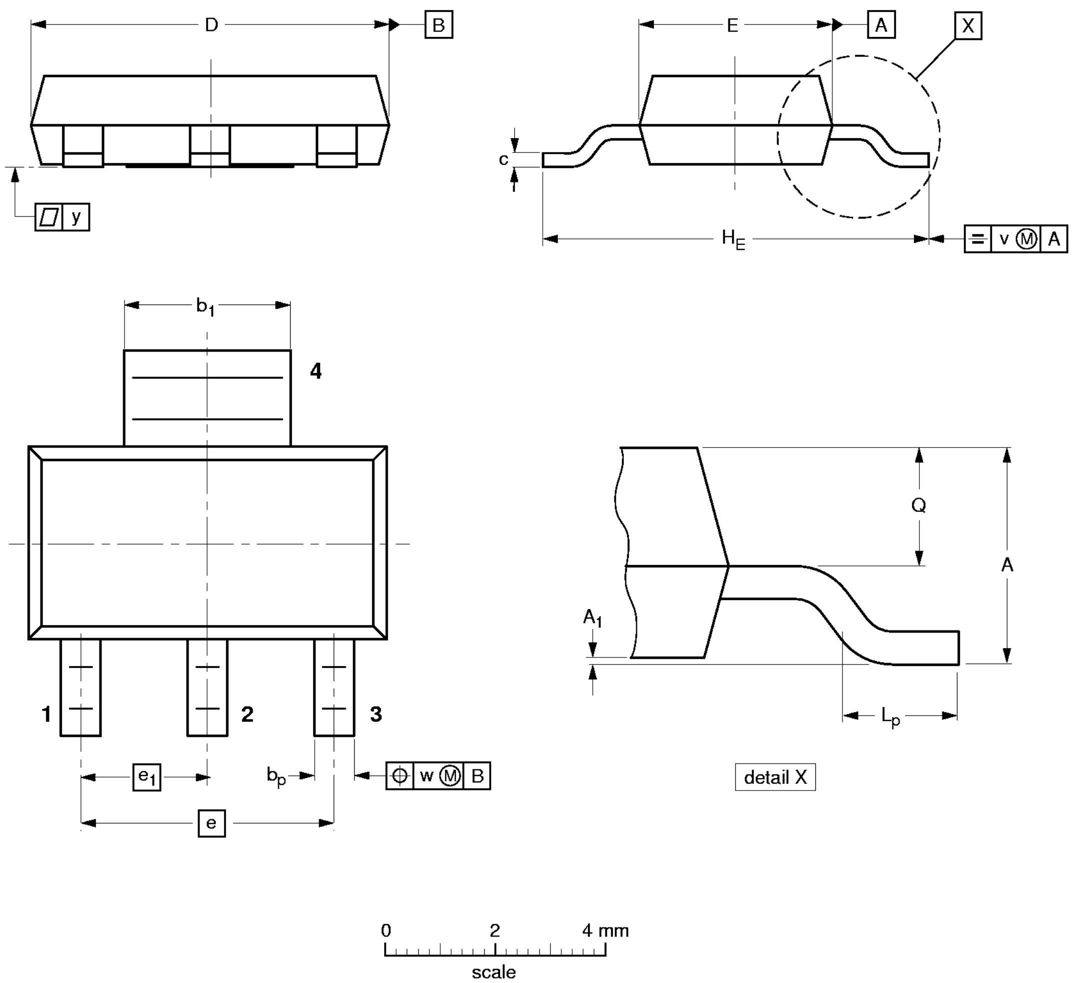
Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA.

PACKAGE OUTLINES

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						~~96-11-11~~ 97-02-28