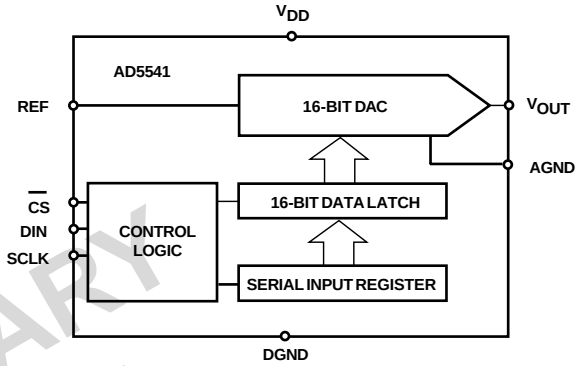
+5V, Serial Input Voltage Output, 16-Bit DACs

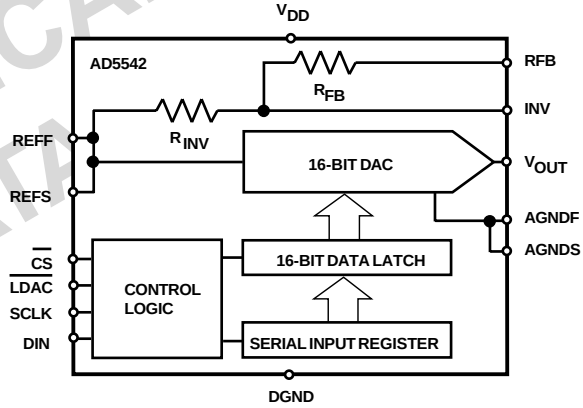
Preliminary Technical Data — AD5541/AD5542

FEATURES
Full 16-bit Performance
+5V Single Supply operation
Low Power
Short Settling Time
Unbuffered Voltage Output capable of driving 60kΩ loads directly
SPI/QSPI/MICROWIRE compatible interface standards
Power-On Reset clears DAC output to 0V (Unipolar mode)
Schmitt Trigger Inputs for Direct Optocoupler Interface

APPLICATIONS
Digital Gain and Offset Adjustment
Automatic Test Equipment
Data Aquisition Systems
Industrial Process Control

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD5541 and AD5542 are single 16 bit, serial input, voltage output DAC's that operate from a single +2.7V to +5V supply.

The AD5541 and AD5542 utilize a versatile three-wire interface that is compatible with SPI™, QSPI™ and MICROWIRE™ interface standards.

These DAC's provide 16 bit performance without any adjustments. The DAC output is unbuffered which reduces power consumption and offset errors contributed to by an output buffer.

The AD5542 can be operated in bipolar mode generating a $\pm V_{REF}$ output swing. The AD5542 also includes Kelvin sense connections for the reference and analog ground pins to reduce layout sensitivity.

The AD5541 and AD5542 are available in an SO package.

PRODUCT HIGHLIGHTS

1. Single Supply Operation.
   The AD5541 and AD5542 are fully specified and guaranteed for a single +5V ±5% supply.
2. Low Power Comsumption.
   These parts consume typically 1.5mW with a +5 V supply
3. 3 wire Serial Interface.
4. Unbuffered output capable of driving 60kΩ loads. This reduces power consumption as there is no internal buffer to drive.
5. Power On Reset circuitry.

SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corporation.

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AD5541/AD5542–SPECIFICATIONS (V_{DD} = +5V ± 5%, V_{REF} = +2.5V, AGND = DGND = 0 V. All specifications $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	Min	Typ	Max	Units	Test Conditions
STATIC PERFORMANCE					
Resolution	16			Bits	
Relative Accuracy		±0.5	±1.0	LSB	L grade
		±0.5	±2.0	LSB	B, K grade
		±0.5	±4.0	LSB	A grade
Differential Nonlinearity		±0.5	±1.0	LSB	Guaranteed Monotonic
Gain Error			±5	LSB	T_A = +25°C
			±10	LSB	
Gain Error Temperature Coefficient		±0.1		ppm/°C	
Zero Code Error			±1	LSB	T_A = +25°C
			±2	LSB	
Zero Code Temperature Coefficient		±0.05		ppm/°C	
AD5542					
Bipolar Resistor Matching		1.0			R_{FB}/R_{INV}
			±0.015	%	Ratio Error
Bipolar Zero Offset Error			±10	LSB	T_A = +25°C
			±20	LSB	
Bipolar Zero Temperature Coefficient		±0.5		ppm/°C	
OUTPUT CHARACTERISTICS					
Output Voltage Range	0		V_{REF}-1LSB	V	Unipolar Operation
	$-V_{REF}$		V_{REF}-1LSB	V	AD5542 Bipolar Operation
Output Voltage Settling Time		1		µs	to 1/2LSB of FS, C_L = 10pF
Slew Rate		25		V/µs	C_L = 10pF, measured from 0% to 63%
Digital-to-Analog Glitch Impulse		10		nV-s	1 LSB Change Around the Major Carry
Digital Feedthrough		10		nV-s	
DC Output Impedance		6.25		kΩ	tolerance typically 20%
Power Supply Rejection Ratio			±1.0	LSB	Δ V_{DD} ± 10%
DAC REFERENCE INPUT					
Reference Input Range	2.0		V_{DD}	V	
Reference Input Resistance[2]	9			kΩ	Unipolar Operation
	7.5			kΩ	AD5542, Bipolar Operation
LOGIC INPUTS					
Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.8	V	
V_{INH}, Input High Voltage	2.4				
Input Capacitance[3]			10	pF	
Hysteresis Voltage[3]		0.4		V	
REFERENCE					
Reference -3dB Bandwidth		1.3		MHz	All 1s loaded
Reference Feedthrough		1		mVp-p	All 0s loaded, V_{REF} = 1Vp-p at 100kHz
Signal-to-Noise Ratio		92		dB	
Reference Input Capacitance		75		pF	Code 0000 hex
		120		pF	Code FFFF hex
POWER REQUIREMENTS					
V_{DD}	4.75		5.25	V	
I_{DD}		0.3	1.1	mA	
Power Dissipation		1.5		mW	

NOTES
[1]Temperature ranges are as follows: A, B Versions: -40°C to +85°C, K, L Versions: 0°C to +70°C.
[2]Reference input resistance is code dependent, minimum at 8555 hex.
[3]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1,2]

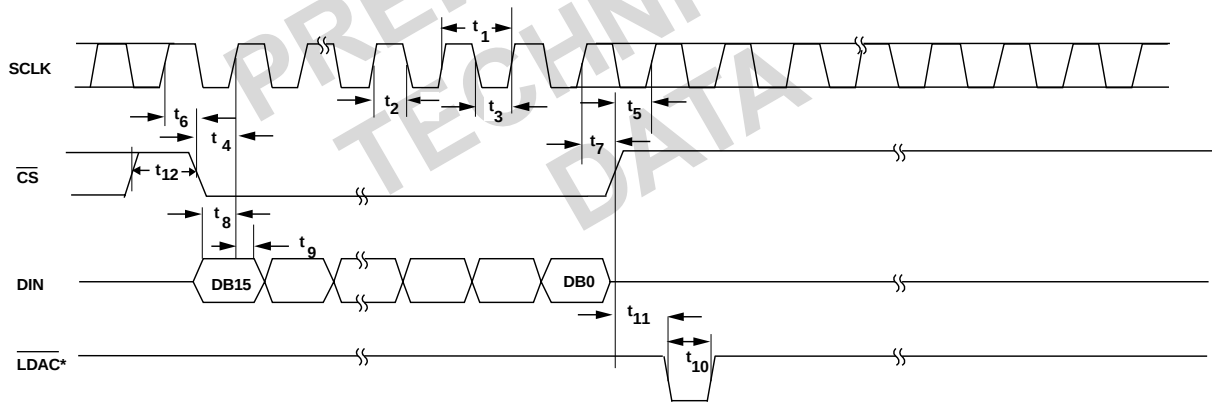
(V_{DD} = +5V ± 5%, V_{REF} = +2.5V, AGND = DGND = 0 V. All specifications T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} All Versions	Units	Description
f_{SCLK}	25	MHz max	SCLK cycle frequency
t_1	40	ns min	SCLK cycle time
t_2	20	ns min	SCLK high time
t_3	20	ns min	SCLK low time
t_4	15	ns min	$\overline{CS}$ low to SCLK high setup
t_5	15	ns min	$\overline{CS}$ high to SCLK high setup
t_6	35	ns min	SCLK high to $\overline{CS}$ low hold time
t_7	20	ns min	SCLK high to $\overline{CS}$ high hold time
t_8	15	ns min	Data setup tme
t_9	0	ns min	Data Hold time
t_{10}	30	ns min	$\overline{LDAC}$ pulse width
t_{11}	30	ns min	$\overline{CS}$ high to $\overline{LDAC}$ low setup
t_{12}	30	ns min	$\overline{CS}$ high time between active periods

[1] Guaranteed by design. Not production tested.

[2] Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are measured with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} +V_{IH})/2.

Specifications subject to change without notice.



*AD5542 Only. May be tied permanently low if required.

Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	–0.3 V to +6 V
Digital Input Voltage to DGND	-0.3V to V_{DD} +0.3 V
V_{OUT} to AGND	-0.3V to V_{DD} +0.3 V
AGND, AGNDF, AGNDS to DGND	-0.3V to +0.3V
Input Current to Any pin Except supplies	±10mA
Operating Temperature Range	
Industrial (A, B Versions)	–40°C to +85°C
Commercial (K, L Versions)	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Maximum Junction Temperature, (T_J max)	+150°C
Package Power Dissipation	(T_J max – T_A)/θ_{JA}
Thermal Impedance θ_{JA}	
SOIC(R-8)	149.5°C/W
SOIC(R-14)	104.5°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Relative Accuracy	Temperature Range	Package Description	Package Option
AD5541LR	±1 LSB	0°C to +70°C	8-Lead Small Outline IC	SO-8
AD5541KR	±2 LSB	0°C to +70°C	8-Lead Small Outline IC	SO-8
AD5541BR	±2 LSB	–40°C to +85°C	8-Lead Small Outline IC	SO-8
AD5541AR	±4 LSB	–40°C to +85°C	8-Lead Small Outline IC	SO-8
AD5542LR	±1 LSB	0°C to +70°C	14-Lead Small Outline IC	SO-14
AD5542KR	±2 LSB	0°C to +70°C	14-Lead Small Outline IC	SO-14
AD5542BR	±2 LSB	–40°C to +85°C	14-Lead Small Outline IC	SO-14
AD5542AR	±4 LSB	–40°C to +85°C	14-Lead Small Outline IC	SO-14

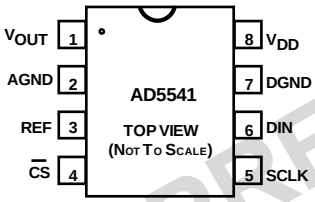
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5541/5542 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

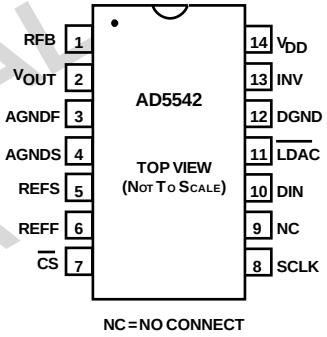
AD5541 PIN FUNCTION DESCRIPTION

Mnemonic	Pin	Description
V_{OUT}	1	Analog output voltage from the DAC.
AGND	2	Ground Reference point for analog circuitry.
REF	3	This is the voltage reference input for the DAC. Connect to external +2.5V reference. Reference can range from 2V to V_{DD}.
$\overline{CS}$	4	This is a logic input signal. The chip select signal is used to frame the serial data input.
SCLK	5	Clock input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
DIN	6	Serial data input. This device accepts 16-bit words. Data is clocked into the input register on the rising edge of SCLK.
DGND	7	Digital Ground. Ground reference for digital circuitry.
V_{DD}	8	Analog Supply Voltage, +5 V ±5%.

AD5541 PIN CONFIGURATION
SOIC



AD5542 PIN CONFIGURATION
SOIC



AD5542 PIN FUNCTION DESCRIPTION

Mnemonic	Pin	Description
RFB	1	Feedback resistor. In bipolar mode connect this pin to external op amp output.
V_{OUT}	2	Analog output voltage from the DAC.
AGNDF	3	Ground Reference point for analog circuitry (force).
AGNDS	4	Ground Reference point for analog circuitry (sense).
REFS	5	This is the voltage reference input (sense) for the DAC. Connect to external +2.5V refer ence. Reference can range from 2V to V_{DD}.
REFF	6	This is the voltage reference input (force) for the DAC. Connect to external +2.5V reference. Reference can range from 2V to V_{DD}.
$\overline{CS}$	7	This is a logic input signal. The chip select signal is used to frame the serial data input.
SCLK	8	Clock input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
NC	9	No Connect.
DIN	10	Serial data input. This device accepts 16-bit words. Data is clocked into the input register on the rising edge of SCLK.
$\overline{LDAC}$	11	$\overline{LDAC}$ input. When this input is taken low, the DAC register is simultaneously updated with the contents of the input register.
DGND	12	Digital Ground. Ground reference for digital circuitry.
INV	13	Connected to the internal scaling resistors of the DAC. Connect INV pin to external opamps inverting input in bipolar mode.
V_{DD}	14	Analog Supply Voltage, +5 V ±5%.

TERMINOLOGY

Relative Accuracy
For the DAC's relative accuracy or endpoint linearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity
Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Gain Error
Gain error is the difference between the actual and ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

Gain Error Drift
This is a measure of the change in gain error with changes in temperature. It is expressed in ppm/°C.

Zero Code Error
Zero code error is a measure of the output error when zero code is loaded to the DAC register.

Zero Code Temperature Coefficient
This is a measure of the change in zero code error with a change in temperature. It is expressed in µV/°C.

Digital-to-Analog Glitch Impulse
Digital-to-Analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. $\overline{CS}$ is held high, while the CLK and DIN signals are toggled. It is specified in nV-s and is measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

Power Supply Rejection Ratio
This specification indicates how the output of the DAC is affected by changes in the power supply voltage. Power-supply rejection ratio is quoted in terms of % change in output per % change in V_{DD} for full scale output of the DAC. V_{DD} is varied by ±10%.

Reference Feedthrough
This is a measure of the feedthrough from the V_{REF} input to the DAC output when the DAC is loaded with all 0s. A 100kHz, 1Vp-p is applied to V_{REF}. Reference feedthrough is expressed in mVp-p.

GENERAL DESCRIPTION

The AD5541/5542 are single 16 bit, serial input, voltage output DAC's. They operate from a single supply ranging from +2.7 V to +5 V and consume typically 300 µA with a supply of +5 V. Data is written to these devices in a 16 bit word format, via a three or four wire serial interface. To ensure a known power up state, these parts were designed with a power on reset function. In unipolar mode the output is reset to 0V, while in bipolar mode, the AD5542 output is set to $-V_{REF}$. Kelvin sense connections for the reference and analog ground are included on the AD5542.

Digital-to-Analog Section

The DAC architecture consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 2. The DAC architecture of the AD5541/5542 is segmented. The 4 MSBs of the 16 bit data word are decoded to drive 15 switches E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or V_{REF}. The remaining 12 bits of the data word drive switches S0 to S11 of a 12 bit voltage mode R-2R ladder network.

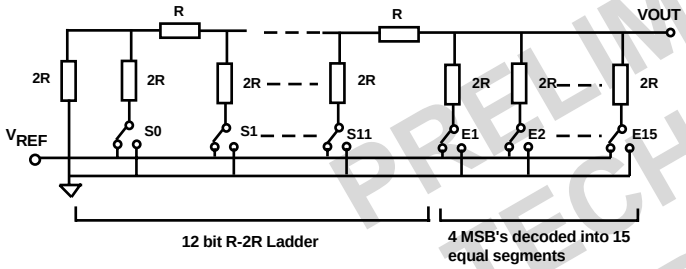


Figure 2. Dac Architecture.

In this type of DAC configuration, the output impedance is independent of code, while the input impedance seen by the reference is heavily code dependant. The output voltage is dependant on the reference voltage as shown in the following equation.

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where *D* is the decimal data word loaded to the DAC register and *N* is the resolution of the DAC. For a reference of +2.5 V, the equation simplifies to the following.

$$V_{OUT} = \frac{2.5 \times D}{65{,}536}$$

giving a V_{OUT} of 1.25 V with midscale loaded, and 2.5 V with full scale loaded to the DAC.
The LSB size is V_{REF}/65,536.

SERIAL INTERFACE

The AD5541 and AD5542 are controlled by a versatile 3-wire serial interface, which operates at clock rates up to 25 MHz and is compatible with SPI, QSPI, MICROWIRE and DSP interface standards. The timing diagram can be seen in Figure 1. Input data is framed by the chip select input, $\overline{CS}$. After a high to low transition on $\overline{CS}$, data is shifted synchronously and latched into the input register on the rising edge of the serial clock, SCLK. Data is loaded MSB first in 16 bit words. After 16 data bits have been loaded into the serial input register, a low to high transition on $\overline{CS}$ transfers the contents of the shift register to the DAC. Data can only be loaded to the part while $\overline{CS}$ is low.

The AD5542 has an $\overline{LDAC}$ function which allows the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. $\overline{LDAC}$ should be maintained high while data is written to the shift register. Alternatively, $\overline{LDAC}$ may be tied permanently low to update the DAC synchronously. With $\overline{LDAC}$ tied permanently low, the rising edge of $\overline{CS}$ will load the data to the DAC.

UNIPOLAR OUTPUT OPERATION

These DACs are capable of driving unbuffered loads of 60kΩ. Unbuffered operation results in low supply current, typically 300µA, and a low offset error. The AD5541 provides a unipolar output swing ranging from 0 V to V_{REF}. The AD5442 can be configured to output both unipolar and bipolar voltages. Figure 3 shows a typical unipolar output voltage circuit. The code table for this mode of operation is shown in Table 1.

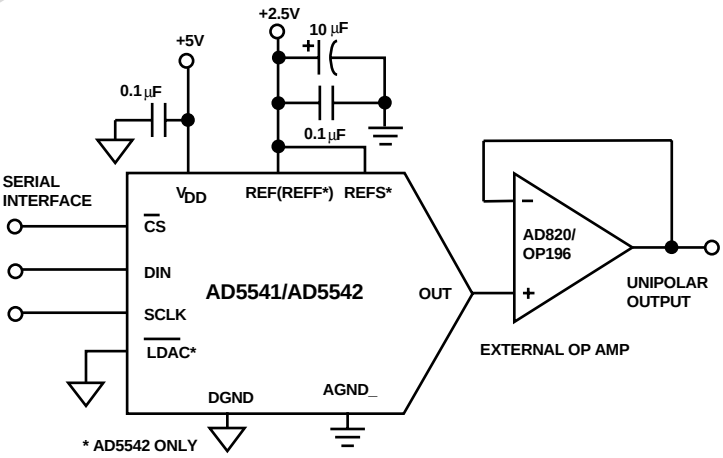


Figure 3. Unipolar Output.

Table 1. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
1111 1111 1111 1111	V_{REF} * (65,535/65,536)
1000 0000 0000 0000	V_{REF} * (32,768/65,536) = 1/2V_{REF}
0000 0000 0000 0001	V_{REF} * (1/65,536)
0000 0000 0000 0000	0 V

BIPOLAR OUTPUT OPERATION

With the aid of an external opamp, the AD5542 may be configured to provide a bipolar voltage output. A typical circuit of such operation is shown in Figure 4. The matched bipolar offset resistors R_{FB} and R_{INV} are connected to an external opamp to achieve this bipolar output swing. Table 2 shows the transfer function for this output operating mode. Also provided on the AD5542 are a set of Kelvin connections to the analog ground inputs.

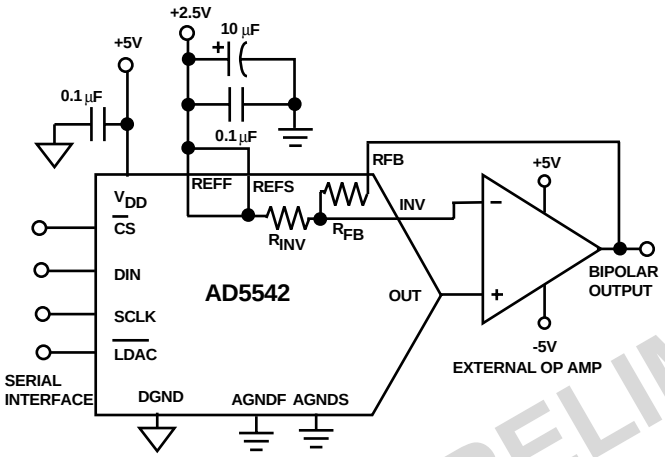


Figure 4. Bipolar Output (AD5542 only).

Table 2. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
1111 1111 1111 1111	$+V_{REF}$ * (32,767/32,768)
1000 0000 0000 0001	$+V_{REF}$ * (1/32,768)
1000 0000 0000 0000	0V
0111 1111 1111 1111	$-V_{REF}$ * (1/32,768)
0000 0000 0000 0000	$-V_{REF}$ * (32,768/32,768) = $-V_{REF}$

OUTPUT AMPLIFIER SELECTION

For bipolar mode, a precision amplifier should be used, supplied from a dual power supply, this will provide the $\pm V_{REF}$ output. In a single supply application, selection of a suitable opamp may be more difficult as the output swing of the amplifier does not usually include the negative rail, in this case AGND. This can result in some degradation of the specified performance unless the application does not use codes near zero.

The selected opamp needs to have very low offset voltage, (the DAC LSB is 38µV with a 2.5 V reference), to eliminate the need for output offset trims. Input bias current should also be very low as the bias current multiplied by the DAC output impedance (approx. 6k) will add to the zero code error. Rail to rail input and output performance is required. For fast settling, the slew rate of the opamp should not impede the settling time of the DAC. Output impedance of the DAC is constant and code independent, but in order to minimise gain errors, the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3dB bandwidth of 1MHz or greater. The amplifier adds another time constant to the system, hence increasing the settling time of the output. A higher 3dB amplifier bandwidth, results in a shorter effective settling time of the combined DAC and amplifier.

FORCE SENSE AMPLIFIER SELECTION

These amplifiers will be single supply, low noise amplifiers. A low output impedance at high frequencies is preferred as they need to be able to handle dynamic currents of up to ±20mA.

REFERENCE AND GROUND

As the input impedance is code dependant, the reference pin should be driven from a low impedance source. The AD5541/5542 operates with a voltage reference ranging from +2 V to V_{DD}. The DAC's full scale output voltage is determined by the reference. Tables 1 and 2 outline the analog output voltage for particular digital codes. For optimum performance, Kelvin sense connections are provided on the AD5542.

If the application doesn't require separate force and sense lines, they should be tied together close to the package to minimize voltage drops between the package leads and the internal die.

POWER ON RESET

These parts have a power on reset function to ensure the output is at a known state upon power up. On power up, the DAC register contains all zeros, until data is loaded from the serial register. However, the serial register is not cleared on power up, so its contents are undefined. When loading data initially to the DAC, 16 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 16 bits are loaded, then the last 16 are kept, and if less than 16 are loaded, then bits will remain from the previous word. If the AD5541/5542 needs to be interfaced with data shorter than 16 bits, then the data should be padded with zeros at the LSBs.

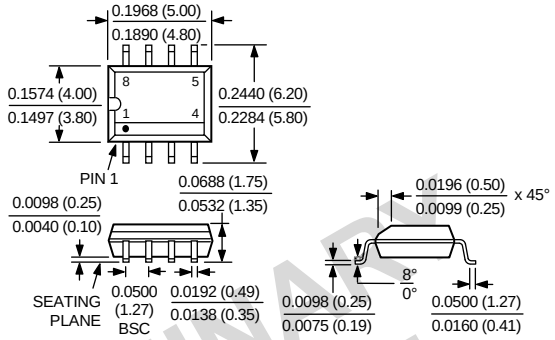
POWER SUPPLY AND REFERENCE BYPASSING

For accurate high resolution performance, it is recommended that the reference and supply pins be bypassed with a 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SO
(SO-8)



14 Lead SO
(R-14)