REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 04. Editorial changes to pages 2,3,5,6,7, and 8. Editorial changes throughout.	91-03-22	M. A. Frye
B	Add device type 05. Format update, editorial changes throughout.	95-10-16	M. A. Frye

REV																				
SHEET																				
REV	B	B	B	B																
SHEET	15	16	17	18																

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
89-11-15

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, PROGRAMMABLE LOGIC CELL ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88638**

SHEET 1 OF 18

DESC FORM 193
JUL 94

5962-E300-95

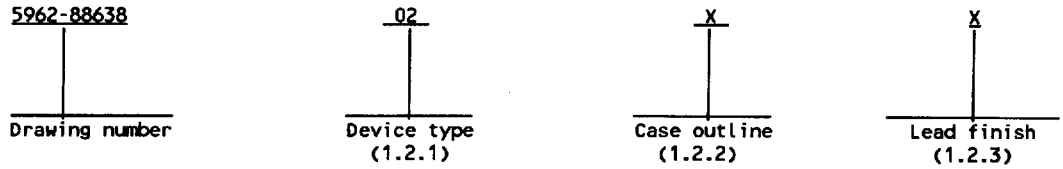
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0014058 995

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Toggle speed
02	2018	10 x 10, 1800 gate programmable array	33 MHz
03	2018	10 x 10, 1800 gate programmable array	50 MHz
04	2018	10 x 10, 1800 gate programmable array	70 MHz
05	2018	10 x 10, 1800 gate programmable array	100 MHz

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15-PN	84	pin grid array package 1/

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V to 7.0 V
Input voltage range (V_{IN})	-0.5 V to V_{CC} + 0.5 V
Voltage applied to three-state output range (V_{TS})	-0.5 V to V_{CC} + 0.5 V
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum soldering temperature (soldering, 10 seconds)	+260°C
Thermal resistance (Θ_{JC})	See MIL-STD-1835
Maximum junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Supply voltage relative to ground range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Input voltage range (V_{IN})	0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	0.0 V dc to V_{CC}

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Microcircuits, General Specification for.

1/ 84 actual pins used plus one (1) electrically not connected, locator pin = 85; not maximum listed in appendix C of MIL-M-38510.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic block diagrams. The logic block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA, $V_{IN} = V_{IHC}$ minimum, V_{IHT} minimum or V_{ILC} maximum, V_{ILt} maximum		1,2,3	All	3.7		V
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 4.0 mA, $V_{In} = V_{IHC}$ minimum, V_{IHT} minimum or V_{ILC} maximum, V_{ILt} maximum		1,2,3	All		0.4	V
Quiescent power supply current	I_{CCO}	$V_{CC} = V_{IN}$ = 5.5 V,	CMOS	1,2,3	All		10	mA
			TTL				15	
Power-down supply current	I_{CCPD}	$V_{CC} = V_{IN}$ = 5.5 V, $\overline{PWRDWN}$ = 0 V		1,2,3	All		0.5	mA
Power-down supply voltage	V_{PD}	$\overline{PWRDWN}$ = 0 V see figure 3		1,2,3	All	3.5	---	V
Input leakage current	I_{IL}	V_{IN} = 0 V and 5.5 V, V_{CC} = 5.5 V		1,2,3	All	-10	+10	µA
Output leakage current	I_{OZ}	V_{IN} = 0 V and 5.5 V, V_{CC} = 5.5 V with no load		1,2,3	All	-10	+10	µA
High level input voltage TTL	V_{IHT}			1,2,3	All	2	---	V
Low level input voltage TTL	V_{ILT}			1,2,3	All	---	0.8	V
High level input voltage CMOS	V_{IHC}			1,2,3	All	0.7 V_{CC}	---	V
Low level input voltage CMOS	V_{ILC}			1,2,3	All	---	0.2 V_{CC}	V
Input capacitance except XTL1 and XTL2	C_{IN}	See 4.3.1c		4	All	---	10	pF
Input capacitance XTL1 and XTL2	C_{IN}	See 4.3.1c		4	All	---	15	pF
Output capacitance	C_{OUT}	See 4.3.1c		4	All		10	pF
Functional test	FT	See 4.3.1d		7,8A,8B	All			
Interconnect + t_{PID} + t_{OPS} + 10(t_{ILO})	t_{B1}	Measured on 10 columns See figure 3		9,10,11	02		238	ns
					03		178	
					04		119	
					05		86	
Interconnect + t_{PID} + 10(t_{ITO}) + t_{OPS}	t_{B2}			9,10,11	02		288	ns
					03		228	
					04		159	
					05		115	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Interconnect + t_{PID} + t_{OPS} + $10(t_{ITO})$ + $10(t_{QLO})$	t_{B3}	Measured on 10 columns See figure 3	9,10,11	02		410	ns
				03		302	
				04		217	
				05		172	
Tested on all CLBs with t_{ICK} + interconnect + t_{CKO} + $2t_{ILO}$	t_{B4}	See figure 3	9,10,11	02		85	ns
				03		62	
				04		42	
				05		33	
Tested on all CLBs with t_{ICI} + interconnect + t_{CIO} + t_{ILO}	t_{B5}		9,10,11	02		66	ns
				03		49	
				04		38	
				05		26.5	
Tested on all CLBs with t_{ICC} + interconnect + t_{CCO} + $2(t_{ILO})$	t_{B6}		9,10,11	02		90	ns
				03		67	
				04		41	
				05		31	
Interconnect + t_{CKO} + t_{IHCK} + t_{CKIH}	t_{B7}	Measured on 10 rows. See figure 3	9,10,11	02		318	ns
				03		269	
				04		183	
				05		128	
$3t_{PID}$ + interconnect + t_{PL} + t_{LI} + $4(t_{OPS})$	t_{B8}	Tested on all IOBs See figure 3	9,10,11	02		274	ns
				03		204	
				04		141	
t_{PL} + t_{LI} + t_{OPS} + interconnect	t_{B9}		9,10,11	05		32.5	ns
Logic input to output (combinatorial)	t_{ILO}	See figure 3	1/	02		20	ns
				03		15	
				04		10	
				05		7.5	
Logic input to output (transparent-latch)	t_{ITO}		1/	02		25	ns
				03		20	
				04		14	
				05		10	
Logic input to output (additional for Q through F)	t_{QLO}		1/	02		13	ns
				03		8	
				04,05		6	
K clock to output	t_{CKO}		1/	02		20	ns
				03		15	
				04		10.5	
				05		7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
K clock logic-input setup	t_{ICK}		1/	02	12		ns
				03	8		
				04	7		
				05	6		
K clock logic-input hold	t_{CKI}		1/	All	2		ns
C clock to output	t_{CCO}		1/	02		25	ns
				03		19	
				04		13	
				05		9	
C clock logic-input setup	t_{ICC}		1/	02	12		ns
				03	9		
				04	6		
				05	5		
C clock logic-input hold	t_{CCI}		1/	02	6		ns
				03,04	2		
				05	1		
Logic input to G clock to output	t_{CIO}		1/	02		37	ns
				03		27	
				04		20	
				05		13	
Logic input to G clock logic-input setup	t_{ICI}		1/	02	6		ns
				03	4		
				04	3		
				05	2		
Logic input to G clock logic-input hold	t_{CII}		1/	02	9		ns
				03	5		
				04	4		
				05	3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Set/reset direct input A or D to out	t_{RIO}		1/	02		25	ns
				03		22	
				04		16	
				05		10	
Set/reset direct through F or G to out	t_{RLO}		1/	02		37	ns
				03		28	
				04		21	
				05		14	
Set/reset direct master reset pin to out	t_{MRQ}		1/	02		55	ns
				03		45	
				04		40	
				05		17	
Set/reset direct seperation of set/reset	t_{RS}		1/	02	17		ns
				03	9		
				04	7		
				05	6		
Set/reset direct set/reset pulse-width	t_{RPW}		1/	02	12		ns
				03	9		
				04	7		
				05	6		
Flip-flop toggle rate Q through F to flip-flop	F_{CLK}		1/	02	33		MHz
				03	50		
				04	70		
				05	100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock high	t_{CH}		1/	02	12		ns
				03	8		
				04	7		
				05	5		
Clock low	t_{CL}		1/	02	12		ns
				03	8		
				04	7		
				05	5		
Pad (package pin) to input direct	t_{PID}		1/	02		12	ns
				03		8	
				04		6	
				05		4	
I/O clock to input (storage)	t_{LI}		1/	02		20	ns
				03		15	
				04		11	
				05		8	
I/O clock to pad-input setup	t_{PL}		1/	02	12		ns
				03	8		
				04	6		
				05	4		
I/O clock to pad-input hold	t_{LP}		1/	All	0		ns
I/O clock pulse width	t_{LW}		1/	02	12		ns
				03	9		
				04	7		
				05	5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output (enabled) to pad	t_{OP}		1/	02		15	ns
				03		12	
				04		9	
				05		7	
Three-state to pad begin hi-z	t_{THZ}		1/	02		25	ns
				03		20	
				04		15	
				05		11	
Three-state to pad end hi-z	t_{TON}		1/	02		25	ns
				03		20	
				04		16	
				05		13	
$\overline{\text{RESET}}$ to input (storage)	t_{RI}		1/	02		40	ns
				03		30	
				04		26	
				05		17	
$\overline{\text{RESET}}$ to input clock	t_{RC}		1/	02	35		ns
				03	25		
				04	20		
				05	14		

1/ Parameter is not directly tested. Devices are first 100 percent functionally tested. Benchmark patterns (t_{B1-8}) are then used to determine the compliance of this parameter. Characterization data are taken at initial device testing, prior to the introduction of significant changes, and at least twice yearly to monitor correlation between benchmark patterns and this parameter.

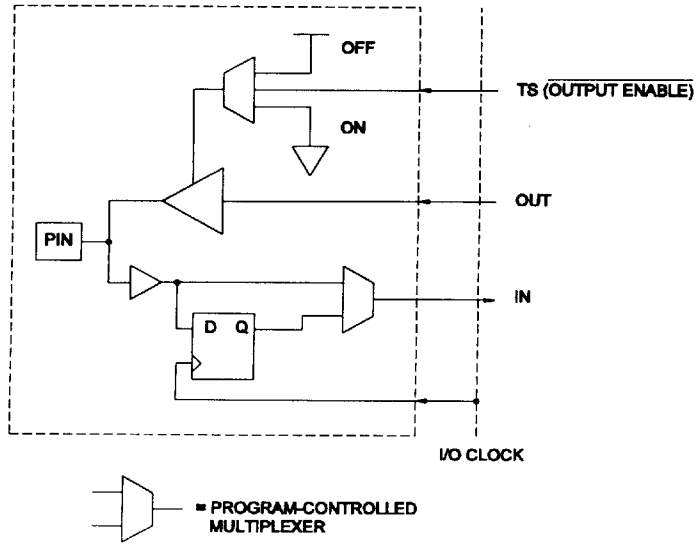
2/ Minimum CLOCK widths for the auxillary buffer are 1.25 times the t_{CH}, t_{CL}.

Case X

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
A1	A9-I/O		D1	I/O		K1	I/O
A2	A8-I/O		D2	I/O		K2	M2-I/O
A3	A-11I/O		D10	$\overline{WRT}$-D1-I/O		K3	HDC-I/O
A4	A-12I/O		D11	I/O		K4	I/O
A5	I/O		E1	I/O		K5	I/O
A6	A-13I/O		E2	I/O		K6	I/O
A7	I/O		E3	I/O		K7	I/O
A8	A-4I/O		E9	I/O		K8	I/O
A9	A-3I/O		E10	I/O		K9	D6-I/O
A10	A-2I/O		E11	CS2-D2-I/O		K10	$\overline{RESET}$
A11	CCLK		F1	I/O		K11	XTL1 or I/O
B1	I/O		F2	I/O		L1	MO-RTRIG
B2	$\overline{PWRDWN}$		F3	VCC		L2	I/O
B3	A10-I/O		F9	VCC		L3	LDC-I/O
B4	A7-I/O		F10	I/O		L4	I/O
B5	I/O		F11	I/O		L5	I/O
B6	A14-I/O		G1	I/O		L6	I/O
B7	I/O		G2	I/O		L7	I/O
B8	A15-I/O		G3	I/O		L8	I/O
B9	A1-I/O		G9	$\overline{CS1}$-D3-I/O		L9	I/O
B10	A0-I/O		G10	I/O		L10	D7-I/O
B11	DIN-D0-I/O		G11	$\overline{CS0}$-D4-I/O		L11	XT2 o I/O
C1	I/O		H1	I/O			
C2	I/O		H2	I/O			
C3	INDEX PIN		H10	D5-I/O			
C5	A6-I/O		H11	I/O			
C6	GND		J1	I/O			
C7	A5-I/O		J2	M1-$\overline{RDATA}$			
C10	$\overline{DOUT}$-I/O		J10	DONE-$\overline{PROG}$			
C11	$\overline{RCLK}$ I/O		J11	I/O			

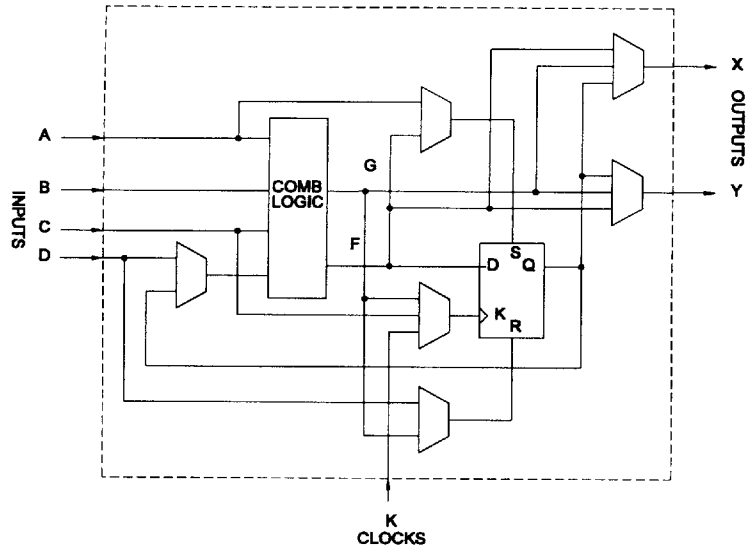
NC = NO CONNECT

FIGURE 1. Terminal connections



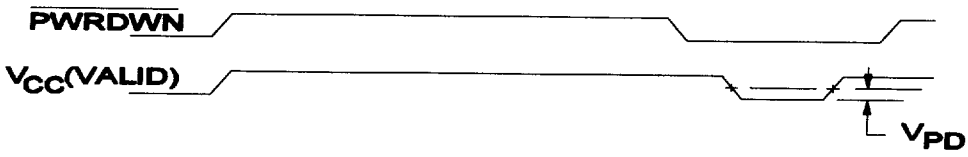
= PROGRAM-CONTROLLED MULTIPLEXER

I/O BLOCK



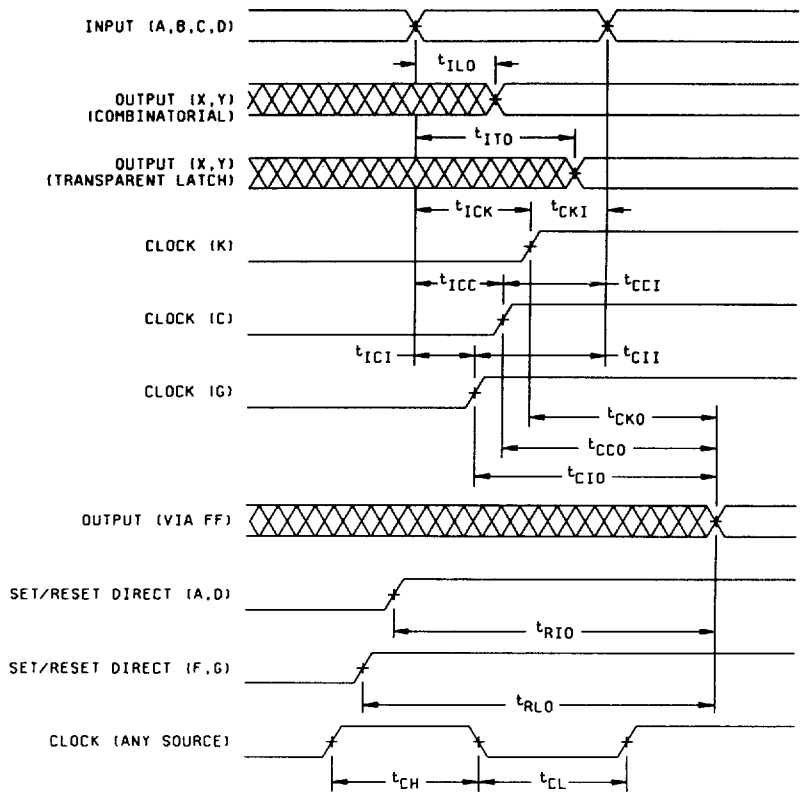
CONFIGURABLE LOGIC BLOCK

FIGURE 2. Logic block diagram.



General logic cell array (LCA) switching characteristics.

FIGURE 3. Timing diagrams and switching characteristics.



NOTES:
1. Configurable logic block (CLB) switching characteristics.
2. Timing is measured at 0.5 Vcc levels with 50 pF minimum output load.
   Input signal conditioning: Rise and fall times ≤ 6 ns; Amplitude = 0 and 3 V.

FIGURE 3. Timing diagrams and switching characteristics - Continued.

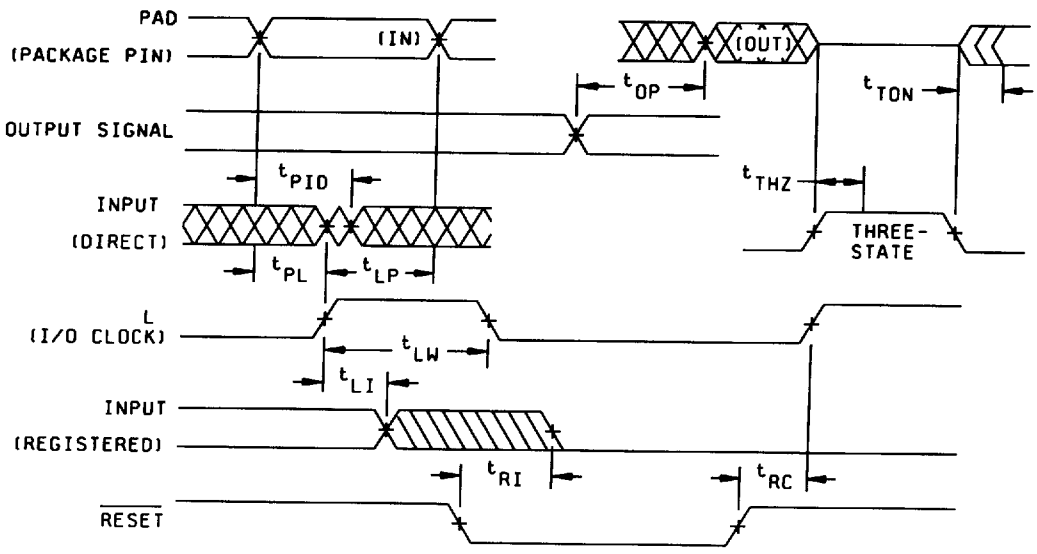


FIGURE 3. Timing diagrams and switching characteristics - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D or E using the circuit submitted with the certificate of compliance (see 3.6 herein). The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 5 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall consist of verifying functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, D, or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Device programming.

4.4.1 Programming procedures and characteristics. Programming procedures and characteristics shall be as specified by the individual device manufacturer and shall be made available upon request.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

Line no.	Test Requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
1	Interim electrical parameters (see 4.2)	
2	Staic burn-in (method 1015)	Required
3	Same as line 1	
4	Dynamic burn-in (method 1015)	Not Required
5	Final electrical paramters	1*,2,3,7*, 8A,8B,9,10, 11
6	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11
7	Group C end-point electrical parameters	2,3,7, 8A,8B
8	Group D end-point electrical parameters	2,3,8A,8B,
9	Group E end-point electrical parameters	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes..

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DDForm 1692, Engineering Change Proposal MIL-STD-481 using DD form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Pin descriptions.

PIN name (number)	Descriptions
$\overline{\text{PWRDWN}}$ (B2)	POWER-DOWN. An active low power-down input stops all internal activity to minimize V_{CC} power and puts all output buffers in a high-impedance state. Configuration is retained, however, internal storage elements are Reset. When the PWRDWN pin returns HIGH, the device returns to operation with the same sequence of reset, buffer enable and DONE/PROGRAM as at the completion of configuration. If not used PWRDWN must be tied to V_{CC}.
M0 (L1)	MODE 0. This input and M1, M2 are sampled before the start of configuration to establish the configuration mode to be used.
RTRIG (L1)	READ TRIGGER. This input transition to a HIGH, after configuration is complete, will initiate a readback of configuration and storage element data by CCLK. This operation may be limited to a single request, or be inhibited altogether, by selecting the appropriate readback option when generating the bit stream.
M1 (J2)	MODE 1. This input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used. If readback is to be used, a 5 k[resistor should be used to define mode level inputs.
$\overline{\text{RDATA}}$ (J2)	READ DATA. After configuration is complete, this pin is the output of the readback data.
M2 (K2)	MODE 2. This input and M0, M1 are sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin becomes a user-programmable I/O.
HDC (K3)	HIGH DURING CONFIGURATION. This pin is held at a HIGH level by the logic cell array (LCA) until after configuration. It is intended to be available as a control output indicator, indicating that configuration is not yet completed. After configuration, this pin is a user I/O.
$\overline{\text{LDC}}$ (L3)	LOW DURING CONFIGURATION. This pin is held at a LOW level by the logic cell array (LCA) until after configuration. It is available as a control output indicating that configuration is not yet completed. It is particulary useful in master mode as a LOW enable for an EPROM. After configuration, this pin is a user I/O. If used as a LOW EPROM enable, it must be programmed as a HIGH after configuration.
$\overline{\text{RESET}}$ (K10)	RESET. This is an active-low input which has three functions. Prior to the start of configuration, a LOW input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle on the order of 100 ms. When the time-out and RESET are complete, the levels of the "M" mode lines are sampled and configuration begins. If RESET is asserted during a configuration, the LCA is reinitialized and will restart the configuration at the termination of RESET. If RESET is asserted after configuration is complete, it will provide an asynchronous reset of all I/O block (IOB) and configurable logic block (CLB) storage elements of the logic cell array (LCA). RESET can also be used to recover from partial power failure.
DONE (J10)	DONE. This open drain output is configurable with or without an internal pull-up resistor of about 3 k[. At the completion of configuration the circuitry of the LCA becomes active in a synchronous order and DONE may be programmed to occur one cycle before or after that.

PIN name (number)	Descriptions
$\overline{\text{PROG}}$ (J10)	PROGRAM. Once configuration is done, a HIGH-to-LOW transition of this program pin will cause an initialization of the LCA and start a reconfiguration if that mode is selected in the current configuration.
XTL1 (K11)	EXTERNAL CRYSTAL. This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.
XTL2 (L11)	EXTERNAL CRYSTAL. This user I/O pin can be used as the input of an amplifier driving an external crystal and bias circuitry.
CCLK (A11)	CONFIGURATION CLOCK. During configuration this pin is an output of an LCA in either master or peripheral mode. LCAs in slave mode use it as clock input . During a readback operation, it is a clock input for the configuration data being shifted out.
DOUT (C10)	DATA OUT. This user I/O pin used during configuration to output serial configuration data for daisy-chained slaves' data in.
DIN (B11)	DATA IN. This user I/O pin used as serial data input during slave or master serial configuration. This pin is Data 0 input in master or peripheral configuration mode.
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$ ($\overline{\text{G11}}$), ($\overline{\text{G9}}$) CS2, WRT (E11),(D10) D1).	CHIP SELECT, WRITE. These four inputs represent a set of signals, three active low and one active high, which are used in the peripheral mode to control configuration data entry. The assertion of all four generates a LOW CCLK and shifts DOUT data. In master mode, these pins become part of the parallel configuration byte (D4, D3, D2, After configuration is complete, they are user-programmed I/O.
$\overline{\text{RCLK}}$ (C11)	READ CLOCK. During master parallel mode configuration, this pin represents a "read" clock of an external dynamic memory device (normally not used). After configuration is complete, this pin becomes a user-programmed I/O.
D0-D7 (B11, D10, E11, G9, G11, H10, K9, L10)	DATA. This set of 8 pins represents the parallel configuration data byte for the parallel master and peripheral modes. After configuration is complete, they are user-programmed I/O pins.
A0-A15	ADDRESS. This set of 16 pins repersents an address output for an external configuration memory during master parallel mode. After configuration is complete, they are user-programmed I/O pins. (Pin numbers are as follows: B10, B9, A10, A9, A8, C7, C5, B4, A2, A1, B3, A3, A4, A6, B6, B8; respectively.)
I/O	INPUT/OUTPUT. A pin which may be programmed by the user to be input and/or output following configuration. Some of these pins present a high-impedance pullup or perform other functions before configuration is complete. Pin numbers are as follows: A5, A7, B1, B5, B7, C1, C2, D1, D2, D11, E1, E2, E3, E9, E10, F1, F2, F10, F11, G1, G2, G3, G10, H1, H2, H11, J1, J5, J7, J11, K1, K4, K5, K6, K7, K8, L2, L4, L5, L6, L7, L8, and L9.
V_{CC} (F3, F9)	Two connections to the nominal +5 V supply voltage. All must be connected.
GND (C6, J6)	Two connections to ground. All must be connected.
Index pin (C3)	For polarization.

6.7 Approved source of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.