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Defense Electronics
Supply Center
Dayton, Ohio

Original date
of drawing:

19 JANUARY 1988

AMSC N/A

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SIZE

CODE IDENT. NO.
67268

REV

MILITARY DRAWING
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Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, 32K X 8,
NMOS EEPROM, MONOLITHIC SILICON

DWG NO. **5962-87649**

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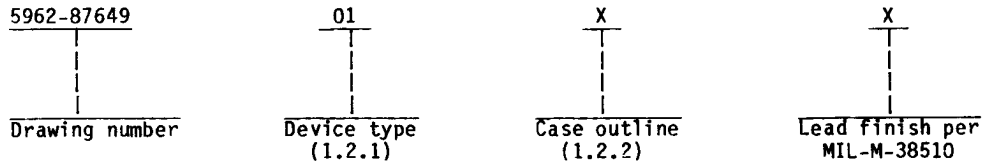
5962-E464

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MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

```
        5962-87649              01              X                X
            |                    |              |                |
            |                    |              |                |
            |                    |              |                |
            |                    |              |                |
       Drawing number      Device type     Case outline     Lead finish per
                             (1.2.1)         (1.2.2)          MIL-M-38510
```

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(see 6.4)	(32K x 8 EEPROM)	350 ns
02	(see 6.4)	(32K x 8 EEPROM)	300 ns
03	(see 6.4)	(32K x 8 EEPROM)	250 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, 1/2" x 1 3/8"), dual-in-line package
Y	C-12 (32-terminal, .450" x .550"), rectangular chip carrier package
Z	See figure 1 (28-lead, 3/8" x 3/4"), flat package

1.3 Absolute maximum ratings. 1/

Temperature under bias - - - - - - - - - - - - - - - - -	$-65°C$ to $+135°C$
Storage temperature range- - - - - - - - - - - - - - - -	$-65°C$ to $+150°C$
Voltage on any pin with respect to ground- - - - - - - -	-1.0 V dc to $+7.0$ V dc
DC output current- - - - - - - - - - - - - - - - - - - -	5 mA
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X and Y- - - - - - - - - - - - - - - - - - - -	See MIL-M-38510, appendix C
Case Z -	$15°C/W$
Lead temperature (soldering, 10 seconds) - - - - - - - -	$+300°C$
Input voltage range- - - - - - - - - - - - - - - - - - -	-0.3 V dc to $+6.5$ V dc
Endurance (minimum) - - - - - - - - - - - - - - - - - - -	10,000 cycles
Data retention (minimum) - - - - - - - - - - - - - - - -	10 years

1.4 Recommended operating conditions.

Operating supply voltage - - - - - - - - - - - - - - - -	5.0 V dc $\pm10\%$
Case operating temperature range (T_C)- - - - - - - - -	$-55°C$ to $+125°C$
High level input voltage - - - - - - - - - - - - - - - -	$+2.0$ V dc to V_{CC} $+1.0$ V dc
Low level input voltage- - - - - - - - - - - - - - - - -	-0.1 V dc to $+0.8$ V dc

1/ Unless otherwise specified, all voltages are referenced to ground.

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DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444			5962-87649
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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510   - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883   - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table. The truth table shall be as specified on figure 3.

3.2.3 Block diagram. The block diagram shall be as specified on figure 4.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C $\leq T_C \leq$ +125°C V_{SS} = 0.0 V, 4.5 V $\leq V_{CC} \leq$ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Supply current	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, All I/Os are open, all other inputs at V_{CC}	1, 2, 3	All		120	mA
Supply current (standby)	I_{SB}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, all other inputs at V_{CC}	1, 2, 3	All		60	mA
Input leakage current	I_{IL}	V_{IN} = 0.0 V to 5.5 V	1, 2, 3	All		10	μA
Output leakage current	I_{OL} 1/	$\overline{CE}$ = $\overline{OE}$ = V_{IH}, V_{OUT} = 0.0 V to 5.5 V	1, 2, 3	All		10	μA
Low level input voltage	V_{IL}		1, 2, 3	All	-1.0	0.8	V
High level input voltage	V_{IH}		1, 2, 3	All	2.0	V_{CC} +1	V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA, V_{CC} = 4.5 V	1, 2, 3	All		0.4	V
High level output voltage	V_{OH}	I_{OH} = -400 μA, V_{CC} = 4.5 V	1, 2, 3	All	2.4		V
Input capacitance	C_I 2/ 3/	V_{IN} = 0.0 V, V_{CC} = 5.0 V f = 1.0 MHz, T_A = +25°C See 4.3.1c	4	All		6	pF
Output capacitance	C_O 2/ 3/	V_{IN} = 0.0 V, V_{CC} = 5.0 V f = 1.0 MHz, T_A = +25°C See 4.3.1c	4	All		10	pF
Read cycle time	t_{AVAV} 4/	See figure 5	9,10,11	01 02 03	350 300 250		ns
Address access time	t_{AVAQ} 4/	See figure 5 $\overline{CE}$ = $\overline{OE}$ = V_{IL}	9,10,11	01 02 03		350 300 250	ns
Chip enable access time	t_{ELQV} 4/	See figure 5 $\overline{OE}$ = V_{IL}	9,10,11	01 02 03		350 300 250	ns

See footnotes at end of table.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0.0$ V, 4.5 V $\le V_{CC} \le 5.5$ V 4/ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output enable access time	t_{OLQV}	See figure 5 $\overline{CE} = V_{IL}$	9,10,11	All		100	ns
Chip enable to output in low Z	t_{ELQX} 2/	See figure 5	9,10,11	All	0		ns
Chip disable to output in high Z	t_{EHQZ} 2/ 5/	See figure 5	9,10,11	All	0	80	ns
Output enable to output in low Z	t_{OLQX} 2/	See figure 5	9,10,11	All	0		ns
Output disable to output in high Z	t_{OHQZ} 2/ 5/	See figure 5	9,10,11	All	0	80	ns
Output hold from address change	t_{AXQX}	See figure 5 $\overline{CE} = \overline{OE} = V_{IL}$	9,10,11	All	0		ns
Write cycle time $\overline{WE}$ controlled write	t_{WLWL} 6/	See figures 6 and 7	9,10,11	All		10	ms
Write cycle time $\overline{CE}$ controlled write	t_{ELEL} 6/	See figures 6 and 7	9,10,11	All		10	ms
Address to $\overline{WE}$ setup time	t_{AVWL}	See figures 6 and 7	9,10,11	All	0		ns
Address to $\overline{CE}$ setup time	t_{AVEL}	See figures 6 and 7	9,10,11	All	0		ns
Address hold time after $\overline{WE}$ low	t_{WLAX}	See figures 6 and 7	9,10,11	All	150		ns
Address hold time after $\overline{CE}$ low	t_{ELAX}	See figures 6 and 7	9,10,11	All	150		ns
$\overline{CE}$ to $\overline{WE}$ setup time	t_{ELWL}	See figures 6 and 7	9,10,11	All	0		ns
$\overline{WE}$ to $\overline{CE}$ setup time	t_{WLEL}	See figures 6 and 7	9,10,11	All	0		ns

TABLE I. Electrical performance characteristics - Continued.

See footnotes at end of table.

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Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0.0$ V, 4.5 V $\le V_{CC} \le 5.5$ V 4/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
CE hold after WE high	t_{WHEH}	See figures 6 and 7	9,10,11	All	0		ns
WE hold after CE high	t_{EHWH}	See figures 6 and 7	9,10,11	All	0		ns
CE pulse width	t_{ELEH}	See figures 6 and 7	9,10,11	All	150		ns
WE pulse width	t_{WLWH}	See figures 6 and 7	9,10,11	All	150		ns
OE high setup time	t_{OHEL} t_{OHWL} 7/	See figures 6, 7, 8, and 9	9,10,11	All	10		ns
OE high hold time	t_{WHOL} t_{EHOL} 7/	See figures 6, 7, 8, and 9	9,10,11	All	10		ns
Write control recovery time	t_{WHWL}	See figures 6 and 7	9,10,11	All	1		µs
Data valid time	t_{WLDV}	See figure 6	9,10,11	All		300	ns
Data setup time	t_{DVWH} t_{DVEH}	See figure 6	9,10,11	All	100		ns
Data setup time	t_{WHDX} t_{EHDX}	See figure 6	9,10,11	All	15		ns
Byte load cycle	t_{WLWL}	See figure 7	9,10,11	All	2	100	µs
Data valid to next write	t_{DVWL}	See figures 8 and 9	9,10,11	All	10		µs
CE to WE setup time	t_{ELWL}	See figure 10	9,10,11	All	10		ns
Data to WE setup time	t_{DVWL} 7/	See figure 10	9,10,11	All	10		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $V_{SS} = 0.0$ V, 4.5 V $\leq V_{CC} \leq 5.5$ V 4/ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Data hold after $\overline{WE}$ high	t_{WHDX}	See figure 10	9,10,11	All	50		ns
Write enable pulse width	t_{WLWH}	See figure 10	9,10,11	All	175		ns
$\overline{WE}$ high to $\overline{CE}$ hold time	t_{WHEH}	See figure 10	9,10,11	All	50		ns
VOE to $\overline{WE}$ setup time	t_{OHWL}	See figure 10	9,10,11	All	10		ns
VOE hold time	t_{WHOL}	See figure 10	9,10,11	All	10		ns
Erase cycle time	t_{WLWL} 9/	See figure 10	9,10,11	All		10	ms

1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OL} with the output under test connected to V_{OUT}.

2/ Tested initially and after any design changes that affect that parameter and guaranteed to the limits specified in table I.

3/ All pins not being tested are to be open.

4/ Output load: 1 TTL gate and $C_L = 100$ pF.
   Input rise and fall times: $= < 10$ ns.
   Input pulse levels: $V_{IL} = 0.0$ V, $V_{IH} = 3.0$ V.
   Timing measurement reference level:
      Inputs: 1.5 V.
      Outputs: 1.5 V.

5/ Tested by inference only, but guaranteed to the limits of table I.

6/ t_{WLWL} and t_{ELEL} for the byte write operations, define the time of the internal programming cycle (a maximum) this is equivalent to the minimum cycle time between write operations when neither data polling or toggle bit testing are employed.

7/ Data polling and toggle bit functionality, 100 percent tested ac parameters guaranteed by design.

8/ Data must be valid within 300 ns after the initiation of a write cycle.

9/ t_{WLWL} for the high voltage erase, defines the time of the internal programming cycle and is referenced in the above table to indicate a maximum limit, not an operation mode.

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DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444</td><td>SIZE
A</td><td></td><td>5962-87649</td></tr>
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7</td></tr>
</table>

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.9 Processing EEPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacture prior to delivery.

3.9.1 Erasure of EEPROMs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.6 herein.

3.9.2 Programmability of EEPROMs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and table I herein.

3.9.3 Verification of state of EEPROMs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of reading the devices in accordance with the procedures and characteristics specified in 4.7. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and Inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply.

    a. Burn-in test (method 1015 of Mil-STD-883).

        (1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

        (2) T_A = +125°C, minimum.

        (3) Prior to burn-in, the devices shall be programmed with a topological alternating bit pattern. The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be removed from the lot.

    b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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c. An endurance test including a data retention bake, in accordance with method 1033 of MIL-STD-883, prior to burn-in (e.g., may be performed at wafer sort) shall be included as part of the screening procedure with the following conditions:

   (1) Method A.

       (a) Cycling may be block, byte, or page at equipment room ambient temperature and shall cycle all bytes for a minimum 10,000 cycles.

       (b) After cycling, perform a high temperature unbiased storage for 2 hours 30 minutes at +250°C minimum, or 24 hours at +170°C minimum, or 72 hours at +150°C minimum. All devices shall be programmed with a charge on all memory cells in each device, such that the cell will read opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern).

       (c) Read the data retention pattern and test using subgroups 1, 7, and 9 minimum, (e.g., high temperature equivalent subgroups 2, 8A, and 10 may be used) after cycling and bake, but prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure and shall be removed from the lot.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

   a. Tests shall be as specified in table II herein.

   b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

   c. Subgroup 4 (C_I and C_0 measurements) shall be measured only for the initial test and after process or design changes which may affect input and output capacitance.

4.3.2 Groups C and D inspections.

   a. End-point electrical parameters shall be as specified in table II herein.

   b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

       (1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

       (2) T_A = +125°C, minimum.

       (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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SEE NOTE 4
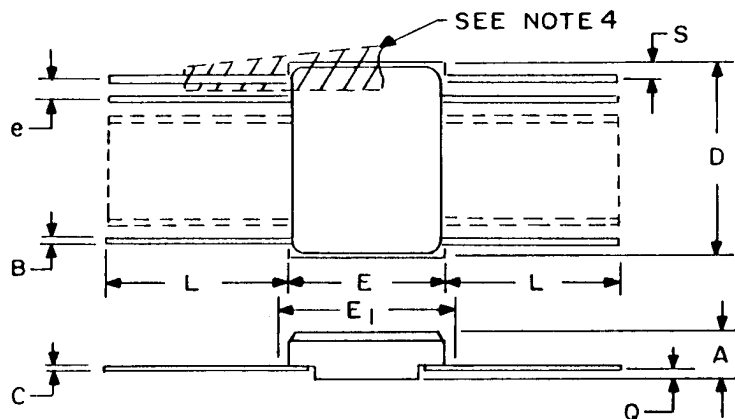
Parameter	Minimum	Maximum
A	.082 (2.08)	.118 (3.00)
B	.015 (0.38)	.022 (0.56)
C	.003 (0.08)	.009 (0.23)
D	.712 (18.08)	.740 (18.80)
E	.404 (10.26)	.416 (10.57)
E1		.420 (10.67)
e	.050 (1.27)	bsc
L	.250 (6.35)	.370 (9.40)
Q	.010 (0.25)	.040 (1.02)
S		.045 (1.14)

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Millimeters are in parentheses.
4. Index area: a notch, tab, or pin one identification mark shall be located within the shaded area shown.
5. E1 allows for alloy brazed overrun.
6. Dimensions B and C increase by 3 mils maximum limit if tin plate/solder dip lead finish is applied.

FIGURE 1. Case outline Z.

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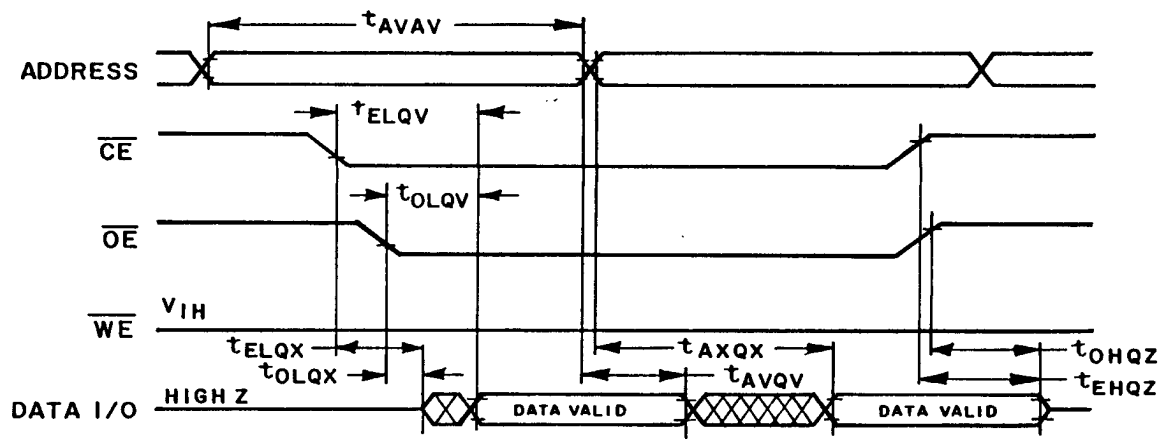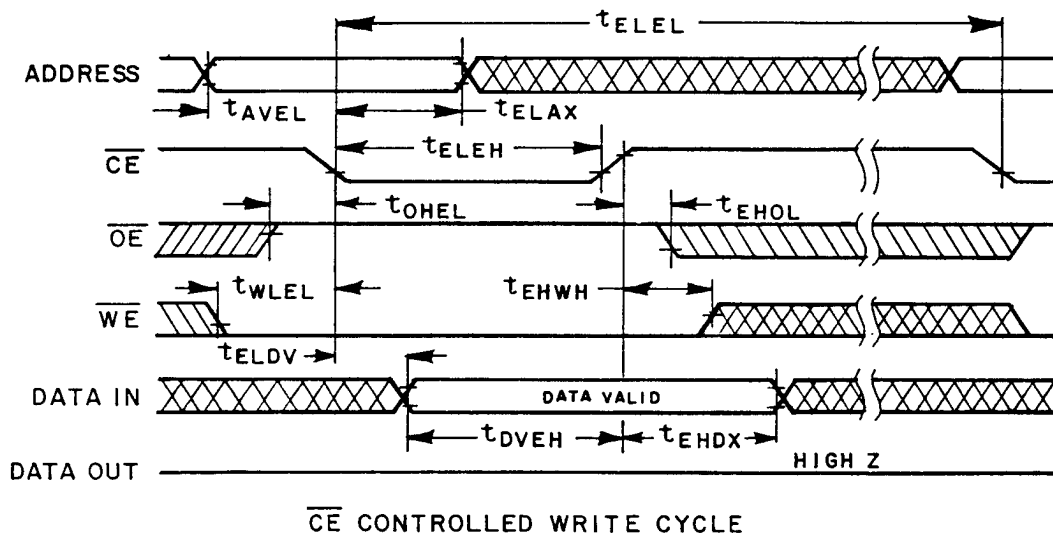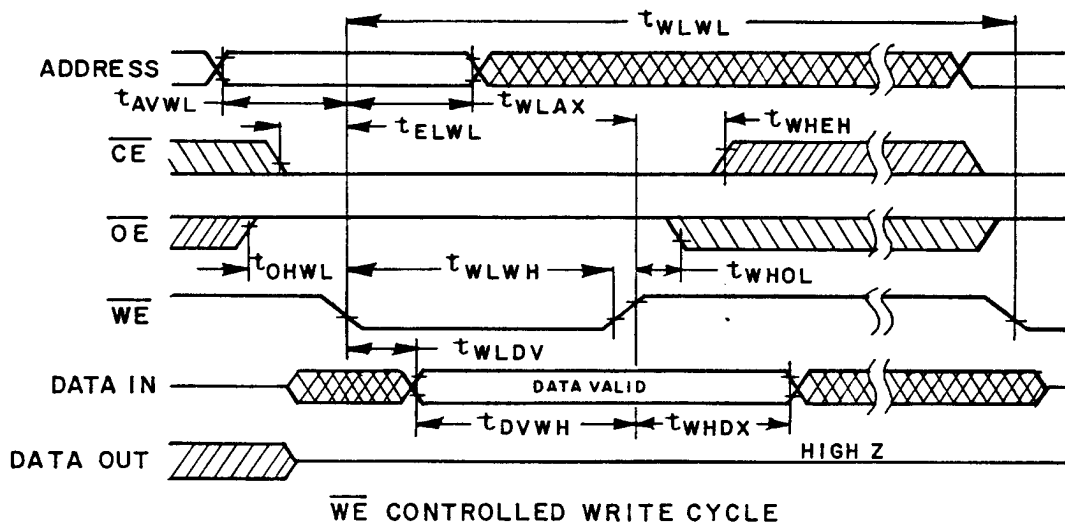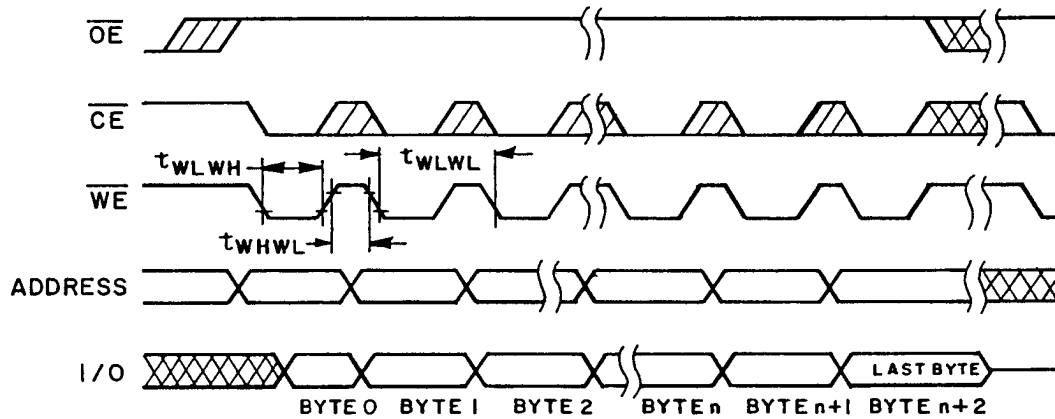SEP 87

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Cases X and Z

A_{14}	1	28	V_{CC}
A_{12}	2	27	$\overline{WE}$
A_7	3	26	A_{13}
A_6	4	25	A_8
A_5	5	24	A_9
A_4	6	23	A_{11}
A_3	7	22	$\overline{OE}$
A_2	8	21	A_{10}
A_1	9	20	$\overline{CE}$
A_0	10	19	I/O_7
I/O_0	11	18	I/O_6
I/O_1	12	17	I/O_5
I/O_2	13	16	I/O_4
V_{SS}	14	15	I/O_3

Case Y

Top: A_7 A_{12} A_{14} NC V_{CC} $\overline{WE}$ A_{13}
Pins: 4 3 2 1 32 31 30

Left			Right
A_6	5	29	A_8
A_5	6	28	A_9
A_4	7	27	A_{11}
A_3	8	26	NC
A_2	9	25	$\overline{OE}$
A_1	10	24	A_{10}
A_0	11	23	$\overline{CE}$
NC	12	22	I/O_7
I/O_0	13	21	I/O_6

Bottom pins: 14 15 16 17 18 19 20
Bottom: I/O_1 I/O_2 V_{SS} NC I/O_3 I/O_4 I/O_5

FIGURE 2. Terminal connections.

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and write inhibit	High Z	Standby
X	L	X	Write inhibit	---	---
X	X	H	Write inhibit	---	---

FIGURE 3. Truth table.
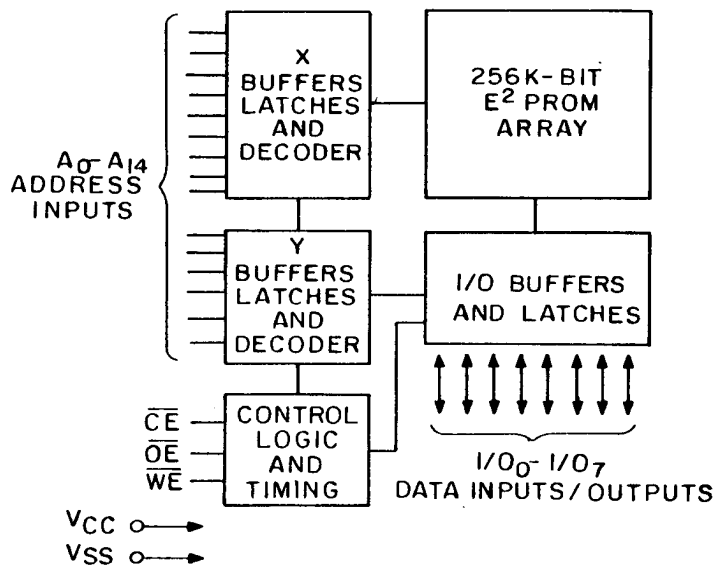
FIGURE 4. Block diagram.

FIGURE 5.   Switching waveform (read operation).

WE CONTROLLED WRITE CYCLE

CE CONTROLLED WRITE CYCLE

FIGURE 6. Switching waveforms (byte write cycle).

*For each successive write within the page write operation, $A_5 - A_{12}$ should be the same or writes to an unknown address could occur.
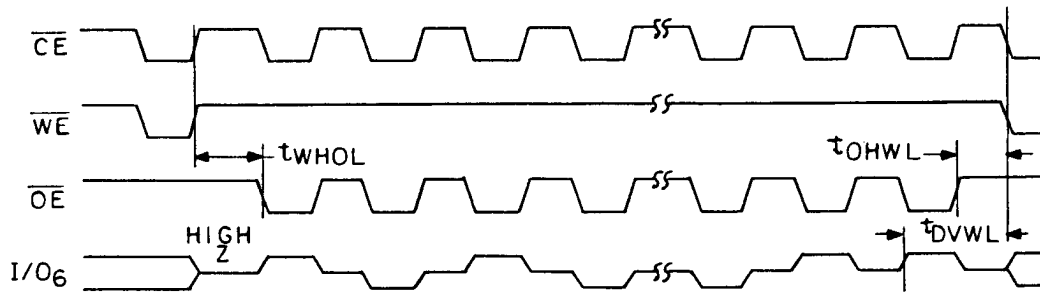
FIGURE 7. Switching waveform (page write operation).
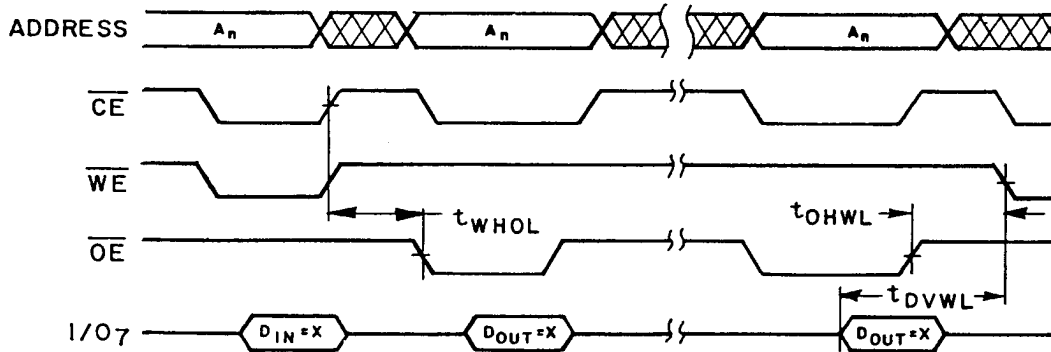
FIGURE 8. Switching waveform (data polling).

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$\overline{CE}$

$\overline{WE}$

t_{WHOL} t_{OHWL}

$\overline{OE}$

HIGH Z t_{DVWL}

I/O_6

*Beginning and ending state of I/O_6 will vary.

FIGURE 9. Switching waveform (toggle bit testing).

V_{CC} INPUT V_{CC} = 5 V ± 10%

V_{OE} = 18 V MIN, AND 20 V MAX

$\overline{OE}$ t_{OHWL} t_{WLWH} t_{WHOL}

$\overline{WE}$

t_{ELWL} t_{WHEH}

$\overline{CE}$

t_{DVWL} t_{WHDX}

I/O_{0-7} t_{WLWL}
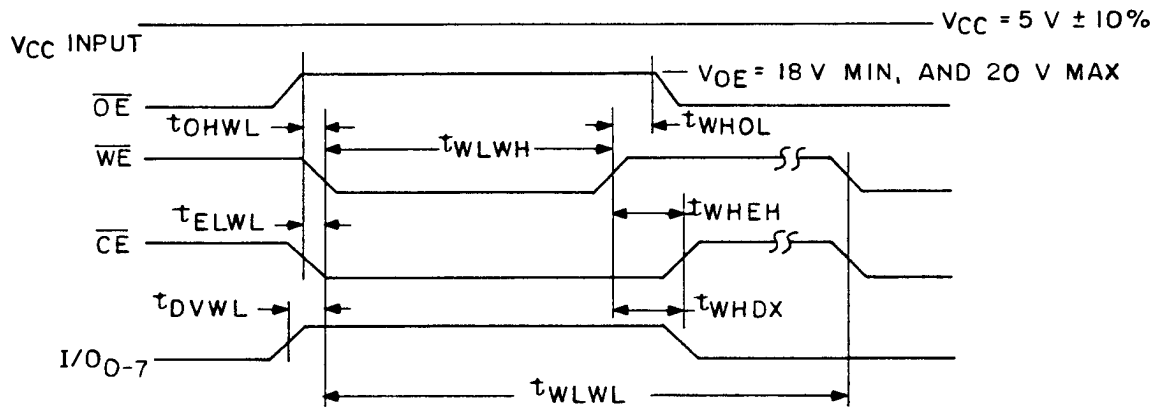
NOTES:
1. All timing is referenced to $\overline{WE}$ edges.
2. V_{OE} must be stable minimum 10 ns prior to $\overline{WE}$ low conditions and held stable minimum 10 ns after $\overline{WE}$ high condition.

FIGURE 10. Switching waveform (chip erase).

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TABLE II. Electrical test requirements. 1/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7, 8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3,7,8,9, 10,11

1/ Any subgroups at the same temperature may be combined when using a multifunction tester.

*   PDA applies to subgroups 1 and 7.

** Indicates that subgroup 4 will only be performed during initial qualification or after any design or process changes that may affect capacitance.

c. An endurance test, in accordance with method 1033 of MIL-STD-883, shall be added to group C, subgroup 1 inspection prior to performing the steady state life test. Cycling may be block, byte, or page on devices passing group A after completion of the requirements of 4.2 herein. The following conditions shall be met:

(1) All bytes shall be cycled for a minimum 10,000 cycles at equipment room ambient temperature.

(2) After cycling, perform a high temperature unbiased storage for 2 hours 30 minutes at +250°C minimum, or 24 hours at +170°C minimum, or 72 hours at +150°C minimum. All devices shall be programmed with a charge on all memory cells in each device, such that the cell will read opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern).

(3) Read the data retention pattern and test using subgroups 1, 7, and 9 minimum, (e.g., high temperature equivalent subgroups 2, 8A, and 10 may be used) after cycling and bake, but prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure and shall be removed from the lot.

4.4 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.4.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

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4.5 Programming procedure method A1. The waveforms and timing relationships shown on figures 6 and 7 and the conditions specified in table I shall be adhered to.

4.5.1 Byte write operation. Information introduced by selectively programming "L" (logic 0 level) or "H" (logic 1 level) into the desired bit locations. A programmed "L" can be changed to a "H" by programming an "H", no erasure is necessary.

4.5.2 Page mode write operation. During a page mode write cycle, the bits of the selected bytes can be "H" or "L", and addresses within the page that do not require data change should not be selected, therefore, a page mode write cycle can be used to write data into two to sixty-four address locations within the same page.

4.5.3 Data polling. During the internal programming cycle after either a byte or page write operation, an attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0XXX XXXX and read data = 1XXX XXXX). Once the programming cycle has completed, I/O_7 will reflect true data, (i.e., write data = 0XXX XXXX and read data = 0XXX XXXX). The waveforms and timing relationships shown on figures 6, 7, and 8, and conditions specified in table I shall be adhered to.

4.5.4 Toggle bit operation. While the internal programming cycle after either a byte or page write operation is in progress, the toggle bit, I/O_6, will alternate between "L" and "H" each time the device is read. Completion of the internal cycle is indicated when two successive read operations show I/O_6 either "L" or "H" for both reads. The waveforms and timing relationships shown on figures 6, 7, and 9, and the conditions specified in table I shall be adhered to.

4.6 Erasing procedure. There are two forms of erasure, byte erasure and chip erasure, whereby the bits of the address selected will be erased.

4.6.1 Byte erasure. Byte erasure is performed in accordance with the waveforms and timing relationships shown on figure 6 and the conditions specified in table I.

4.6.2 High voltage chip erasure. High voltage chip erasure is performed in accordance with the waveforms and timing relationships shown on figure 10 and the conditions specified in table I.

4.7 Read mode operation. The device is in the read mode whenever the $\overline{CE}$ and $\overline{OE}$ pins are at V_{IL}, and the $\overline{WE}$ pin is at V_{IH}. The waveforms and timing relationships shown on figure 5 and the test conditions specified in table I shall apply.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8764901XX	60395	X28256DMB-35	
5962-8764901YX	60395	X28256EMB-35	
5962-8764901ZX	60395	X28256FMB-35	
5962-8764902XX	60395	X28256DMB-30	
5962-8764902YX	60395	X28256EMB-30	
5962-8764902ZX	60395	X28256FMB-30	
5962-8764903XX	60395	X28256DMB-25	
5962-8764903YX	60395	X28256EMB-25	
5962-8764903ZX	60395	X28256FMB-25	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
60395	Xicor, Incorporated 851 Buckeye Court Milpitas, CA 95035

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