REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change Table I, footnotes, t_{PLH}, t_{PHL}. Add figure 3. Editorial changes throughout.	88-04-04	M. A. Frye
B	Changes IAW NOR 5962-R201-92. -tvn	95-05-11	Tim Noh
C	Add "C" case. Revise per current boilerplate. -ljs	98-01-22	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV										
SHEET										
REV										
SHEET										
REV STATUS	REV	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9

PMIC N/A	PREPARED BY Monica L. Poelking	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Raymond Monnin	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, DIGITAL, ADVANCED LOW-POWER SCHOTTKY TTL, AND GATE, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 87-08-19	
	REVISION LEVEL C	SIZE A; CAGE CODE **67268**; **5962-86842**
		SHEET 1 OF 9

DSCC FORM 2233
APR 97

5962-E158-98

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-86842	01	D	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALS08	Quadruple two-input positive AND gate

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat package
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc minimum to 7.0 V dc maximum
Input voltage range (V_I)	-1.5 V dc at -18 mA to 7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (PD) per device 1/	22 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD 1835
Junction temperature (T_J)	175°C
Operating free-air temperature range	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	+2.0 V
Maximum low level input voltage (V_{IL})	
T_C = +125°C	0.7 V dc
T_C = -55°C	0.8 V dc
T_C = +25°C	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Timing waveforms and test circuit. The test circuit and timing requirements shall be as specified on figure 3.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ unless otherwise specified 1/ 2/		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	$V_{IH} = 2.0$ V $V_{CC} = 4.5$ V	$V_{IL} = 0.8$ V	1, 3	2.5		V
		$I_{OH} = -0.4$ mA 3/ 4/	$V_{IL} = 0.7$ V	2			
Low level output voltage	V_{OL}	$V_{IH} = 2.0$ V $V_{CC} = 4.5$ V	$V_{IL} = 0.8$ V	1, 3		0.4	V
		$I_{OL} = 4.0$ mA 4/ 5/	$V_{IL} = 0.7$ V	2			
Input clamp voltage	V_{IC}	$V_{CC} = 4.5$ V $I_{IN} = -18$ mA		1, 2, 3		-1.5	V
High level input current	I_{IH1}	$V_{CC} = 5.5$ V $V_{IN} = 2.7$ V All other inputs = 0.0 V		1, 2, 3		20	µA
	I_{IH2}	$V_{CC} = 5.5$ V $V_{IN} = 7.0$ V All other inputs = 0.0 V		1, 2, 3		100	µA
Low level input current	I_{IL}	$V_{CC} = 5.5$ V $V_{IN} = 0.4$ V All other inputs = 4.5 V		1, 2, 3		-0.1	mA
Output current	I_O	$V_{CC} = 5.5$ V $V_{OUT} = 2.25$ V 6/		1, 2, 3	-20	-112	mA
High level supply current	I_{CCH}	$V_{CC} = 5.5$ V $V_{IN} \geq 4.5$ V (All inputs)		1, 2, 3		2.4	mA
Low level supply current	I_{CCL}	$V_{CC} = 5.5$ V $V_{IN} \leq 0.4$ V (All inputs)		1, 2, 3		4.0	mA
Functional tests		See 4.3.1c 7/		7, 8A ,8B			
Propogation delay time A, B to Y	t_{PHL}	$V_{CC} = 4.5$ V to 5.5 V $C_L = 50$ pF		9, 10, 11	3	12.5	ns
	t_{PLH}	$R_L = 500\Omega$ 8/ See Figure 3		9, 10, 11	4	14	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Unused inputs that do not directly control the pin under test must be ≥ 2.5 V or ≤ 0.4 V.

2/ Unused inputs shall not exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.

3/ One input to gate under test must be = V_{IH}; the other inputs shall be ≥ 2.0 V.

4/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper output state, the test must be performed with each input being selected as the V_{IL} maximum or V_{IH} minimum input.

5/ One input to gate under test must be = V_L, the other inputs shall be ≥ 2.0 V.

6/ The output conditions have been chosen to produce a current that closely approximates one-half of the true short circuit output current, I_{OS}. Not more than one output will be tested at a time and the duration of the test condition shall not exceed one second.

7/ Functional tests shall be conducted at input test conditions of $0.0\ V \leq V_{IIL} \leq V_{OL}$ and $V_{OH} \leq V_{IH} \leq V_{CC}$.

8/ The propagation delay limits are based on single output switching. Unused inputs = 3.5 V or ≤ 0.3 V.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Device type	01	01
Case outlines	C & D	· 2
Terminal number	Terminal symbol	Terminal symbol
1	1A	NC
2	1B	1A
3	1Y	1B
4	2A	1Y
5	2B	NC
6	2Y	2A
7	GND	NC
8	3Y	2B
9	3A	2Y
10	3B	GND
11	4Y	NC
12	4A	3Y
13	4B	3A
14	V_{CC}	3B
15	- - -	NC
16	- - -	4Y
17	- - -	NC
18	- - -	4A
19	- - -	4B
20	- - -	V_{CC}

NC = no connection

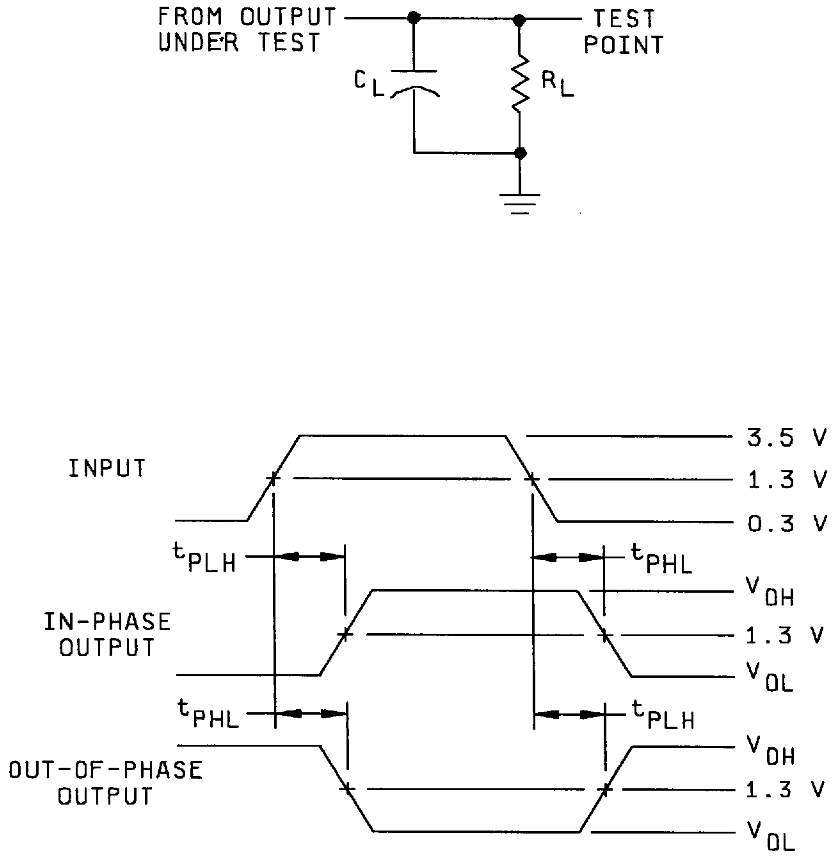
FIGURE 1. Terminal connections.

Each Gate		
INPUTS		OUTPUT
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

Positive logic Y = AB
H = high level voltage
L = Low level voltage

FIGURE 2. Truth table.

STANDARD **MICROCIRCUIT DRAWING** DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-86842**
		REVISION LEVEL C	SHEET **6**



NOTES:

1. C_L includes probe and jig capacitance.
2. All input pulses have the following characteristics: PRR ≤ 10 MHz., duty cycle = 50%, $t_r = t_f = 3$ ns ± 1 ns.
3. The outputs are measured one at a time with one input transition per measurement.

FIGURE 3. Timing waveforms and test circuit.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-86842**
		REVISION LEVEL C	SHEET 7

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A = +125°C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7, 8A, and 8B shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) $T_A = +125°C$, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 98-01-22

Approved sources of supply for SMD 5962-86842 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Replacement military specification part number
5962-8684201CA	01295	SNJ54ALS08J	
5962-8684201DA	01295	SNJ54ALS08W	M38510/37401BDA
5962-86842012A	01295	SNJ54ALS08FK	M38510/37401B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated 13500 N Central Expressway P.O. Box 655303 Dallas, TX 75265 POC: I-20 at FM 1788 Midland, TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.