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SP8802 3.3GHZ ÷ 2 Fixed Modulus Divider Advance Information

Features

- Very High Speed Operation 3.3GHz
- Silicon Technology for low Phase Noise (Typically better than -140dBc/Hz at 10kHz)
- Specified Over the Full Military Temperature Range
- Low Power Dissipation 420mW (typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Available as DESC SMD 5962-9066101MPA

DS2111 ISSUE 7.2 June 1999 Ordering Information SP8802/A/DG Military temperature range DES9066101/AC/DGAZ (SMD)

Thermal Characteristics

 $\theta ja = 150^{\circ}C/W$ $\theta jc = 50^{\circ}C/W$

Absolute Maximum Ratings

Supply voltage V _{cc}	6.5V
Clock Input voltage	2.5V p-p
Storage temperature range	-65°C to +150°C
Junction temperature	+175°C

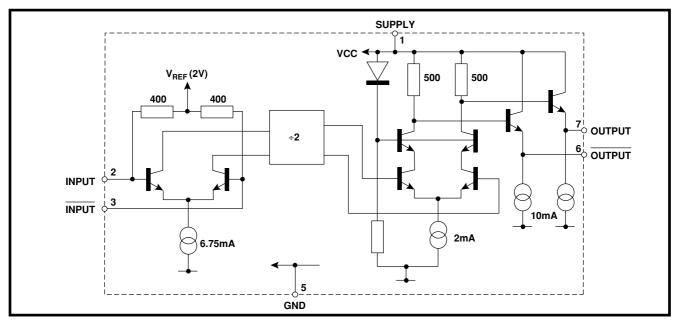


Figure 1 SP8802 Block diagram

Description

The SP8802 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current source for the emitter

follower outputs

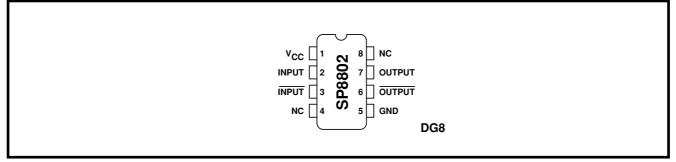


Figure 2 Pin connections

Electrical Characteristics

Guaranteed over the temperature range T_{amb} -55°C to +125°C (see note) and supply voltage range 4.75V to 5.25V. Tested at T_{amb} = -55°C and +100°C, V_{CC} = 4.75V and 5.25V.

Characteristic	Pin		Value		Units	Conditions					
Characteristic		Min	Min Typ		Units	Contantionic					
Supply current	1		84	100	mA	$V_{cc} = 5V$					
Input sensitivity 0.65GHz to 2.8GHz	2, 3			175	mV	RMS sinewave					
3.3GHz				400	mV	measured in 50 ohm system.					
Input impedance	2, 3		50		Ω	See Figs. 3 & 4					
(series equivalent)			2		рF						
Output Voltage with fin = 1000MHz	6, 7	0.8	1		Vp-p	$V_{\rm CC} = 5V$					
Output Voltage with f = 3GHz	6, 7		0.35		Vp-p	V_{cc}° = 5V load as Fig. 4					
""											

NOTE: Devices must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at T_{amb}>100°C.

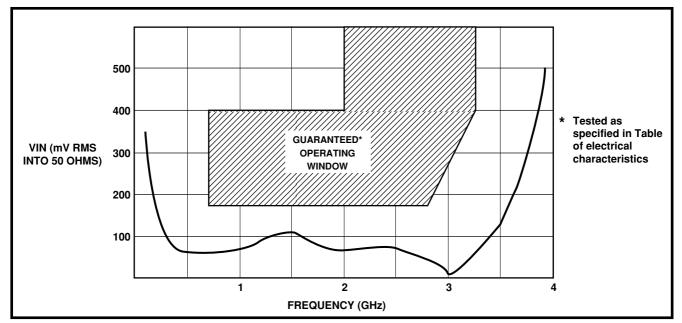


Figure 3 Typical input sensitivity

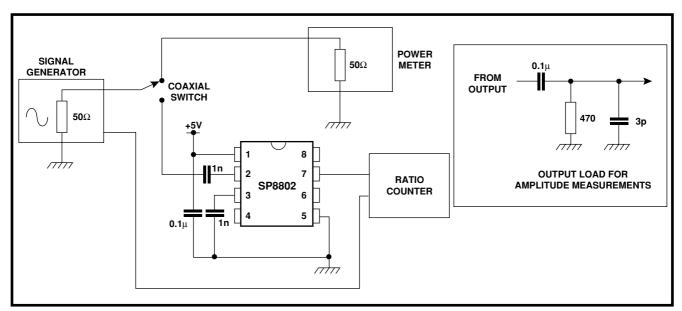


Figure 4 Test circuit

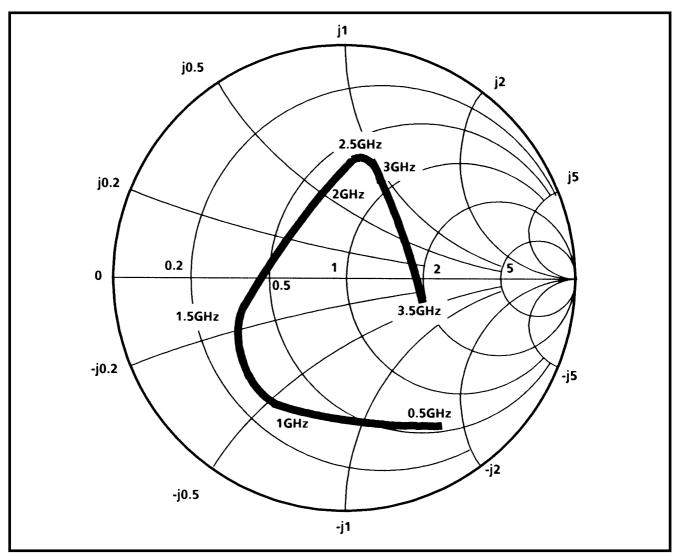


Figure 5 Typical input impedance

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		Í						JSEATING PLANE	<u></u>	J	" Leads " spacing	/		Pin 1 Ref. notch	:			
	,					Nomi	$\frac{1}{1}$		_لر	J —								
		SEMICONDUCTOR				eA Nominal Centres	>			 	m							
		DG /	Previous package codes		This drawing	S			` ⊳									
		\cap	des		supers			NOTE		2						Symbol		
GPDO		(Glass Seal Ceramic)	Package Outline for	Package Code	supersedes 418/ED/39501/001 (Swindon)			RECTANGUL	040	Pin feat	1.14 0.36 0.58 15	54 B	7.62) 51 5.08	MIN Nominal MAX	Altern. Dimensions		
GPDUUZ/U	0100	\bigcirc	e for 8 lead DIL	DH)1/001 (Swindon)			GULAR		features		0.100 BSC:	0.300	0 020	MIN Nominal MAX	Control Dimensions in inches		



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