TFT LCD Approval Specification

MODEL NO.: N154C1-L03

Customer : _____

Approved by : _____

Note :

記錄	工作	審核	角色	投票
2007-03-23 17:28:45 CST	Approve by Dept. Mgr.(QA RA)	tomy_chen(陳永一 /52720/54140/43150)	Department Manager(QA RA)	Accept
2007-03-21 17:21:42 CST	Approve by Director	teren_lin(林添仁 /56910/36064)	Director	Accept

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 0.0	May. 10. '06	All	All	Tentative specification first issued.
Ver 1.0	Jun. 15. '06	4	1.5	Mechanical Specification - depth
		6	2.2.2	Backlight Unit – lamp current, lamp frequency
		7	3.1	TFT LCD Module – power supply current
		9	3.2	Backlight Unit
		12	5.1	TFT LCD Module – Note(1) connector part no.
		13	5.2	Backlight Unit – connector pin definition
		18	6	Add Inverter Specification
		24	8.1	Test Conditions
		24	8.2	Optical Specifications
		32	11.3	Carton Label
Ver 3.0	Aug. 15.'06	16	5.5	EDID Data Structure
Ver 3.1	Aug. 24.'06	8	3.1	Electrical Characteristics
		12	4.1	Block Diagram
		13	5.1	Input Terminal Pin Assignment
		23	7.1	Input Signal Timing Specifications
Ver 3.2	Feb. 27.'07	15	5.5	EDID Data for MGD-Lite Project
		19	6.4.2	Electrical characteristics
Ver 3.3	Mar.21.'07	9	3.2	Update BLU power consumption and note.(4)
		18	6.1	Update inverter specification.
		21	6.4.2	Update Brightness control
		31	11.1	Update CMO label and add PPID label

1 GENERAL DESCRIPTION

1.1 OVERVIEW

N154C1-L03 is a 15.4" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface. This module supports 1440 x 900 WXGA+ mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is not built in.

1.2 FEATURES

- Thin and light weight
- WXGA+ (1440 x 900 pixels) resolution
- DE (Data Enable) only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 2 pixel/clock
- Support EDID Structure Version 1.3

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Outline Dimension	344(W) x 222 (H)	mm	(1)
Active Area	331.56 (H) x 207.225 (V)	mm	
Bezel Opening Area	335 (H) x 210.7 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1440 x R.G.B. x 900	pixel	-
Pixel Pitch	0.23025 (H) x 0.23025 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Glare	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	343.5	344	344.5	mm	(1)
	Vertical(V)	221.5	222	222.5	mm	
	Depth(D)	---	---	6.3	mm	
Weight		---	530	545	g	-
I/F connector mounting position		The mounting inclination of the connector makes the screen center within ±0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

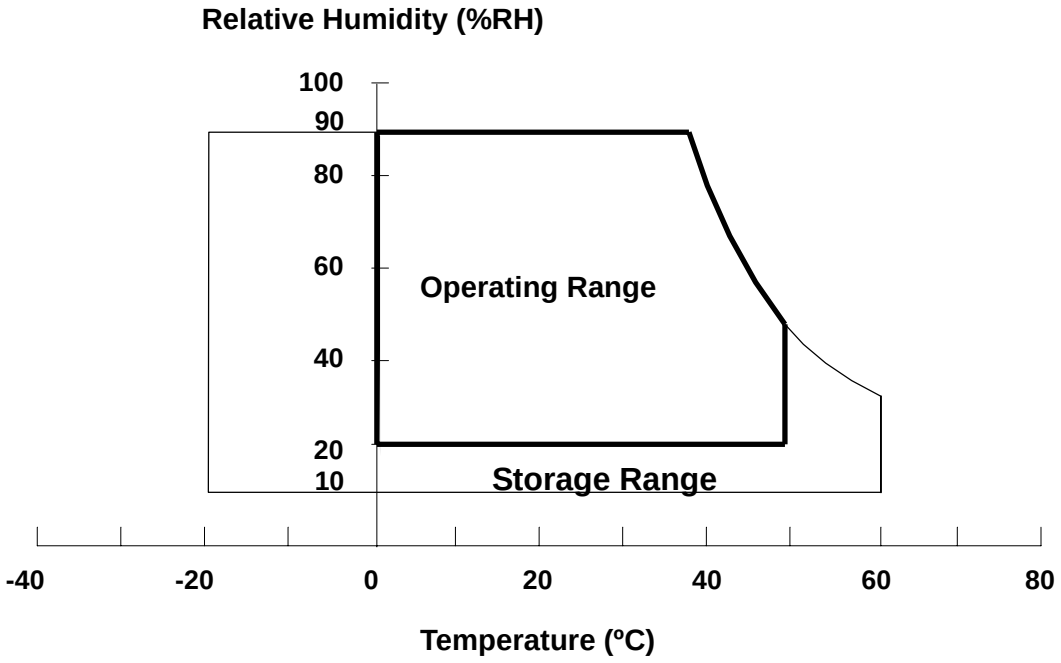
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	220/2	G/ms	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 50 ºC max.

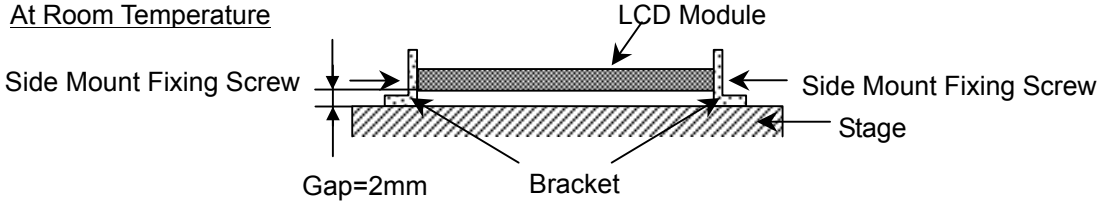


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (220G / 2ms) is half Sine Wave,.

Note (4) 10~200 Hz, 0.5hr/cycle 1cycle for X,Y,Z

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	Vcc+0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	-	2.5K	V_{RMS}	(1), (2), I_L = 6.0 mA
Lamp Current	I_L	2.0	7.0	mA_{RMS}	(1), (2)
Lamp Frequency	F_L	45	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to Section 3.2 for further information).

3 ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

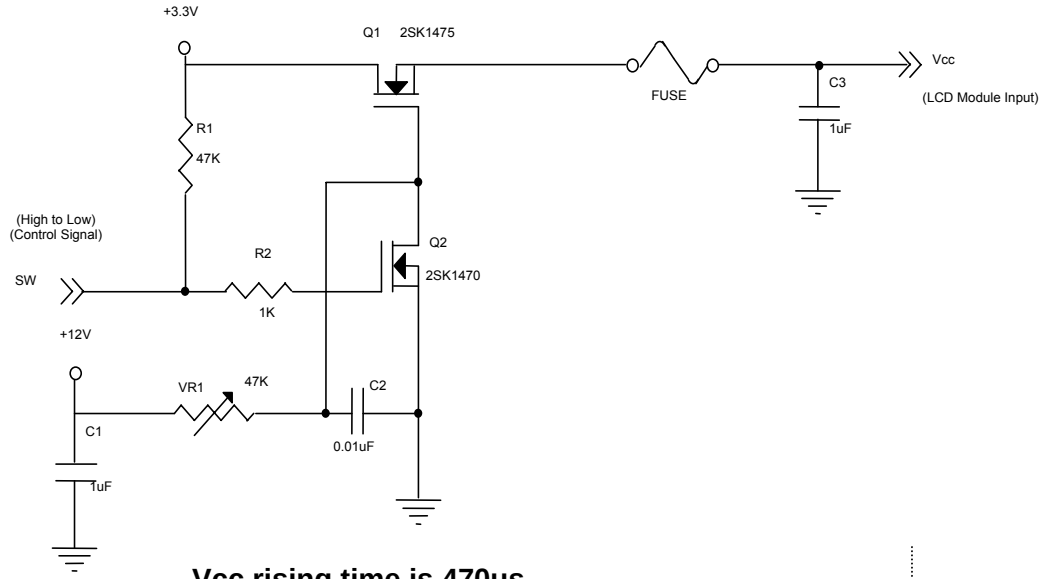
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	3.0	3.3	3.6	V	-
Permissive Ripple Voltage		V_{RP}		50		mV	-
Rush Current		I_{RUSH}			1.5	A	(2)
Initial Stage Current		I_{IS}			1.0	A	(2)
Power Supply Current	White	Icc		290	350	mA	(3)a
	Black			430	500	mA	(3)b
LVDS Differential Input High Threshold		$V_{TH(LVDS)}$			+100	mV	(5), V_{CM}=1.2V
LVDS Differential Input Low Threshold		$V_{TL(LVDS)}$	-100			mV	(5) V_{CM}=1.2V
LVDS Common Mode Voltage		V_{CM}	1.125		1.375	V	(5)
LVDS Differential Input Voltage		$\|V_{ID}\|$	100		600	mV	(5)
Terminating Resistor		R_T		100		Ohm	
Power per EBL WG		P_{EBL}	-	3.2	-	W	(4)

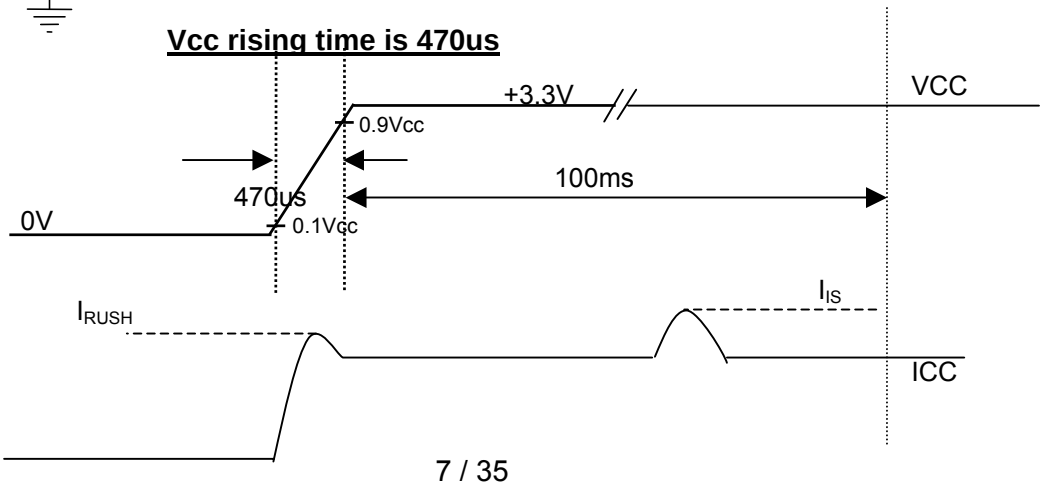
Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCC is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.





Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

b. Black Pattern

Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

(a) Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

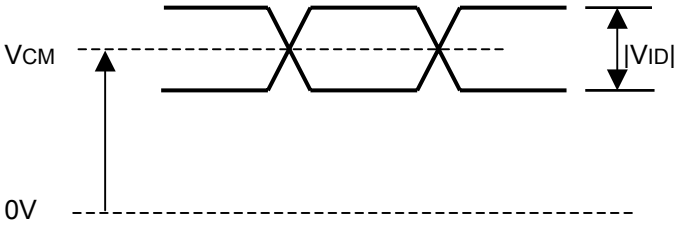
(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits.

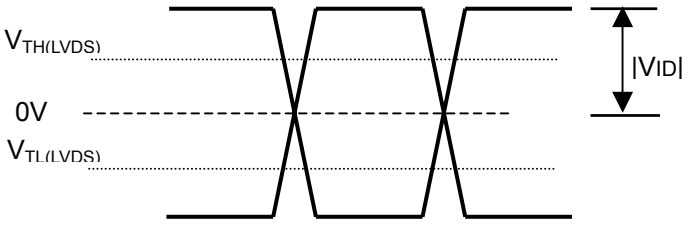
(d) The inverter used is provided from Sumida.

Note (5) The parameters of LVDS signals are defined as the following figures.

Single Ended



Differential

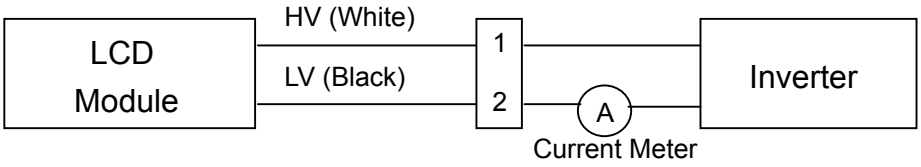


3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	657	730	803	V_{RMS}	I_L = 6.0 mA
Lamp Current	I_L	2.0	6.0	7.0	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	(1460) (25 °C)	V_{RMS}	(2)
		-	-	(1600) (0 °C)	V_{RMS}	(2)
Operating Frequency	F_L	45	55	80	KHz	(3)
Power Consumption	P_L	-	-	6.0	W	(4), I_L = 6.0 mA
Lamp Life Time	L_{BL}	15,000	-	-	Hrs	(5)

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage that must be larger than Vs should be applied to the lamp for more than 1 second after startup. Otherwise, the lamp may not be turned on normally.

Note (3) The lamp frequency may generate interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) P_{BL} = Inverter input power

Inverter input power is measured at 8th step(the max brightness step) @Vin=12V

Note (5) The lifetime of lamp is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I_L = 6.0 mA_{RMS} until one of the following events occurs:

(a) When the brightness becomes or lower than 50% of its original value.

(b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that the brightness is less than 70% compared to the center point.)

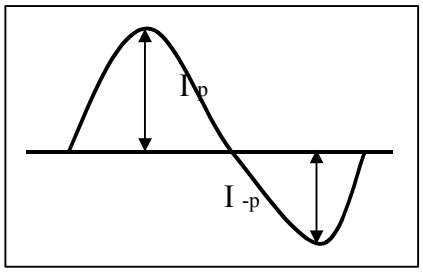
Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid generating too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below;

b. The distortion rate of the waveform should be within √2 ± 10%;

c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

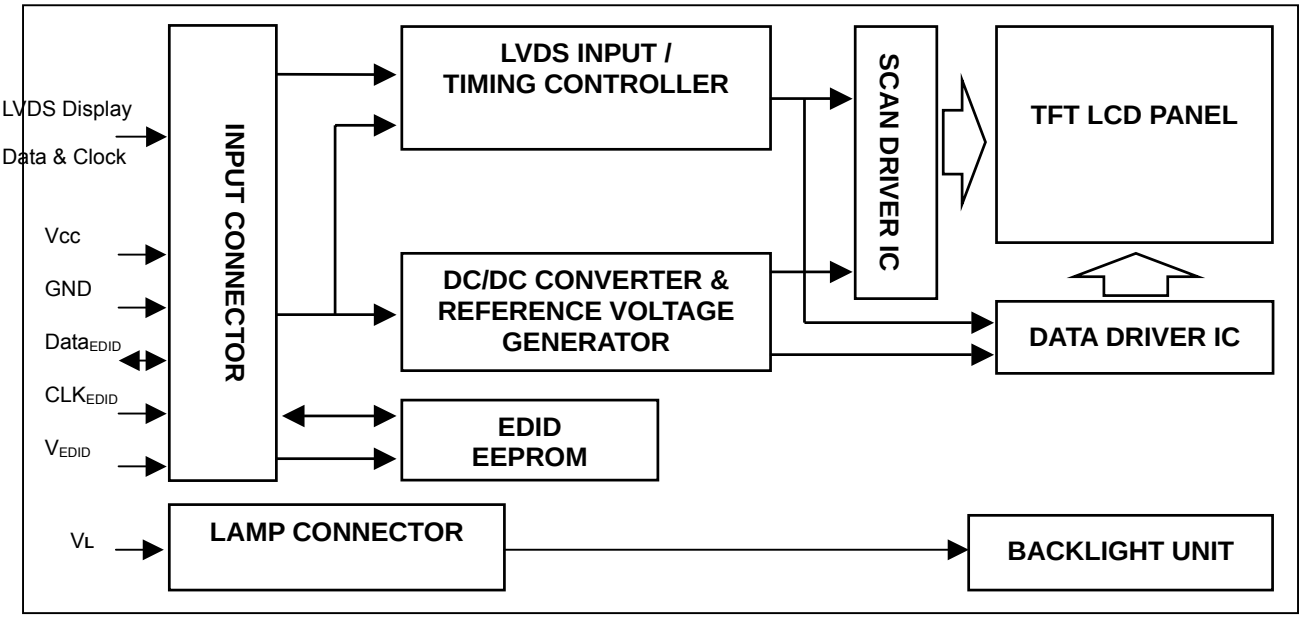
$$| I_p - I_{-p} | / I_{rms} * 100\%$$

* Distortion rate

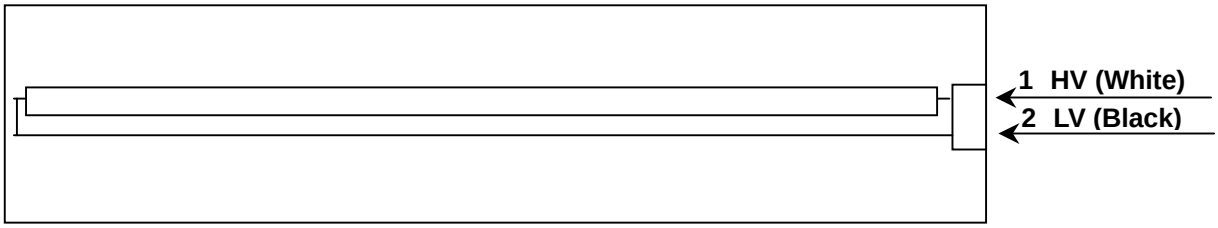
$$I_p \text{ (or } I_{-p}) / I_{rms}$$

4 BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



5 INPUT TERMINAL PIN ASSIGNMENT

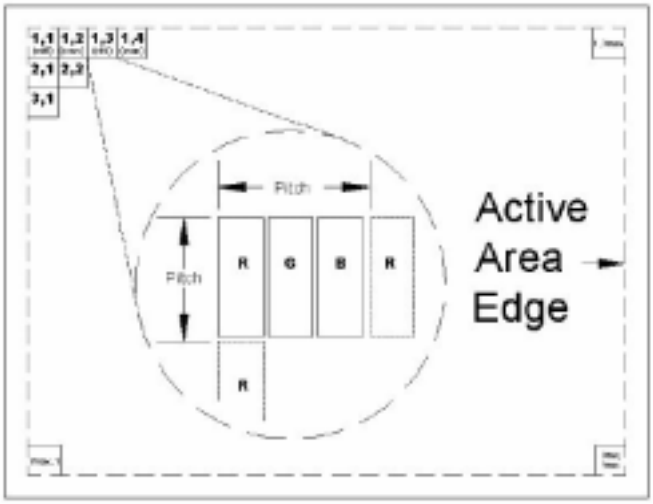
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V_{EDID}	DDC 3.3V Power		
5	NC	Non-Connection		
6	CLK_{EDID}	DDC Clock		
7	$DATA_{EDID}$	DDC Data		
8	RXO0-	LVDS Differential Data Input (Odd)	Negative	
9	RXO0+	LVDS Differential Data Input (Odd)	Positive	
10	Vss	Ground		
11	RXO1-	LVDS Differential Data Input (Odd)	Negative	
12	RXO1+	LVDS Differential Data Input (Odd)	Positive	
13	Vss	Ground		
14	RXO2-	LVDS Differential Data Input (Odd)	Negative	
15	RXO2+	LVDS Differential Data Input (Odd)	Positive	
16	Vss	Ground		
17	RXOC-	LVDS Clock Data Input (Odd)	Negative	
18	RXOC+	LVDS Clock Data Input (Odd)	Positive	
19	Vss	Ground		
20	RxE0-	LVDS Differential Data Input (Even)	Negative	
21	RxE0+	LVDS Differential Data Input (Even)	Positive	
22	Vss	Ground		
23	RxE1-	LVDS Differential Data Input (Even)	Negative	
24	RxE1+	LVDS Differential Data Input (Even)	Positive	
25	Vss	Ground		
26	RxE2-	LVDS Differential Data Input (Even)	Negative	
27	RxE2+	LVDS Differential Data Input (Even)	Positive	
28	Vss	Ground		
29	RXEC-	LVDS Clock Data Input (Even)	Negative	
30	RXEC+	LVDS Clock Data Input (Even)	Positive	

Note (1) Connector Part No.: JAE-FI-XB30SL-HF11 or equivalent

Note (2) User's connector Part No: JAE-FI-X30C2L or equivalent

Note (3) The first pixel is odd as shown in the following figure.



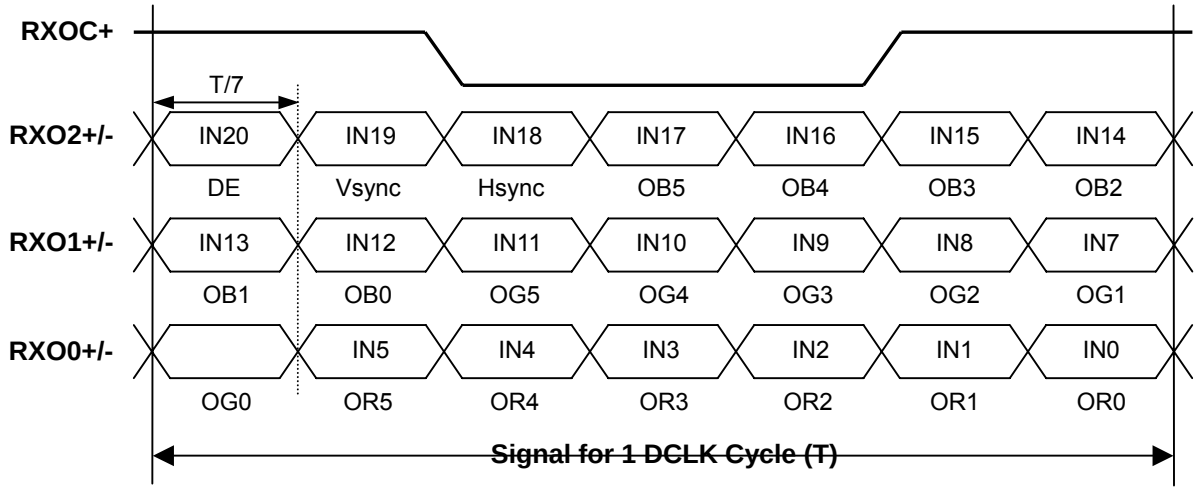
5.2 BACKLIGHT UNIT

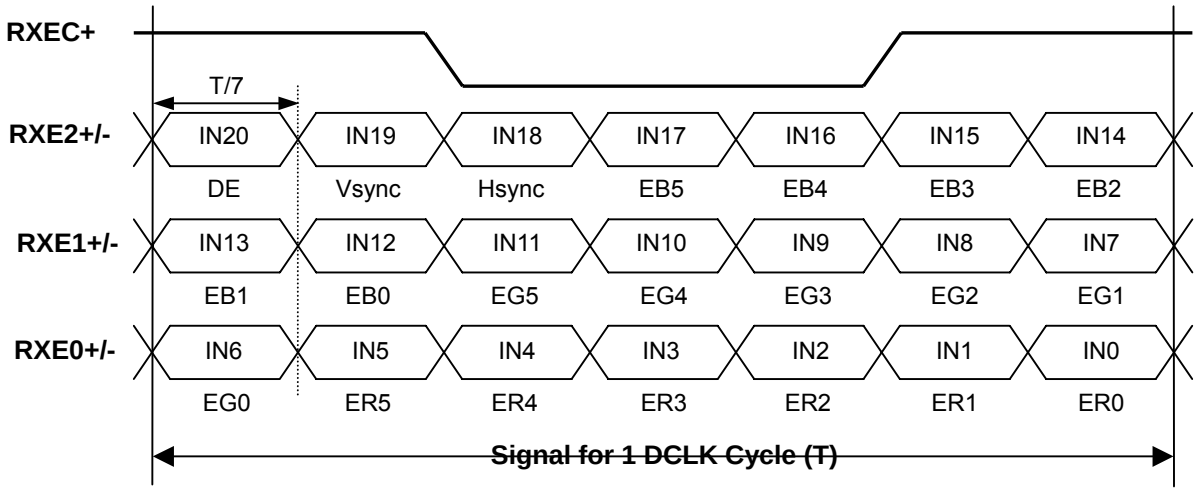
Pin	Symbol	Description	Color
1	HV	High Voltage	White
2	LV	Ground	Black

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL





5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name (“CMO”)	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N154C1-L03)	38	00111000
11	0B	ID product code (hex LSB first; N154C1-L03)	15	00010101
12	0C	ID S/N (fixed “0”)	00	00000000
13	0D	ID S/N (fixed “0”)	00	00000000
14	0E	ID S/N (fixed “0”)	00	00000000
15	0F	ID S/N (fixed “0”)	00	00000000
16	10	Week of manufacture (fixed week code)	30	00110000
17	11	Year of manufacture (fixed year code)	10	00010000
18	12	EDID structure version # (“1”)	01	00000001
19	13	EDID revision # (“3”)	03	00000011
20	14	Video I/P definition (“digital”)	80	10000000
21	15	Active area horizontal 33.156cm	21	00100001
22	16	Active area vertical 20.7225cm	15	00010101
23	17	Display Gamma (Gamma = ”2.2”)	78	01111000
24	18	Feature support (“Active off, RGB Color”)	0A	00001010
25	19	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0	D5	11010101
26	1A	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0	70	01110000
27	1B	Red-x (Rx = “0.593”)	97	10010111
28	1C	Red-y (Ry = “0.341”)	57	01010111
29	1D	Green-x (Gx = ”0.318”)	51	01010001
30	1E	Green-y (Gy = ”0.541”)	8A	10001010
31	1F	Blue-x (Bx = ”0.150”)	26	00100110
32	20	Blue-y (By = ”0.136”)	22	00100010
33	21	White-x (Wx = ”0.313”)	50	01010000
34	22	White-y (Wy = ”0.329”)	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer’s reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (“88.75MHz”, According to VESA CVT Rev1.1)	AB	10101011
55	37	# 1 Pixel clock (hex LSB first)	22	00100010
56	38	# 1 H active (“1440”)	A0	10100000
57	39	# 1 H blank (“160”)	A0	10100000
58	3A	# 1 H active : H blank (“1440 : 160”)	50	01010000
59	3B	# 1 V active (”900”)	84	10000100
60	3C	# 1 V blank (”26”)	1A	00011010
61	3D	# 1 V active : V blank (”900 :26”)	30	00110000
62	3E	# 1 H sync offset (”48”)	30	00110000
63	3F	# 1 H sync pulse width ("32”)	20	00100000
64	40	# 1 V sync offset : V sync pulse width (”3 : 6”)	36	00110110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”48: 32 : 3 : 6”)	00	00000000
66	42	# 1 H image size (”332 mm”)	4C	01001100
67	43	# 1 V image size (”207 mm”)	CF	11001111
68	44	# 1 H image size : V image size (”332 : 207”)	10	00010000
69	45	# 1 H boarder (”0”)	00	00000000
70	46	# 1 V boarder (”0”)	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	19	00011001
72	48	Detailed timing description # 2 Pixel clock (“73.75 MHz”, According to VESA CVT Rev1.1)	CF	11001111
73	49	# 2 Pixel clock (hex LSB first)	1C	00011100
74	4A	# 2 H active (“1440”)	A0	10100000
75	4B	# 2 H blank (“160”)	A0	10100000
76	4C	# 2 H active : H blank (“1440 : 160”)	50	01010000
77	4D	# 2 V active (”900”)	84	10000100
78	4E	# 2 V blank (”22”)	16	00010110
79	4F	# 2 V active : V blank (”900 : 22”)	30	00110000
80	50	# 2 H sync offset (”48”)	30	00110000
81	51	# 2 H sync pulse width (”32”)	20	00100000
82	52	# 2 V sync offset : V sync pulse width (”3 : 6”)	36	00110110
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width (”48 : 32 : 3 : 6”)	00	00000000
84	54	# 2 H image size (”332 mm”)	4C	01001100
85	55	# 2 V image size (”207 mm”)	CF	11001111

86	56	# 2 H image size : V image size (”332 : 207”)	10	00010000
87	57	# 2 H boarder (”0”)	00	00000000
88	58	# 2 V boarder (”0”)	00	00000000
89	59	Module "A" Revision = Example: 00, 01, 02, 03, etc.	00	00000000
90	5A	Detailed timing description # 2	00	00000000
91	5B	# 2 Flag	00	00000000
92	5C	# 2 Reserved	00	00000000
93	5D	# 2 FE (hex) defines ASCII string (Model Name “N154C1-L03”, ASCII)	FE	11111110
94	5E	# 2 Flag	00	00000000
95	5F	# Dell P/N "MC196" 1st character (“U”)	55	01010101
96	60	# Dell P/N " MC196" 1st character (“Y”)	59	01011001
97	61	# Dell P/N " MC196" 1st character (“3”)	33	00110011
98	62	# Dell P/N " MC196" 1st character (“7”)	37	00110111
99	63	# Dell P/N " MC196" 1st character (“1”)	31	00110001
100	64	LCD Supplier EEDID Revision #: "3"	33	00110011
101	65	# 2 1st character of name (“N”)	4E	01001110
102	66	# 2 2nd character of name (“1”)	31	00110001
103	67	# 2 3rd character of name (“5”)	35	00110101
104	68	# 2 4th character of name (“4”)	34	00110100
105	69	# 2 5th character of name (“C”)	43	01000011
106	6A	# 2 6th character of name (“1”)	31	00110001
107	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag:	FE	11111110
112	70	Flag	00	00000000
113	71	SMBUS value @ 10nits = 33d	21	00100001
114	72	SMBUS value @ 17nits = 45d	2D	00101101
115	73	SMBUS value @ 24nits = 54d	36	00110110
116	74	SMBUS value @ 30nits = 60d	3C	00111100
117	75	SMBUS value @ 60nits = 88d	58	01011000
118	76	SMBUS value @ 110nits = 120d	78	01111000
119	77	SMBUS value @ 180nits = 165d	A5	10100101
120	78	SMBUS value @ 250 nits = 228d	E4	11100100
121	79	Numbers of LVDS Recevier chip = 2	02	00000010
122	7A	BIST Enable: Yes = '01' No = '00' ("Yes")	01	00000001
123	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
124	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
125	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	48	01001000

6 INVERTER SPECIFICATION

6.1 Connector type

Input connector type: **LVC-D20SFYG** (HONDA)

Output connector: **JST SM02B-BHSS-1-TB** (JST)

6.2 Input connector pin assignment

Input Connector pin assignment:

Input connector		Comments
HONDA	**LVC-D20SFYG**	
Pin	**Function**	
1	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
2	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
3	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
4	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
5	GND	Ground
6	NC	No Connection
7	5VALW	This should be used as power source that stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
8	GND	Ground
9	SMB_DAT	SMBus interface for sending brightness & contrast information to the inverter/panel
10	SMB_CLK	SMBus interface for sending brightness & contrast information to the inverter/panel
11	GND	Ground
12	INV_PWM	System side PWM input signal for brightness control
13	GND	Ground
14	NC	No Connection
15	DIAG_LOOP	Diag pin for Dell testing. Pin15 & 20 must be connected electrically on the inverter board.
16	GND	Ground
17	5VALW	This should be used as power source that stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
18	5VALW	This should be used as power source that stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
19	NC	No Connection
20	DIAG_LOOP	Diag pin for Dell testing. Pin15 & 20 must be connected electrically on the inverter board.

Absolute maximum ratings

Items	Absolute max. ratings	Unit
INV_SRC (Voltage)	-1.0~23.5	V
FPBACK/SMB_CLK/SMB_DAT (Voltage)	-1.0~5.5	V

6.3 Output connector pin assignment

Pin	Name	Description
1	CFL-High	High-voltage output to the CCFL
2	CFL-Low	Low-voltage output to the CCFL

6.4 General electrical specification:

6.4.1Absolute maximum ratings

Items	Absolute max. ratings	Unit
INV_SRC (Voltage)	-1.0~23.5	V
FPBACK/SMB_CLK/SMB_DAT (Voltage)	-1.0~5.5	V

6.4.2 Electrical characteristics:

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Uint
1	Input Voltage	INV_SRC		7.5	14.4	21	V
2	Input Signal Level for 5VSUS	5VSUS		4.75	5	5.2	V
3	Input Signal Level for 5VALW	5VALW		4.75	5	5.2	V
4	Input Power	Pin(Max)	185nits@Vin=12V	-	-	4.6	W
5	Brightness Adjust (Lamp Current Control)	SMB_DAT	Control by SMBus(256 steps dimming control)	00H	-	FFH	-
6	Output Voltage	Vout	IL = 6.3mA(typ)	657	730	803	Vrms
7	Output Current	Iout (Min)	Vin=7.5V~21V SMB_DAT=00H Ta=25℃, after running 30 min.	1.5	1.8	2.1	mArms
		Iout (Max)	Vin=7.5V~21V SMB_DAT=FFH Ta=25℃, after running 30 min.	6	6.3	6.6	mArms
8	Operation Frequency	Freq	Vin=7.5V~21V	45	-	65	KHz
9	Burst mode frequency	f_B	Vin=7.5V~21V	200	-	220	Hz
10	Open Lamp Voltage	Vopen	No Load	1400	--	1600	Vrms
11	Striking Time	Ts	No Loadw	0.6	1	1.4	Sec
12	Efficiency	η	Vin=7.5V, SMB_DAT=FFH (RES LOAD=100K ohm)	80	-	-	%
13	Start and Delay Time		Vin=14.4V, SMB_DAT=00H	-	130	200	uS
14	Start –up time (Turn on delay time)		Vin=14.4V, SMB_DAT=FFH	-	-	0.1	Sec

- Input Voltage

  The operating input voltage of inverter shall be defined.

  The inverter shall ignite the CCFL lamp at minimum input voltage at any environment conditions.

- On/Off control

  Enable: At "**ON**" condition (FPBACK=Hi), enable the inverter.

  Disable: At "**OFF**" condition (FPBACK=Lo), disable the inverter.

- Quiescent current

  At the inverter "**OFF**" condition, input quiescent should be less than 0.1mA.

- Open lamp voltage

  The inverter start-up output voltage will be above "**Vopen**" for "**Ts**" minimum at any condition under specify until lamp to be ignited. The inverter should be shutdown if lamp ignition was failed in "**Ts**" maximum. The inverter shall be capable of withstanding the output connections open without component over-stress / fire / smoke /arc.

- Burst mode frequency

  The burst mode frequency should be in specification in any environment condition and electrical condition.

- Brightness control

  SM-BUS values for panel luminance are to be included in the on LCD board EEDID ROM chip table. The supplier will measure panel luminance in a system and define the SMBUS values for each of the 8 required luminance levels. The panel luminance, for which SMBUS values will be provided in the EEDID from byte # 113(hex #71), to byte # 120, (hex # 78), is show in the table below. The inverter supplier should provide these appropriate values to CMO.

Step Count	Step 1	Step 2	Step3	Step 4	Step 5	Step 6	Step 7	Step 8
Address	Byte 113	Byte 114	Byte 115	Byte 116	Byte 117	Byte 118	Byte 119	Byte 120
SM-Bus Data Value	33	45	54	60	88	120	165	228
Luminance (nits)	10	17	24	30	60	110	180	250

- Output ripple ratio

  Ripple ratio = 2 * (Ipeak - Ivalley) / (Ipeak + Ivalley) * 100%

  The Ripple ratio should be less than 5% and ripple frequency should be less than 200 Hz.

- Power up Overshoot & Undershoot

  Overshoot & Undershoot at power up should not exceed the following limits.

Vin	Output current Io(rms)	Io (dI) Overshoot/Undershoot	Settling time (dT)
0→Vin(min.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		
0→Vin(typ.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		
0→Vin(max.)	Io(max.)	150% / 50%	5 ms max.

	Io(min.)		

dI=Imax.-Io or dI=(Io-Imin.)/Io

- Output connections short protection

  The inverter shall be capable of withstanding the output connections short without damage or over-stress. And the inverter maximum input power shall be limited within 1W.

6.4.3 Mechanical Drawing

6.4.4 Other Information

- Safety
  - The inverter shall meet the requirement of “Limited current circuits” in paragraphs 2.4.1 in IEC60950. There is no fire/smoke while simulating the component of the inverter open/short test.
  - The Inverter AND panel must be UL certified with CB certificate and LCC (Limited Current Circuit) test and test reports from UL. Inverter panel combo must pass Dell Safety requirements.
- EMI

  The inverter must meet the radiated limitation requirement of CISPR22 class B, FCC-B and VCCI level II with 6dB margin minimum while the inverter operating in the complete system.
- Environment Regulation
  - Follow the RoHS requirement.
  - Fill in CMO’s official document <<Environmentally Conscious Products Questionnaire for Suppliers of Materials, Parts, and Products>> and turn in to CMO before CMO’s specification approval process.

- Dell’s other requirements
  1. The inverter must not emit any audible noise.
  2. Please refer to CMO’s official document. “General Inverter Specification for LCD Module” for other general information such as reliability test, safety and etc..
  3. Please also refer to DELL’s official document about inverter:
     - LCD Backlight Design Spec X00-04
     - DELL’s LCD Inverter Qualification Plan, Rev. A00
     - Prohibited Components
     - “Holy Stone(禾申堂)”’s products are prohibited.

7 INTERFACE TIMING

7.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

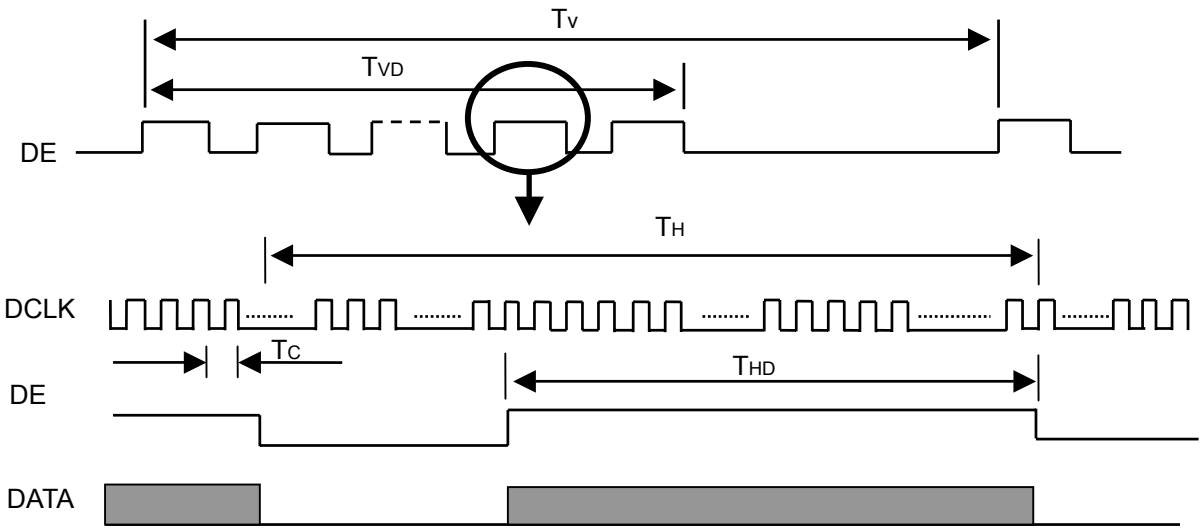
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	25	44.5	60	MHz	(2)
DE	Vertical Total Time	TV	910	926	1500	TH	-
	Vertical Active Display Period	TVD	900	900	900	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	26	TV-TVD	TH	
	Horizontal Total Time	TH	760	800	880	Tc	(2)
	Horizontal Active Display Period	THD	720	720	720	Tc	(2)
	Horizontal Active Blanking Period	THB	TH-THD	80	TH-THD	Tc	(2)

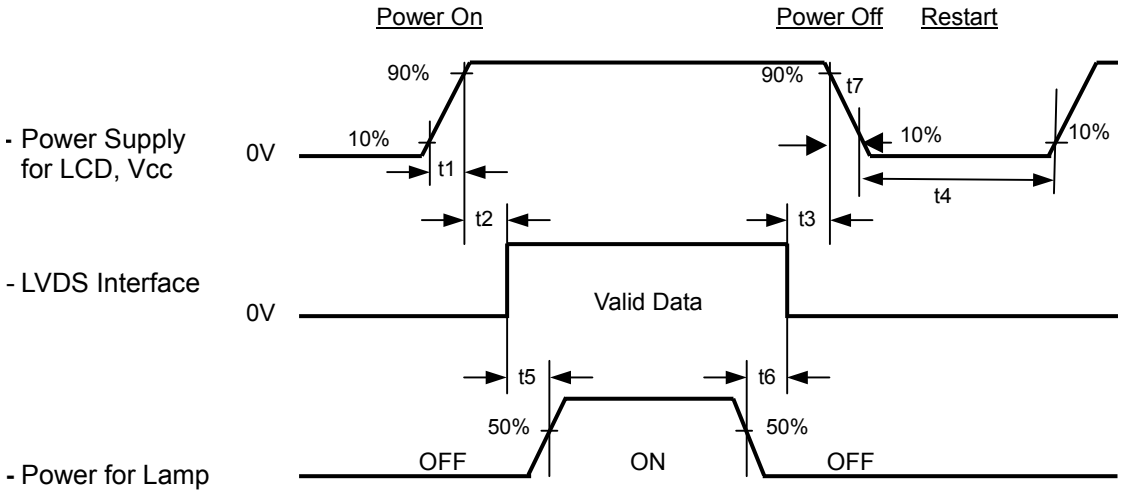
Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

(2) 2 channels LVDS input.

INPUT SIGNAL TIMING DIAGRAM



7.2 POWER ON/OFF SEQUENCE



Timing Specifications:

0.5 ≦ t1 ≦ 10 ms

0 ≦ t2 ≦ 50 ms

0 ≦ t3 ≦ 50 ms

t4 ≧ 500 ms

t5 ≧ 200 ms

t6 ≧ 200 ms

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time is better to follow 5≦t7≦300 ms.

8 OPTICAL CHARACTERISTICS

8.1 TEST CONDITIONS

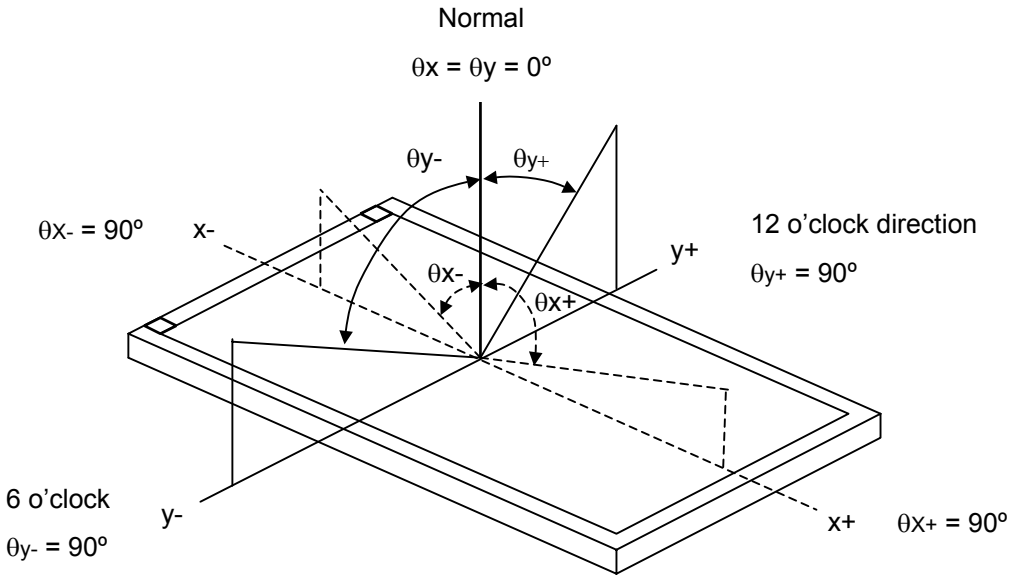
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	6.0	mA
Inverter Driving Frequency	F_L	**61**	KHz
Inverter	Sumida-H05-4915		

The measurement methods of optical characteristics are shown in Section 8.2. The following items should be measured under the test conditions described in Section 8.1 and stable environment shown in Note (5).

8.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	400	600	-	-	(2), (5)
Response Time		T_R		-	6	11	ms	(3)
		T_F		-	14	19	ms	
Average Luminance of White		L_{AVE}		220	250	-	cd/m^2	(4), (5)
Luminance Non-Uniformity		δW_{5p}		-	-	20	%	(5), (6)
		δW_{13p}		-	-	35	%	
Color Gamut		C.G		-	45	-	%	(5), (7)
Color Chromaticity	Red	Rx		TYP -0.02	0.593	TYP +0.02	-	(1), (5)
		Ry			0.341		-	
	Green	Gx			0.318		-	
		Gy			0.541		-	
	Blue	Bx			0.150		-	
		By			0.136		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	55	60	-	Deg.	
		θ_x-		55	60	-		
	Vertical	θ_Y+		45	50	-		
		θ_Y-		45	50	-		

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

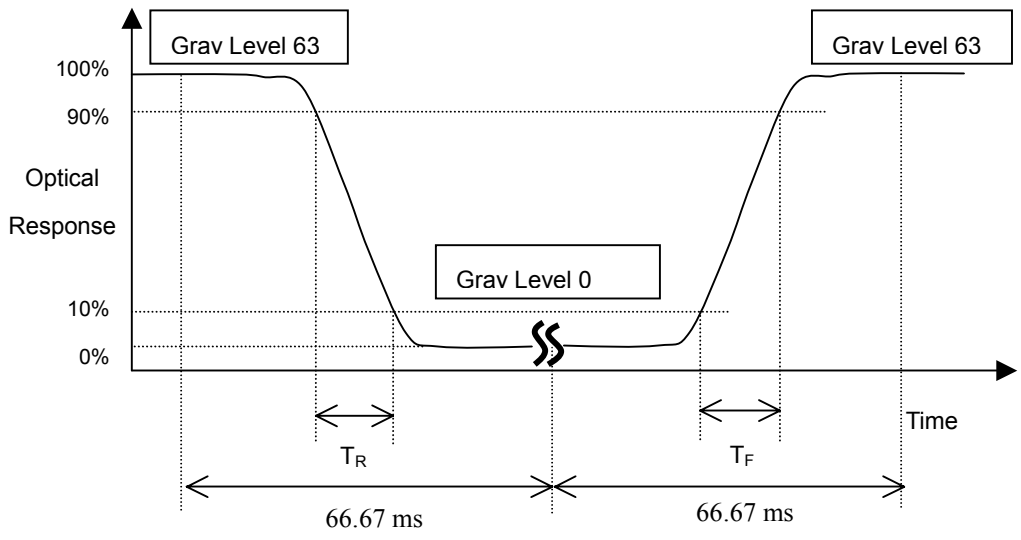
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

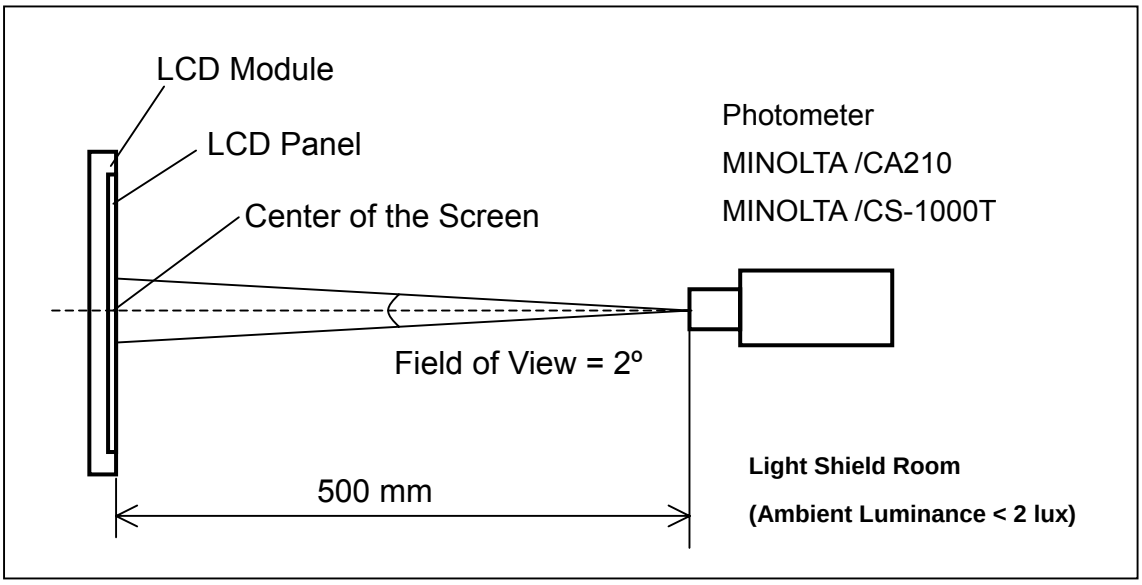
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (5)+ L (10)+ L (11)+ L (12)+ L (13)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6).

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 15 minutes in a windless room.

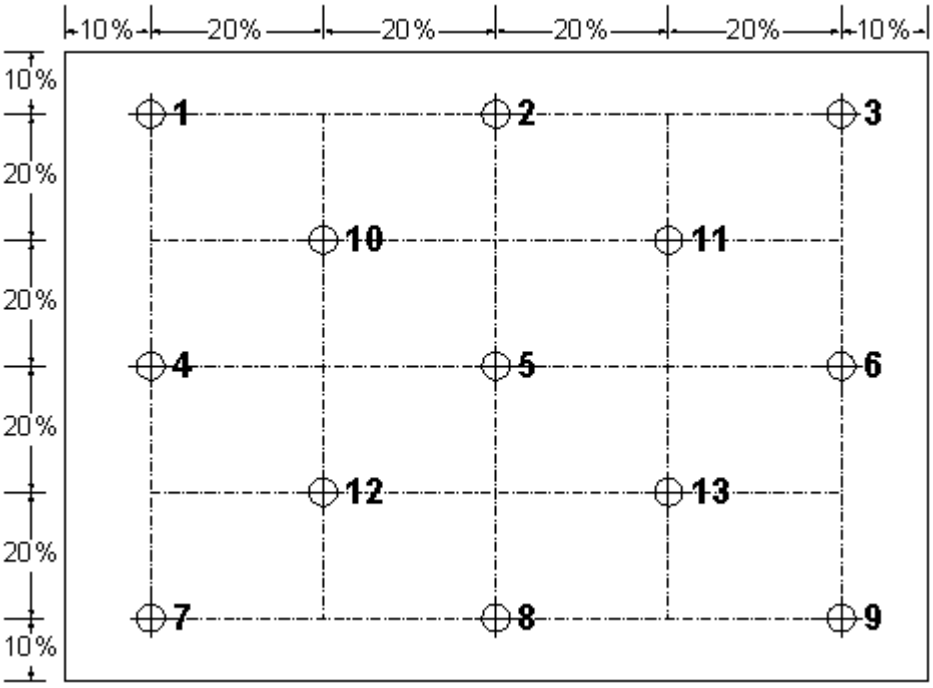


Note (6) Definition of White Variation (δW_{5p}, δW_{13p}):

Measure the luminance of gray level 63 at 5, 13 points

δW_{5p} ={1-{ Minimum [L (5)+ L (10)+ L (11)+ L (12)+ L (13)] / Maximum [L (5)+ L (10)+ L (11)+ L (12)+ L (13)]}} *100%

δW_{13p} ={1-{ Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}} *100%



Ⓧ : Test Point

X=1 to 13

Note (7) Definition of Color Gamut (C.G):

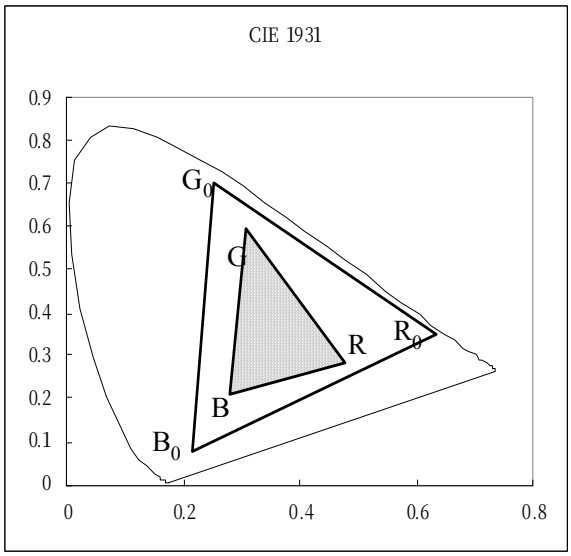
C.G= R G B / R_0 G_0 B_0,*100%

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 63 gray levels of red, green, and blue, respectively.

R_0 G_0 B_0 : area of triangle defined by R_0, G_0, B_0

R G B: area of triangle defined by R, G, B



9 PRECAUTIONS

9.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the lamp wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

9.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

9.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

10 PACKING

10.1 CARTON

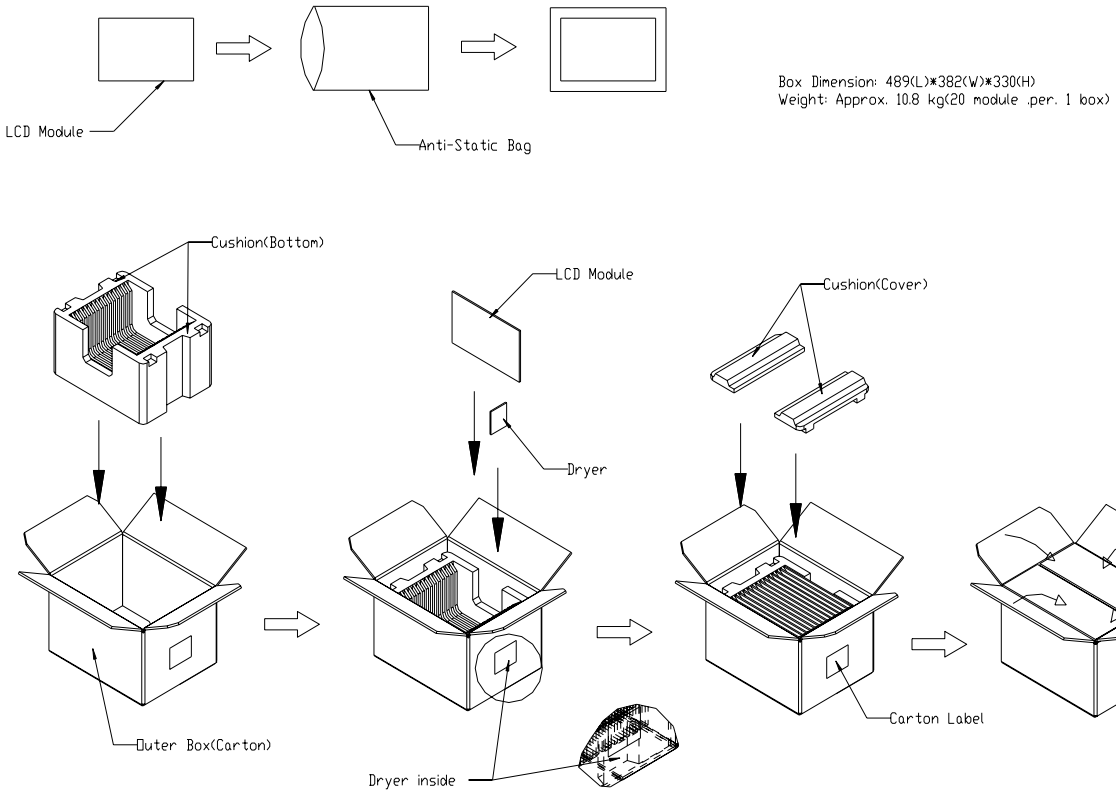


Figure. 10-1 Packing method

10.2 PALLET

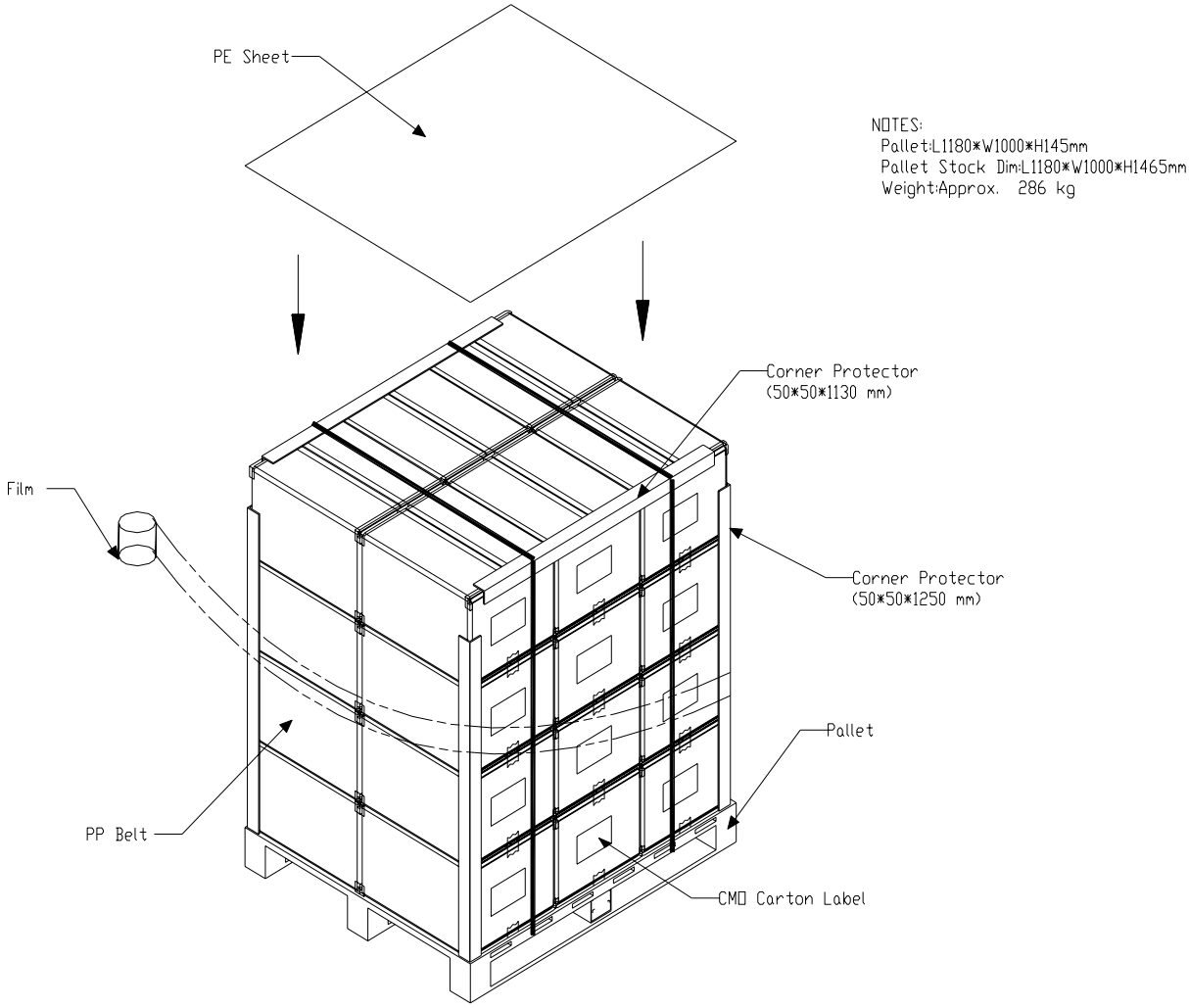
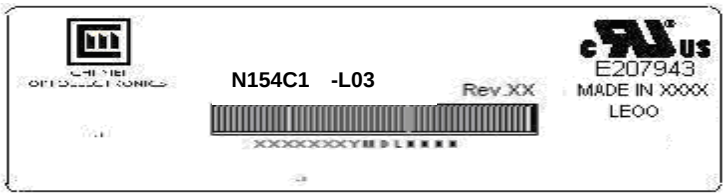


Figure. 10-2 Packing method

11 DEFINITION OF LABELS

11.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N154C1-L03

(b) Revision: Rev. XX, for example: A1, …, C1, C2 …etc.

(c) Serial ID: X X X X X X X Y M D X N N N N

- Serial No.
- CMO Internal Use
- Year, Month, Date
- CMO Internal Use
- Revision
- CMO Internal Use

(d) Production Location: MADE IN XXXX. XXXX stands for production location.

(e) UL/CB logo: "LEOO" especially stands for panel manufactured by CMO Ningbo satisfying UL/CB requirement. "LEOO" is the CMO's UL factory code for Ningbo factory.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

Dell PPID label contains information as below:

(a) Serial ID: TW-0SSSSS-70896-YMD-XXXX

- Serial Numbers
- Production Year, Month, Date
- Manufacturing ID
- Part Number

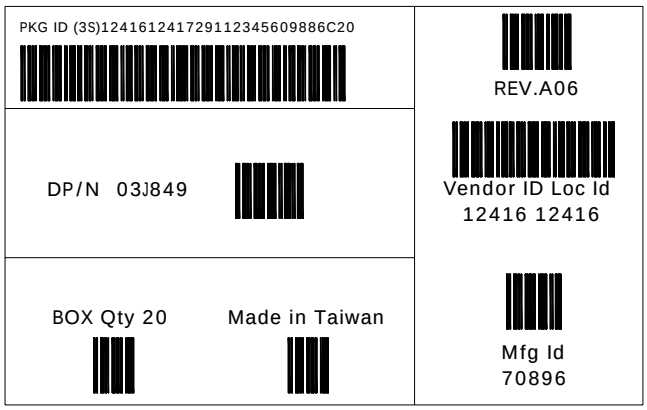
(b) Production location: Made in XXXX.

(c)Revision code: X00, X10, X20, A00..etc.

11.2 CARTON LABEL

(a) Production location: Made In XXXX. XXXX stands for production location

11.3 CARTON LABEL



Type J Label

- Verdana font or equivalent,bold
- 20pt.–all fields
- 203 DPI printer minimum
- Code 128B
- 10–15 mil minimum narrow bar
- .75"minimum barcode height
- .10" or greater quiet zone
- 4.0" x 6.0" label size
- Brady THT –25–402–1 or equivalent
- Brady R6107 series ribbon or equivalent

11.4 PALLET LABEL

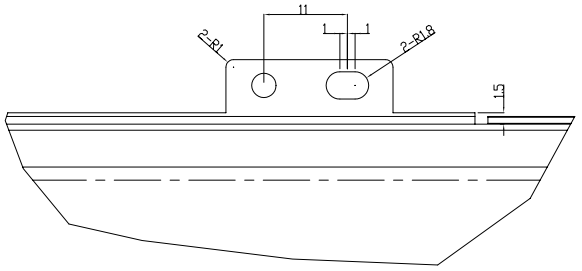
FROM :CMO Corporation Tainan, Taiwan 744 R.O.C	TO:DELL COMPUTER 2128 West Braker Austin TX
P.O.NUMBER 12345678	
	DELL P/N 12345
COUNTRY OF ORIGIN TW	
	PACKING LIST# 1234567890123
PACKING LIST QTY 654321	
	DESTINATION MAS LOC 60
DESTINATION LOCATION B4	
	AIRBILL NUMBER 12345678901234567890

PKG CNT	BOX CNT	REVISION	SHIP DATE
999 OF 999	12345	A00-00	Apr 29,2003

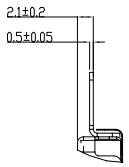
PART DESCRIPTION XXXXXXXXXXXXXXXXXXXXXXXXX
12345678901234567890123456789012345678901

Type K Label

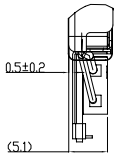
- Verdana font or equivalent,bold
- 12pt.–all descript fields
- 10pt.–all data fields
- 203 DPI printer minimum
- Code 128B
- 10 mil minimum narrow bar
- .30–,50"minimum barcode height
- .10" or greater quiet zone
- 4.0" x 6.5" label size
- Brady THT –78–402–.9 or equivalent
- Brady R6107 series ribbon or equivalent



DETAIL A
SCALE 4:1
(2 Places)

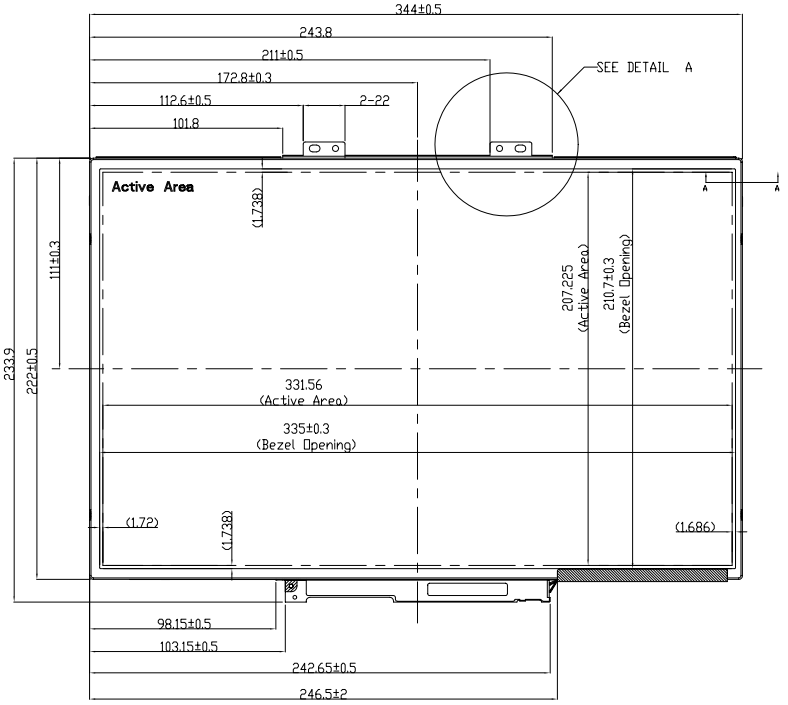


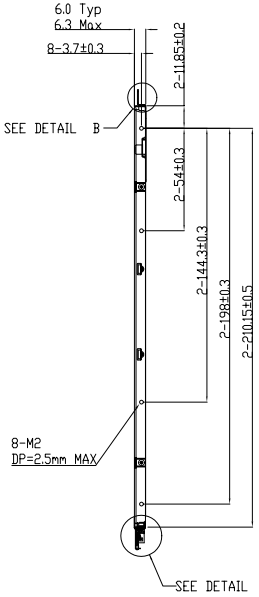
DETAIL B
SCALE 4:1

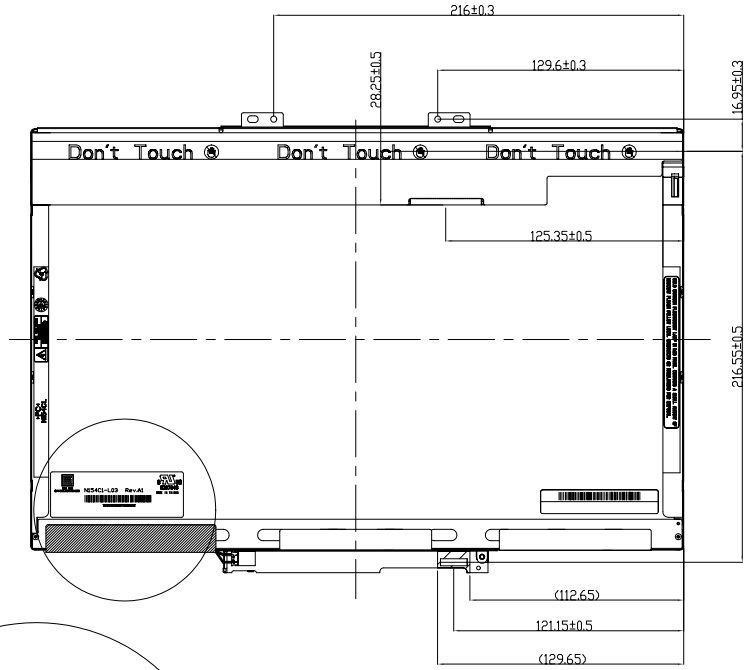


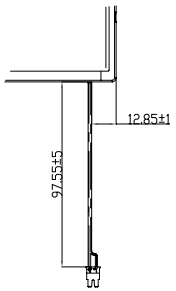
DETAIL C
SCALE 4:1

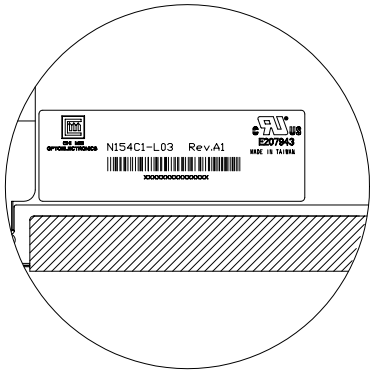
NOTE:
1.GENERAL TOLERANCE : ±0.5 mm.
2.THE SCREW TORQUE FOR MOUNTING SHALL NOT EXEED 2.0 kgf-cm (0.196 N-m).
3."*" MARKS THE DESIGN CRITICAL DIMENSION.
4." Ⓟ" MARKS THE PROCESS CRITICAL DIMENSION.
5.SIGNAL INTERFACE CINNECTOR: FI-XB30SRL-HF11 (JAE).
6.CCFL CONNECTOR : BHSR-02VS-1 (JST).



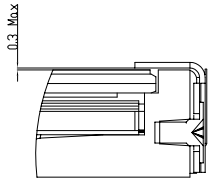








DETAIL A
SCALE 2:1



SECTION A-A
SCALE 10:1

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	Outline_Drawing_N154C1-L03			2D REV.A	
				3D REV.	
Approved	Davis Wang	Drawing No.	N154C1-L03A		
Checked	Shannon Chang	Part No.	None		
Drawer	Jude Lien	Material	TBD	Sheet	1 / 1 A0
Designer	Jude Lien	Date	15-Aug-2006	Scale	XI Unitmm

CHI MEI OPTOELECTRONICS CORP.