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FM27LV010L
1,048,576-Bit (128Kx8) Low Voltage, Low Power EPROM

General Description

The FM27LV010 is a low-power 1Mbit, 3.3V-only one-time-programmable (OTP) read-only memory (EPROM), organized into 128K words with 8 bits per word. Any byte can be accessed in less than 150ns, eliminating the need for WAIT states in high-performance microprocessor systems. The FM27LV010 has separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls which eliminate bus contention issues.

The FM27LV010 is one member of a low voltage EPROM family which range in densities from 512Kb to 1Mb.

Features

■ Read Access Time: 150ns
■ Single 3.3V Power Supply
■ Low Standby Current: 1µA (Typical)

■ Programming Voltage +12.75V
■ Typical programming time 50µs
■ Low Power CMOS Operation
■ 15mA Operation (Max.)
■ CMOS-and TTL-Compatible I/O
■ High-Reliability CMOS Technology
■ Latch-Up Immunity to 100mA from -1V to V_{CC} + 1V
■ Two-Line Control ($\overline{OE}$ & $\overline{CE}$)
■ Standard Product Identification Code
■ JEDEC Standard Pinout
  - 32-pin PDIP
  - 32-pin PLCC
  - 32-pin TSOP (Type 1)
■ Commercial and Industrial Temperature Ranges
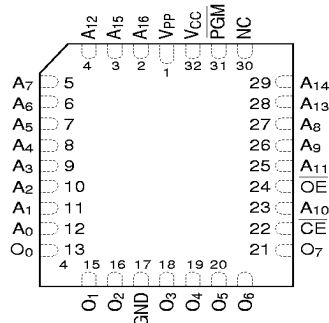
Block Diagram

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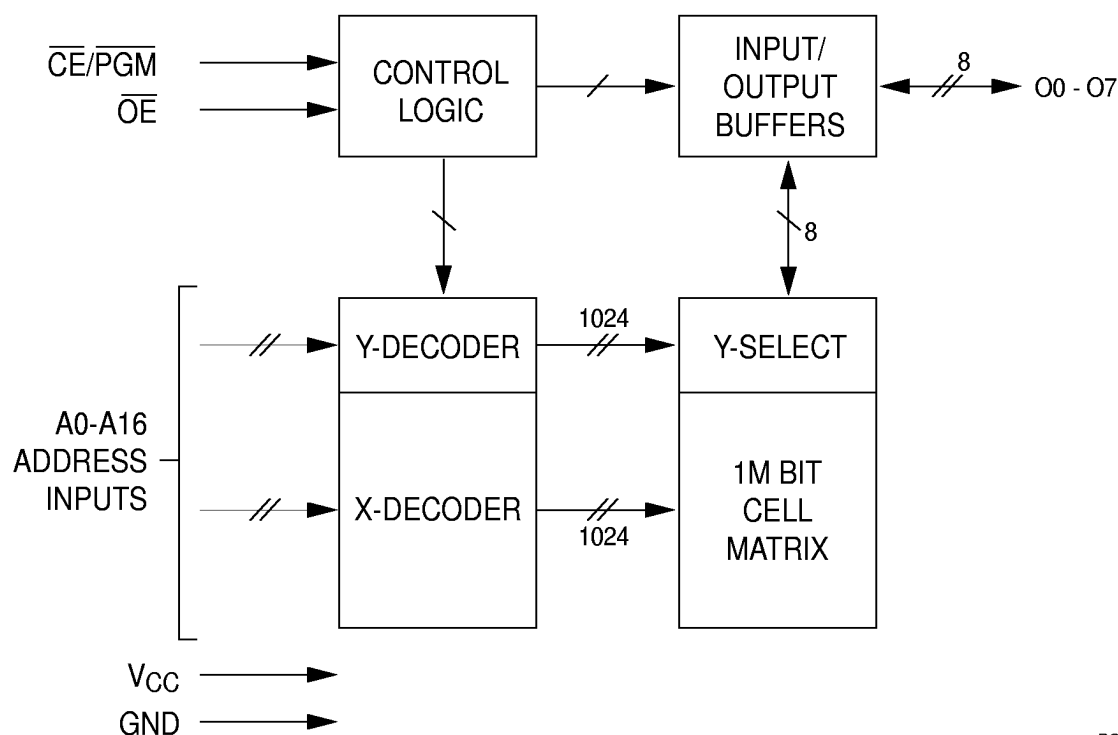
Commercial Temperature Range (0°C to +70°C) V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
FM27LV010 N, T, V 150 L	150

Industrial Temperature Range (-40°C to +85°C) V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
FM27LV010 NE, TE, VE 150 L	150

Pin Names

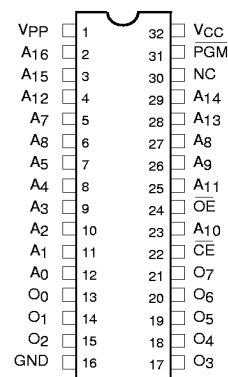| Pin Name	Function
A_0-A_{16}	Addresses
O_0-O_7	Outputs
$\overline{PGM}$	Program
$\overline{OE}$	Output Enable
NC	No Connect
$\overline{CE}$	Chip Enable

Package Types:
N = Plastic DIP Package
T = TSOP Package
V = PLCC Package

All packages conform to the JEDEC standard

PLCC

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PDIP

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TSOP
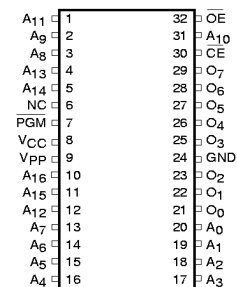
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Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +125°C

All Input Voltage except A9
with Respect to Ground   -0.6V to +7V

V_{PP} and A9 with Respect to Ground   -0.6V to +13.5V

V_{CC} Supply Voltage with
Respect to Ground   -0.6V to +7V

ESD Protection
(MIL St. 883, Method 3015.2)   >2000V

All Output Voltages with
Respect to Ground   -0.6V to V_{CC} + 0.5V

Operating Range

Range	Temperature (T_C)	V_{CC}	Tolerance
Commercial	0°C to +70°C	+3.3V	± 0.3V
Industrial	-40°C to +85°C	+3.3V	± 0.3V

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = -0.4mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA		0.45	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
I_{LI}	Input Leakage Current	V_{IN} = 0 to V_{CC}	-5	5	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to V_{CC}	-10	10	µA
I_{CC3}	V_{CC} Power-Down Current	$\overline{CE}$ = V_{CC} ± 0.3V		10	µA
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}		0.6	mA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = V_{IL}, f = 5MHz, I_{OUT} = 0mA		15	mA
I_{PP}	V_{PP} Supply Current Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}		100	µA

AC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
t_{ACC}	Address to Output Delay		150	ns
t_{CE}	CE to Output Delay		150	ns
t_{OE}	OE to Output Delay		50	ns
t_{DF}	OE or CE High to Output Float, whichever occurred first		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		ns

Capacitance T_A = 25°C, f = 1MHz

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance Except $\overline{OE}/V_{PP}$	V_{IN} = 0V	8	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
V_{PP}	$\overline{OE}/V_{PP}$ Input Capacitance	V_{IN} = 0V	18	25	pF

AC Waveforms for Read Operation

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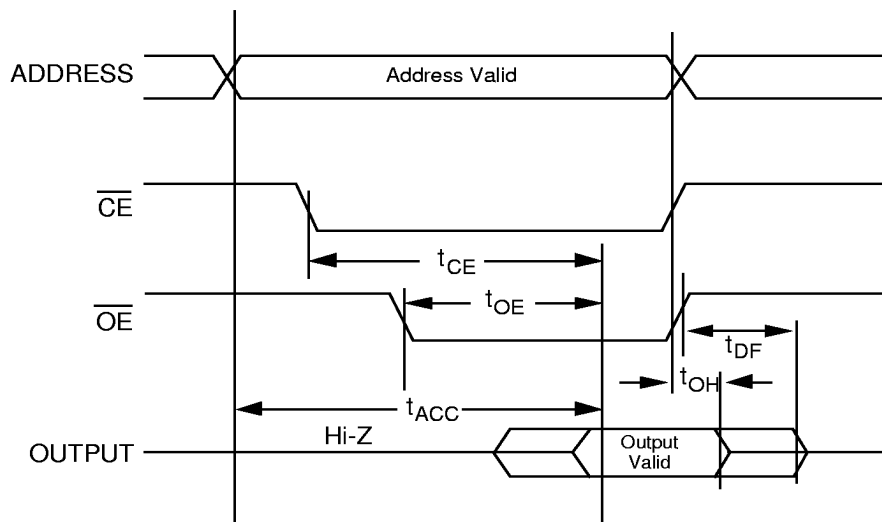
Output Test Waveforms and Measurements

AC DRIVING LEVELS: 2.4V, 0.45V
AC MEASUREMENT LEVEL: 2.0V, 0.8V

t_R, t_F < 20 ns (10% to 90%)

Output Test Load

1.3V

(1N914)

3.3K

OUTPUT PIN

C_L
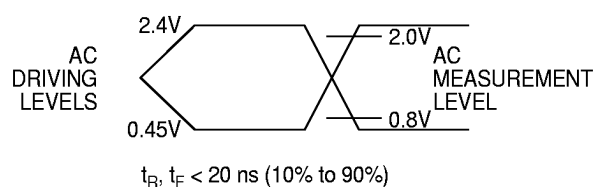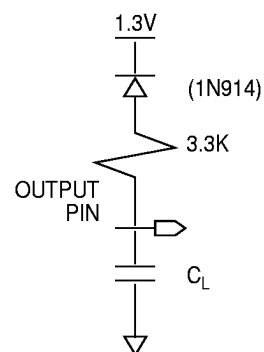
Note:C_L = 100pF including jig capacitance

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DC Programming Characteristics

Sumbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN} = V_{IL}$, V_{IH}		5.0	µA
V_{IL}	Input Low Level		-0.5	0.8	V
V_{IH}	Input High Level		2.4	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V
I_{CC2}	V_{CC} Supply Current			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		10	mA
V_{ID}	A9 Product ID Voltage		11.5	12.5	V
V_{PP}	Programming Supply Voltage		12.5	13.0	V
V_{CC}	Power Supply Voltage		6.25	6.75	V

Switching Programming Characteristics ($T_A = +25° \pm 5°C$)

Symbol	Parameter	Min	Max	Units
t_{AS}	Address Setup Time	1		μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	1		μs
t_{DS}	Data Setup Time	1		μs
t_{AH}	Address Hold Time	0		μs
t_{DH}	Data Hold Time	1		μs
t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	V_{PP} Setup Time	1		μs
t_{PW}	PGM Program Pulse Width	20	105	μs
t_{VCS}	V_{CC} Setup Time	1		μs
t_{CES}	$\overline{CE}$ Setup Time	1		μs
t_{OE}	Data Valid from $\overline{OE}$		150	ns

Programming Waveforms
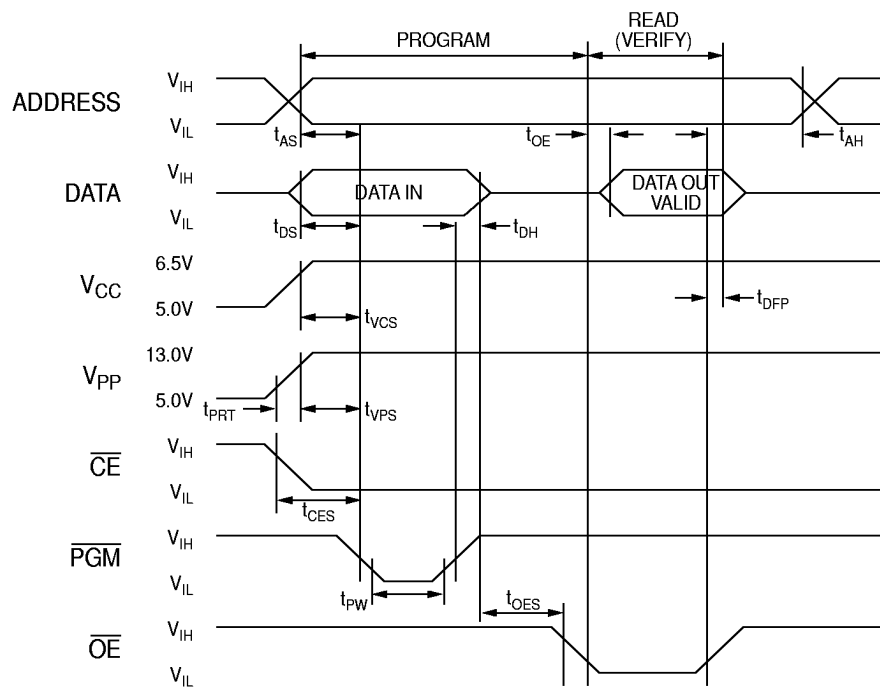
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Turbo Low Voltage Programming Algorithm Flow Chart

$V_{CC} = 6.5V$ $V_{PP} = 12.75V$
n = 0
ADDRESS = FIRST LOCATION

PROGRAM ONE 50µs PULSE
INCREMENT n

VERIFY BYTE

n = 10?

DEVICE FAILED

LAST ADDRESS?

INCREMENT ADDRESS
n = 0

ADDRESS = FIRST LOCATION

VERIFY BYTE

INCREMENT ADDRESS

PROGRAM ONE 50 µs PULSE

LAST ADDRESS?

CHECK ALL BYTES
1ST: $V_{CC} = V_{PP} = 4.0V$
2ND: $V_{CC} = V_{PP} = 3.0V$
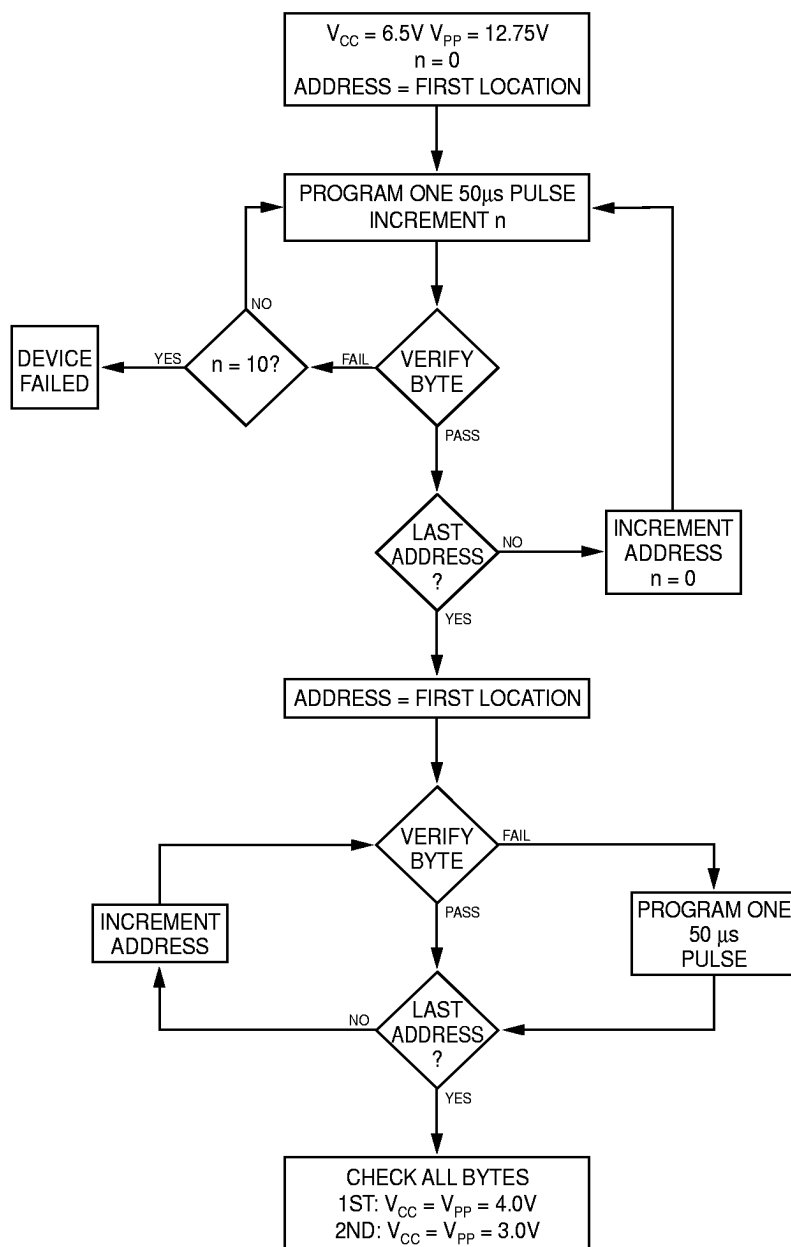
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Figure 1

Note: National Semiconductor NM27C010 Fast Programming Algorithm may also be used.

Functional Description

Device Operation

The modes of operation of the EPROM are listed in Table 1. The power supplies required are V_{CC} and OE/V_{PP}. The OE/V_{PP} power supply must be at 12.75 during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power must be at 6.5V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE/PGM) is the power control and should be used for device selection. Output Enable (OE/V_{PP}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that CE has been low and addresses have been stable for at least t_{ACC} - t_{OE}.

Standby Mode

The FM27LV010 has CMOS standby mode which reduces the maximum V_{CC} current to 1μA (typical). It is placed in CMOS standby when CE is at V_{CC} ± 0.3V. The FM27LV010 also has a TTL standby mode which reduces the maximum V_{CC} current to 0.6 mA. It is placed in TTL standby when CE is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the OE input.

Two-Line Output Control Function

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that CE be decoded and used as the primary device-selection function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Programming

Caution: Exceeding 13.5V on pin 22 (OE/V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the OE/V_{PP} power supply is at 12.75V. it is required that at least a 0.1μf capacitor be placed across V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address locaiton to be programmed.

The EPROM is programmed with the Turbo Low Voltage Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50μs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50μs pulse. The Turbo Low Voltage Programming Algorithm will be available in early Quarter 1, 1998. Until this program is installed the EPROM may be programmed using National Semiconductor NM27C010 Fast Programming Algorithm.

The EPROM must not be programmed with a DC signal applied to the CE/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Program Inhibit Mode

Programming of multiple FM27LV010 in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for CE, all like inputs of the parallel FM27LV010 may be common. A TTL low-level program pulse appled to a FM27LV010 CE input with OE/V_{PP} = 12.75 ± 0.25V will program that FM27LV010. A high-level CE input inhibits the other FM27LV010 from being programmed.

Program Verify Mode

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with OE/V_{PP} and CE at V_{IL}. Data should be verified at t_{DV} after the falling edge of CE.

System Consideration

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7μF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Selection

The modes of operation of the FM27LV010 are listed in Table 1. A single 3.3V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

Functional Description (Continued)

Table 1. Mode Selection

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A1	A9	V_{PP}	Output
Read	V_{IL}	V_{IL}	X (Note 2)	X	X	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	X	X	V_{CC}	High Z
Standby (TTL)	V_{IH}	X	X	X	X	X	V_{CC}	High Z
Standby (CMOS)	$V_{CC} \pm 0.3V$	X	X	X	X	X	V_{CC}	High Z
Program (Note 4)	V_{IL}	V_{IH}	V_{IL}	X	X	X	V_{PP}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	X	V_{PP}	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	X	V_{PP}	High Z
Manufacturer Code (Note 3)	V_{IL}	X	V_{IL}	V_{IL}	V_{IH}	VH (Note 1)	V_{CC}	
Device Code (Note 3)	V_{IL}	X	V_{IH}	V_{IH}	V_{IH}	VH (Note 1)	V_{CC}	

Note 1: VH = 12.0V ± 0.5V.
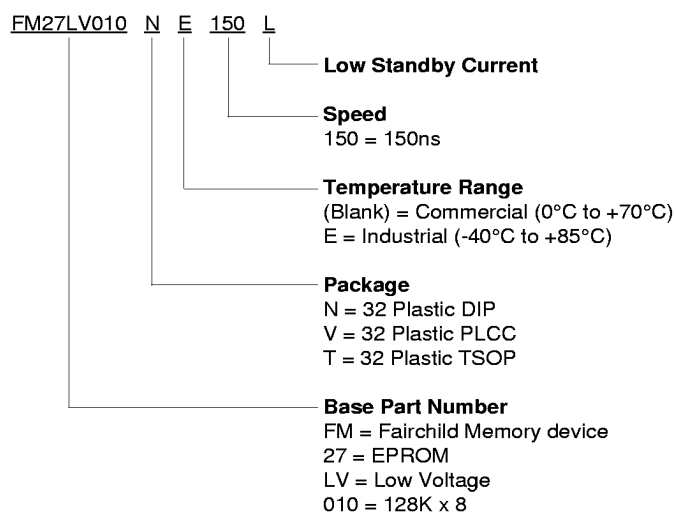
Note 2: X = Either V_{IH} or V_{IL}.

Note 3: For Manufacturer Code and Device Code, A1 = V_{IH}
When A1 = V_{IL}, both codes will read 7F.

Note 4: See DC Programming Characteristics for V_{PP} voltage during programming.
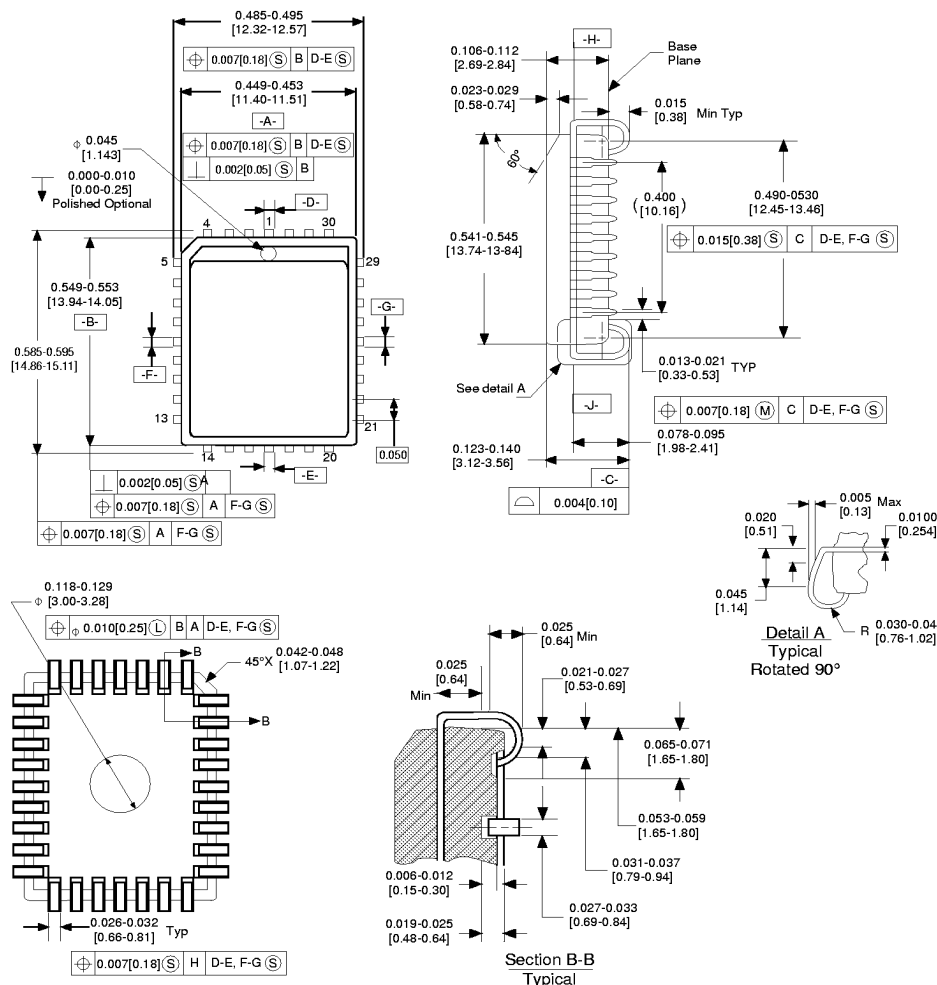
Table 2. Manufacturer's Identification Code

Pins Code	A 0	A 1	O 7	O 6	O 5	O 4	O 3	O 2	O 1	O 0	Hex Data
Manufacturer	0	1	0	0	0	1	1	1	0	0	1C
Device Type	1	1	0	1	0	0	0	0	0	1	01
Continuation	0	0	0	1	1	1	1	1	1	1	7F
	1	0	0	1	1	1	1	1	1	1	7F

Ordering Information

FM27LV010 N E 150 L

Low Standby Current

Speed
150 = 150ns

Temperature Range
(Blank) = Commercial (0°C to +70°C)
E = Industrial (-40°C to +85°C)

Package
N = 32 Plastic DIP
V = 32 Plastic PLCC
T = 32 Plastic TSOP

Base Part Number
FM = Fairchild Memory device
27 = EPROM
LV = Low Voltage
010 = 128K x 8

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Physical Dimensions inches (millimeters) unless otherwise noted

20.0 ± 0.2

1   32

0.5

16   17

0.15-0.25 TYP

0.95 - 1.06

8.0 ± 0.2

0.150±0.08
(Leadframe
Thickness)

18.4 ± 0.1

⌒ 0.10

See Detail A

DETAIL A
Typical

1.27 MAX

0°-5°

0-0.25   0.4-0.6

32-Pin TSOP Package

1.64 – 1.66
(41.66 – 42.164)

32   17

0.062
(1.575) TYP
RAD

0.490 – 0.550
(12.446 – 13.97)

1   16

Pin No. 1 IDENT

0.580
(14.73)
MIN

0.600 – 0.620
(15.240 – 15.748)

90°–105°

0.008 - 0.015
(0.203 – 0.381)

0.040 - 0.090
(1.016 – 2.286)

0.100 ±0.010
(2.540 ±0.254)

0.035 - 0.07
(0.889 – 1.778)

0.050
(1.270)
TYP

0.018 ±0.003
(0.457 ±0.078)

0.125 – 0.165
(3.175 – 4.191)

0.145 – 0.210
(3.683 – 5.334)

86°– 94°
TYP

0.015
(0.381)

0.120 – 0.150
(3.048 – 3.81)

32-Lead Plastic One-Time-Programmable Dual-in-Line

Physical Dimensions inches (millimeters) unless otherwise noted

32-Lead Plastic Leaded Chip Carrier (PLCC)
Package Number VA32A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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