T-51-10-90

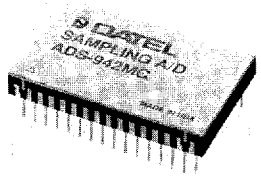
# ADS-942

## 14-Bit, 2.0 MHz, High Resolution Sampling A/D Converter

*PRELIMINARY PRODUCT DATA*

### FEATURES

- **14-Bit resolution**
- **Internal Sample/Hold**
- **2.0 MHz minimum throughput**
- **Functionally complete**
- **Small 32-pin DIP**
- **Low-power 2.9 Watts**
- **Three-state output buffers**
- **Samples up to Nyquist**



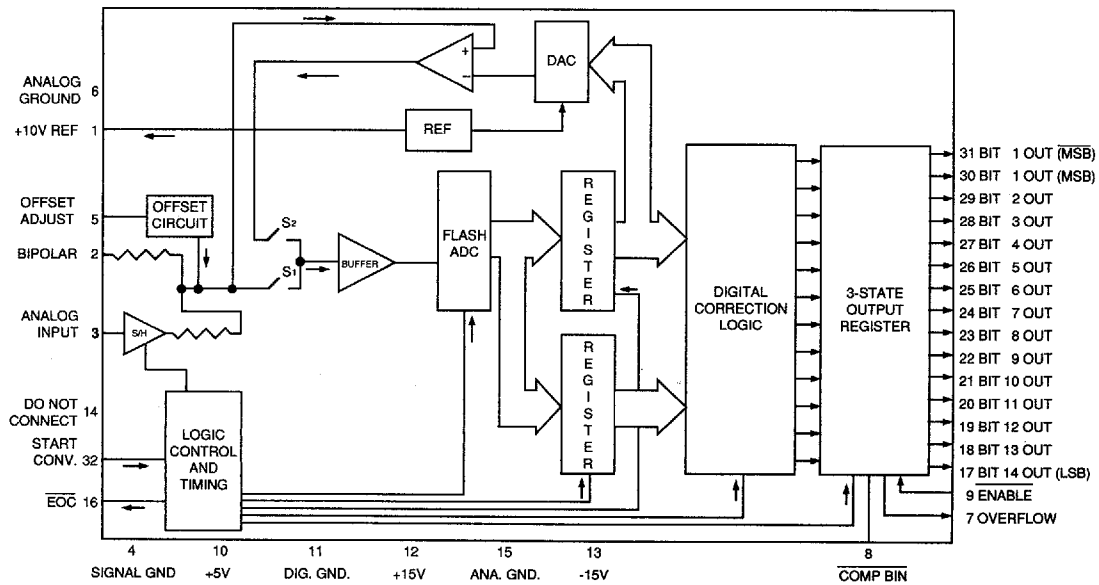

### GENERAL DESCRIPTION

DATEL's ADS-942 is a 14-bit, 2.0 MHz sampling rate, functionally complete A/D converter. The ADS-942 samples up to Nyquist with no missing codes.

Packaged in a small 32-pin DIP, power requirements are ±15 volts and +5 volts with 2.9 Watts power dissipation.

### INPUT/OUTPUT CONNECTIONS

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | +10V REF. OUT | 17 | BIT 14 OUT (LSB) |
| 2 | BIPOLAR | 18 | BIT 13 OUT |
| 3 | ANALOG INPUT | 19 | BIT 12 OUT |
| 4 | SIGNAL GROUND | 20 | BIT 11 OUT |
| 5 | OFFSET ADJUST | 21 | BIT 10 OUT |
| 6 | ANALOG GROUND | 22 | BIT 9 OUT |
| 7 | OVERFLOW | 23 | BIT 8 OUT |
| 8 | $\overline{\text{COMP. BIN}}$ | 24 | BIT 7 OUT |
| 9 | $\overline{\text{ENABLE}}$ | 25 | BIT 6 OUT |
| 10 | +5V | 26 | BIT 5 OUT |
| 11 | DIGITAL GROUND | 27 | BIT 4 OUT |
| 12 | +15V | 28 | BIT 3 OUT |
| 13 | -15V | 29 | BIT 2 OUT |
| 14 | DO NOT CONNECT | 30 | BIT 1 OUT (MSB) |
| 15 | ANALOG GROUND | 31 | BIT 1 OUT ($\overline{\text{MSB}}$) |
| 16 | $\overline{\text{EOC}}$ | 32 | START CONVERT |



# ADS-942

## ABSOLUTE MAXIMUM RATINGS

| PARAMETERS | LIMITS | UNITS |
|---|---|---|
| **+15V Supply (Pin 12)** | -0.3 to +18 | Volts dc |
| **-15V Supply (Pin 13)** | +0.3 to -18 | Volts dc |
| **+5V Supply (Pin 10)** | -0.3 to +7.0 | Volts dc |
| **Digital Inputs (Pins 8, 9, 32)** | -0.3 to +7.0 | Volts dc |
| **Analog Input (Pin 3)** | ±25 | Volts |
| **Lead Temp. (10 Sec.)** | 300 max | °C |

## FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.②

| ANALOG INPUTS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| **Input Voltage Range** | | | | |
| | – | 0 to +10 | – | Volts |
| | – | ±5 | – | Volts |
| **Input Impedance** | 2.2 | 2.5 | – | K Ohms |
| **Input Capacitance** | – | 7 | 15 | pf |
| **DIGITAL INPUTS** | | | | |
| **Logic Levels** | | | | |
| Logic "1" | 2.0 | – | – | Volts dc |
| Logic "0" | – | – | 0.8 | Volts dc |
| Logic Loading "1" | – | – | 5.0 | µA |
| Logic Loading "0" | – | – | -200 | µA |
| **PERFORMANCE** | | | | |
| **Int. Non-Lin. @ $f_{IN}$ = 1 MHz** | | | | |
| +25 °C | – | ±1/2 | ±1 | LSB |
| 0 to +70 °C | – | ±3/4 | ±1.5 | LSB |
| -55 to +125 °C | – | ±1 | ±2.5 | LSB |
| **Diff. Non-Lin. @ $f_{IN}$ = 1 MHz** | | | | |
| +25 °C | – | ±1/2 | ±1 | LSB |
| 0 to +70 °C | – | ±3/4 | ±1.25 | LSB |
| -55 to +125 °C | – | ±1 | ±2.5 | LSB |
| **Full Scale Absolute Accuracy** | | | | |
| +25 °C. | – | ±0.08 | ±0.122 | %FSR |
| 0 to +70 °C | – | ±0.18 | ±0.36 | %FSR |
| -55 to +125 °C | – | ±0.61 | ±0.85 | %FSR |
| **Unipolar Zero Error,** | | | | |
| +25 °C | – | ±0.012 | ±0.04 | %FSR |
| 0 to +70 °C | – | ±0.07 | ±0.13 | %FSR |
| -55 to +125 °C | – | ±0.1 | ±0.17 | %FSR |
| **Bipolar Zero Error,** | | | | |
| +25 °C (Tech Note 1) | – | ±0.04 | ±0.122 | %FSR |
| 0 to +70 °C | – | ±0.07 | ±0.18 | %FSR |
| -55 to +125 °C | – | ±0.1 | ±0.3 | %FSR |
| **Bipolar Offset Error,** | | | | |
| +25 °C (Tech Note 1) | – | ±0.018 | ±0.061 | %FSR |
| 0 to +70 °C | – | ±0.12 | ±0.3 | %FSR |
| -55 to +125 °C | – | ±0.53 | ±0.73 | %FSR |
| **Gain Error,** +25 °C (See Tech Note 1) | – | ±0.018 | ±0.122 | %FSR |
| 0 to +70 °C | – | ±0.12 | ±0.3 | %FSR |
| -55 to +125 °C | – | ±0.53 | ±0.73 | %FSR |
| **No Missing Codes** | Over 0 to 70°C | | | |
| 14 Bits @ 1 MHz $f_{IN}$ | Over -55 to +125°C | | | |
| 13 Bits @ 1 MHz $f_{IN}$ | 14 Bits | | | |
| **Resolution** | | | | |

| OUTPUTS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| **Output Coding** | | | | |
| (Pin 8 Hi) | Straight binary/offset binary | | | |
| (Pin 8 Low) | Complementary binary | | | |
| **Logic Levels** | | | | |
| Logic "1" | 2.4 | – | – | Volts dc |
| Logic "0" | – | – | 0.4 | Volts dc |
| Logic Loading "1" | – | – | -160 | µA |
| Logic Loading "0" | – | – | 6.4 | mA |
| **Internal Reference Voltage,** +25 °C | +9.98 | +10.0 | +10.02 | Volts dc |
| Drift | – | ±13 | ±30 | ppm/ °C |
| External Current | – | – | 5 | mA |
| **DYNAMIC PERFORMANCE** | | | | |
| **Total Harm. Distort. (-0.5 dB)** | | | | |
| DC to 100 KHz | -79 | -85 | – | FS - dB |
| 100 KHz to 1 MHz | -73 | -79 | – | FS - dB |
| **Signal-to-Noise Ratio** (w/o distortion, -0.5 dB) | | | | |
| DC to 100 KHz | -78 | -85 | – | FS - dB |
| 100 KHz to 1 MHz | -73 | -79 | – | FS - dB |
| **Signal-to-Noise Ratio** & distortion, -0.5 dB | | | | |
| DC to 100 KHz | -72 | -77 | – | FS - dB |
| 100 KHz to 1 MHz | -68 | -71 | – | FS - dB |
| **Effective Bits, -0.5 dB** | | | | |
| DC to 100 KHz | 12.3 | 13.0 | – | Bits |
| 100 KHz to 1 MHz | 11.7 | 12.3 | – | Bits |
| **Two-tone Intermodulation Distortion ($f_{IN}$ = 100 KHz,** 240 KHz, Fs=2.0 MHz, -0.5 dB) | -92 | – | – | FS - dB |
| **Input Bandwidth** | | | | |
| Small Signal (-20 dB input) | 6 | – | – | MHz |
| Full Power (0 dB input) | 1.75 | – | – | MHz |
| **Slew Rate** | 210 | 250 | – | V/µSec. |
| **Aperture Delay Time** | – | – | ±10 | nSec. |
| **Aperture Uncertainty, Rms** | – | – | ±10 | pSec. |
| **S/H Acquisition Time** ( to 0.006%FS (10V step) | – | 120 | 150 | nSec. |
| **Feedthrough Rejection** @ $f_{IN}$ = 1 MHz | -85 | – | – | dB |
| **Overvoltage Recovery, ±12V** | – | 1000 | 2000 | nSec. |
| **A/D Conversion Rate** | | | | |
| +25 °C | 2.0 | 2.1 | – | MHz |
| 0 to +70 °C | 2.0 | 2.1 | – | MHz |
| -55 to +125 °C | 2.0 | 2.05 | – | MHz |
| **POWER REQUIREMENTS** | | | | |
| **Power Supply Range** | | | | |
| +15V dc Supply | +14.25 | +15.0 | +15.75 | Volts dc |
| -15V dc Supply | -14.25 | -15.0 | -15.75 | Volts dc |
| +5V dc Supply | +4.75 | +5.0 | +5.25 | Volts dc |
| **Power Supply Current** | | | | |
| +15V dc Supply | – | +70 | +87 | mA |
| -15V dc Supply | – | -80 | -98 | mA |
| +5V dc Supply ① | – | +155 | +165 | mA |
| **Power Dissipation** | – | 2.9 | 3.4 | Watts |
| **Power Supply Rejection** | – | – | 0.02 | %FSR/%V |
| **PHYSICAL/ENVIRONMENTAL** | | | | |
| **Operating Temp. Range** | | | | |
| **-MC** | 0 | – | +70 | °C |
| **-MM** | -55 | – | +125 | °C |
| **Storage Temperature Range** | -65 | – | +150 | °C |
| **Package Type** | 32-pin hermetic sealed, ceramic DIP | | | |
| **Weight** | 0.42 ounces (12 grams) | | | |

① +5V power usage at 1 TTL logic loading per data output bit.
② Warm-up time to full specification: 20 minutes.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## TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 200 Ω trimming potentiometer in series with the analog input for gain adjustment. Use a short in place of the gain adjustment trim pot for operation without adjustments. Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (connect pin 5 to pin 15, analog ground for operation without adjustment).

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 15).

4. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 8) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie pin 18 to ground. The pin 18 signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 9) to a logic "0" (low). To disable, connect pin 9 to a logic "1" (high).

## CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, and Table 1 for the appropriate full-scale range (FSR). Apply a pulse of 35 nanoseconds minimum to the START CONVERT input (pin 32) at a rate of 200 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

**Table 1. Input Connections**

| INPUT RANGE | INPUT PIN | TIE TOGETHER |
|---|---|---|
| 0 to +10V | Pin 3 | Pins 2 and 4 |
| ±5V | Pin 3 | Pins 1 and 2 |

**Table 2. Zero and Gain Adjust**

| FSR | ZERO ADJUST +1/2 LSB | GAIN ADJUST FS - 1/2 LSB |
|---|---|---|
| 0 to +10V | -305 µV | +9.999085V |
| ±5V | -305 µV | -4.999085V |

2. Zero Adjustments
Apply a precision voltage reference source between the analog input (pin 3) and signal ground (pin 4). Adjust the output of the reference source per Table 2.

For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001 with the $\overline{\text{COMP BIN}}$ (pin 8) tied low (straight binary) or between 11 1111 1111 1111 and 11 1111 1111 1110 with the pin 8 tied high (complementary binary).

For bipolar operation, adjust the potentiometer such that the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001 with pin 8 tied high (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with pin 8 tied low (complementary offset binary).

Two's complement coding requires use of the $\overline{\text{MSB}}$ (pin 31) with $\overline{\text{COMP BIN}}$ (pin 8) tied high, adjusting the potentiometer such that the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.

3. Full-Scale Adjustment
Set the output of the voltage reference used in step 2 to the value shown in Table 2.

Adjust the gain trimming potentiometer so that the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111 for $\overline{\text{COMP BIN}}$ (pin 8) tied low for unipolar operation or tied high for bipolar operation (straight binary/offset binary) or between 00 0000 0000 0000 and 00 0000 0000 0001 for $\overline{\text{COMP BIN}}$ tied high for unipolar operastion- or tied low for bipolar operation (complementary binary/complementary offset binary).

Two's complement coding requires use of the $\overline{\text{MSB}}$ (pin 31) with the $\overline{\text{COMP BIN}}$ (pin 8) tied high, adjusting the gain trimming potentiometer so that the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

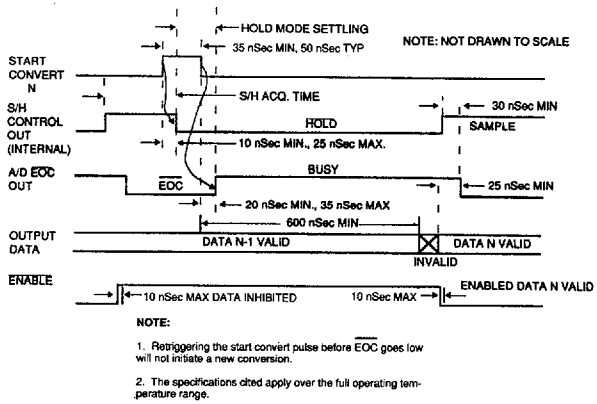
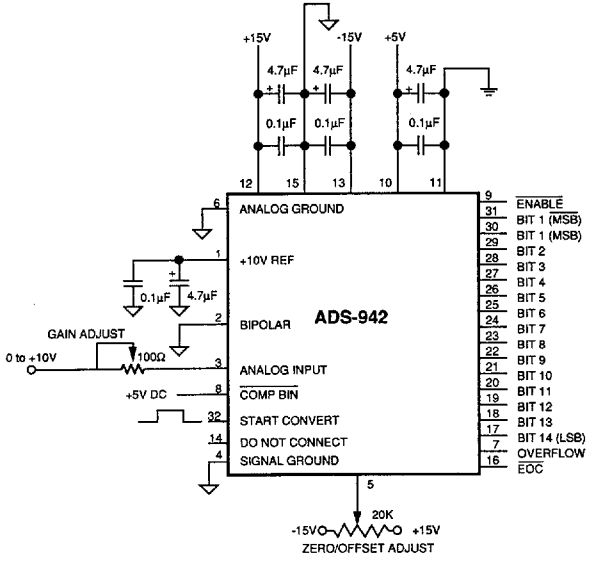


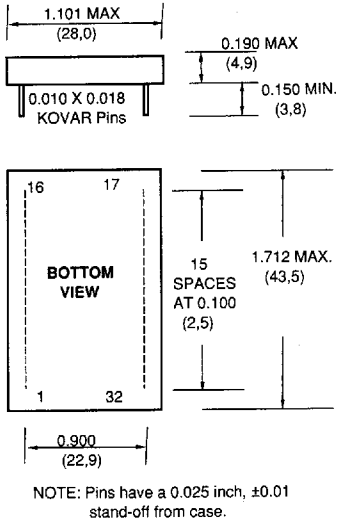

**Figure 2. ADS-942 Timing Diagram**

**Table 3. Output Coding**

| | | STRAIGHT BIN. COMP. BINARY | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **UNIPOLAR SCALE** | **INPUT RANGES, V dc 0 to +10V** | **OUTPUT CODING MSB** | **LSB** | **MSB** | **LSB** | **MSB** | **LSB** | **INPUT RANGE ±10V dc** | **BI POLAR SCALE** |
| FS -1 LSB | +9.999390 | 11 1111 1111 1111 | | 00 0000 0000 0000 | | 01 1111 1111 1111 | | -4.99939 | +FS -1 LSB |
| 7/8 FS | +8.750000 | 11 1000 0000 0000 | | 00 0111 1111 1111 | | 01 1000 0000 0000 | | -3.75000 | +3/4 FS |
| 3/4 FS | +7.500000 | 11 0000 0000 0000 | | 00 1111 1111 1111 | | 01 0000 0000 0000 | | -2.50000 | +1/2 FS |
| 1/2 FS | +5.000000 | 10 0000 0000 0000 | | 01 1111 1111 1111 | | 00 0000 0000 0000 | | 0.00000 | 0 |
| 1/4 FS | +2.500000 | 01 0000 0000 0000 | | 10 1111 1111 1111 | | 10 0000 0000 0000 | | +2.50000 | -1/2 FS |
| 1/8 FS | +1.250000 | 00 1000 0000 0000 | | 11 0111 1111 1111 | | 10 1000 0000 0000 | | +3.75000 | -3/4 FS |
| 1 LSB | +0.000610 | 00 0000 0000 0001 | | 11 1111 1111 1110 | | 10 0000 0000 0001 | | +4.99939 | -FS +1 LSB |
| 0 | 0.000000 | 00 0000 0000 0000 | | 11 1111 1111 1111 | | 10 00000000 0000 | | +5.00000 | -FS |
| | | OFF. BINARY | COMP | OFF | BIN. | TWO'S | COMP. | | |




**MECHANICAL DIMENSIONS INCHES (MM)**




NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

**Figure 3. Typical ADS-942 Connection Diagram**

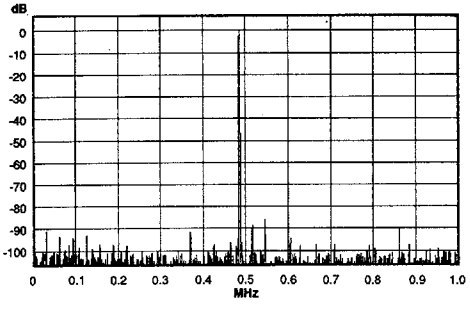



**Figure 4. FFT Analysis of ADS-942**

## ORDERING INFORMATION

| MODEL NUMBER | OPERATING TEMP. RANGE | SEAL |
|---|---|---|
| ADS-942MC | 0 °C to +70 °C | Hermetic |
| ADS-942MM | -55 °C to +125 °C | Hermetic |

**ACCESSORY** ADS-EVAL1 Evaluation Board (without ADS-942)

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

For availibility of MIL-STD-883B versions, contact DATEL.