NEC

MOS INTEGRATED CIRCUIT

MC-42S8LFF64S

3.3 V OPERATION 8M-WORD BY 64-BIT DYNAMIC RAM MODULE (SO DIMM), EDO

Description

The MC-42S8LFF64S is a 8,388,608 words by 64 bits dynamic RAM module (Small Outline DIMM) on which 8 pieces of 64M DRAM : μPD42S65805 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

• EDO (Hyper page mode)

• 8,388,608 words by 64 bits organization

• Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	EDO (Hyper page mode) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-42S8LFF64S-A50	50 ns	84 ns	20 ns	3.89 W	5.76 mW (CMOS level input)
MC-42S8LFF64S-A60	60 ns	104 ns	25 ns	3.31 W	

• Refresh cycle

Family	Refresh cycle	Refresh
MC-42S8LFF64S-A50	4,096 cycles / 128 ms	/RAS only refresh, Normal read / write, /CAS before /RAS refresh, /CAS before /RAS self refresh, Hidden refresh
MC-42S8LFF64S-A60		

• 144-pin small outline dual in-line memory module (Pin pitch = 0.8 mm)

• Single +3.3 V ± 0.3 V power supply

• Serial PD

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

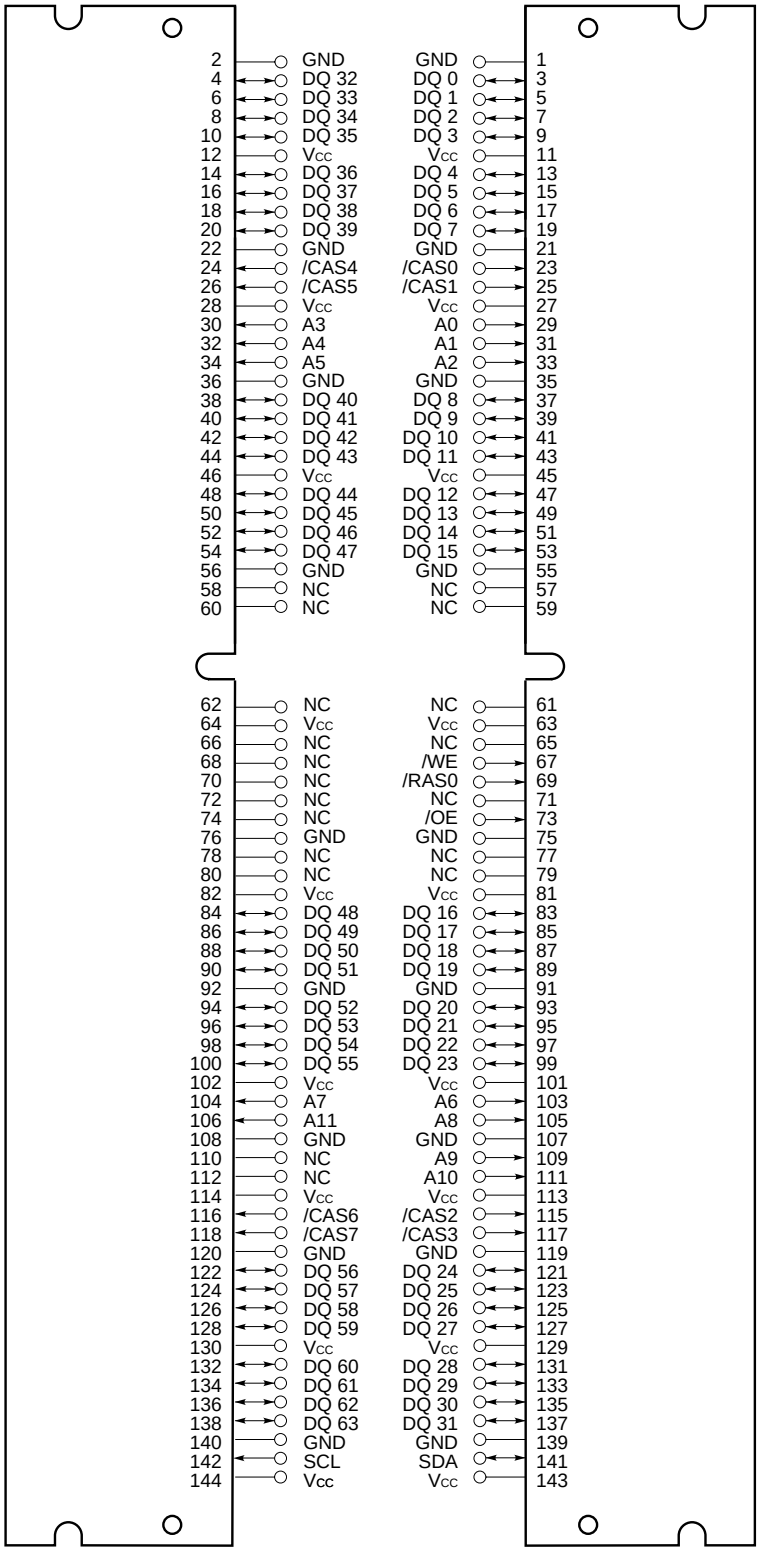
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S8LFF64SA-A50	50 ns	144-pin Small Outline DIMM (Socket Type) Edge connector : Gold plated	8 pieces of μPD42S65805G5 (400 mil TSOP(II)) [Double side]
MC-42S8LFF64SA-A60	60 ns		
MC-42S8LFF64SD-A50	50 ns		
MC-42S8LFF64SD-A60	60 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)

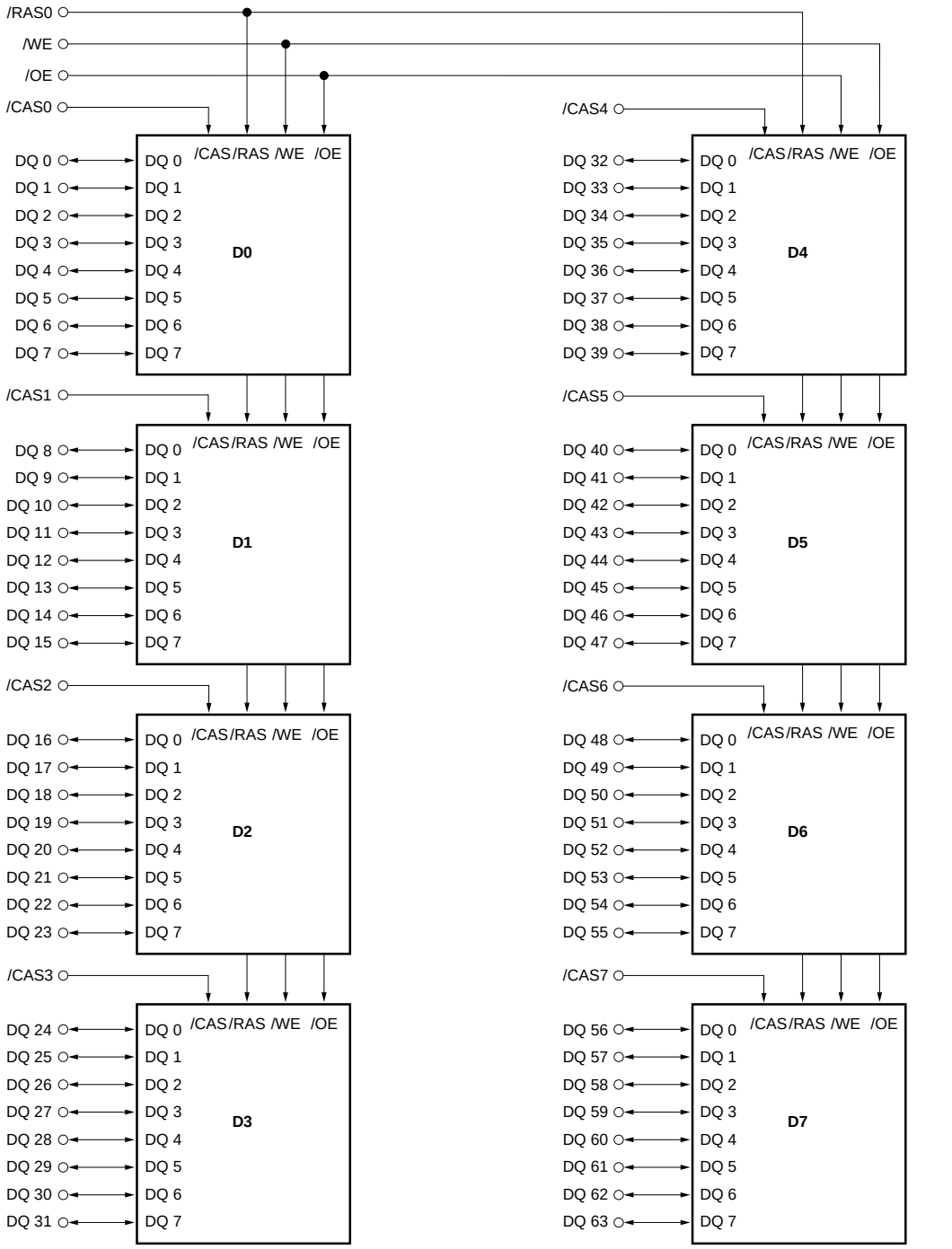
[MC-42S8LFF64SA, 42S8LFF64SD]



/XXX indicates active low signal.

A0 - A11	: Address Inputs
[Row : A0 - A11, Column : A0 - A10]	
DQ0 - DQ63	: Data Inputs / Outputs
/RAS0	: Row Address Strobe
/CAS0 - /CAS7	: Column Address Strobe
/WE	: Write Enable
/OE	: Output Enable
SDA	: Serial Data I/O for PD
SCL	: Clock Input for PD
Vcc	: Power Supply
GND	: Ground
NC	: No Connection

Block Diagram



Remark D0 - D7 : μPD42S65805 (8M words by 8 bits organization)

Electrical Specifications

• All voltages are referenced to GND.

• After power up ($V_{CC} \geq V_{CC\ (MIN.)}$), wait more than 100 μs (/RAS, /CAS inactive) and then, execute eight /CAS before /RAS or /RAS only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		–0.5 to +4.6	V
Supply voltage	V_{CC}		–0.5 to +4.6	V
Output current	I_O		50	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11			70	pF
	C_{I2}	/RAS0			80	
	C_{I3}	/CAS0 - /CAS7			30	
	C_{I4}	/WE			80	
	C_{I5}	/OE			80	
Data input/output capacitance	$C_{I/O}$	DQ0 - DQ63			30	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	/RAS, /CAS cycling	t_{RAC} = 50 ns		1,080	mA	1, 2, 3
		$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		920		
Standby current	I_{CC2}	/RAS, /CAS ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA			8.0	mA	
		/RAS, /CAS ≥ V_{CC}–0.2 V, I_O = 0 mA			1.6		
/RAS only refresh current	I_{CC3}	/RAS cycling, /CAS ≥ $V_{IH\ (MIN.)}$	t_{RAC} = 50 ns		1,080	mA	1, 2, 3 ,4
		$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		920		
Operating current	I_{CC4}	/RAS ≤ $V_{IL\ (MAX.)}$, /CAS cycling	t_{RAC} = 50 ns		840	mA	1, 2, 5
(Hyper page mode (EDO))		$t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		760		
/CAS before /RAS	I_{CC5}	/RAS cycling	t_{RAC} = 50 ns		1,080	mA	1, 2
refresh current		$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		920		
/CAS before /RAS long refresh current (4,096 cycles / 128 ms)	I_{CC6}	/CAS before /RAS refresh : t_{RC} = 31.3 μs /RAS, /CAS : V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V	t_{RAS} ≤ 300 ns		4.0	mA	1, 2
		Standby : /RAS, /CAS ≥ V_{CC} – 0.2 V Address : V_{IH} or V_{IL} /WE, /OE : V_{IH} I_O = 0 mA	t_{RAS} ≤ 1 μs		4.8	mA	1, 2
/CAS before /RAS self refresh current	I_{CC7}	/RAS, /CAS : t_{RASS} = 5 ms V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			3.2	mA	2
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–40	+40	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi–Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during /RAS ≤ $V_{IL\ (MAX.)}$ and /CAS ≥ $V_{IH\ (MIN.)}$.

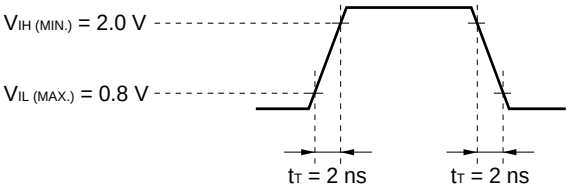
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

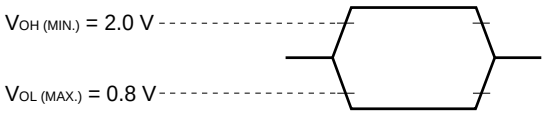
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

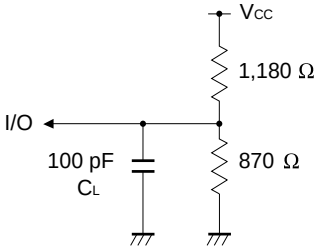
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{RC}	84	–	104	–	ns	
/RAS precharge time	t_{RP}	30	–	40	–	ns	
/CAS precharge time	t_{CPN}	7	–	10	–	ns	
/RAS pulse width	t_{RAS}	50	10,000	60	10,000	ns	1
/CAS pulse width	t_{CAS}	8	10,000	10	10,000	ns	
/RAS hold time	t_{RSH}	13	–	15	–	ns	
/CAS hold time	t_{CSH}	38	–	40	–	ns	
/RAS to /CAS delay time	t_{RCD}	11	37	14	45	ns	2
/RAS to column address delay time	t_{RAD}	9	25	12	30	ns	2
/CAS to /RAS precharge time	t_{CRP}	5	–	5	–	ns	3
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	7	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	7	–	10	–	ns	
/OE lead time referenced to /RAS	t_{OES}	0	–	0	–	ns	
/CAS to data setup time	t_{CLZ}	0	–	0	–	ns	
/OE to data setup time	t_{OLZ}	0	–	0	–	ns	
/OE to data delay time	t_{OED}	10	–	13	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	
Refresh time	t_{REF}	–	128	–	128	ms	

Notes 1. In /CAS before /RAS refresh cycles, $t_{RAS\ (MAX.)}$ is 100 μs.

If 10 μs < t_{RAS} < 100 μs, /RAS precharge time for /CAS before /RAS self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from /RAS
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to /RAS, /CAS cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from /RAS	t_{RAC}	–	50	–	60	ns	1
Access time from /CAS	t_{CAC}	–	13	–	15	ns	1
Access time from column address	t_{AA}	–	25	–	30	ns	1
Access time from /OE	t_{OEA}	–	13	–	15	ns	
Column address lead time referenced to /RAS	t_{RAL}	25	–	30	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to /RAS	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to /CAS	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from /OE	t_{OEZ}	0	10	0	13	ns	3
/CAS hold time to /OE	t_{CHO}	5	–	5	–	ns	4

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from /RAS
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ\ (MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. /WE : inactive (in read cycle)
/CAS : inactive, /OE : active ..... t_{CHO} is effective.
/RAS, /OE : active ..... t_{OCH} is effective.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
/WE hold time referenced to /CAS	t_{WCH}	7	–	10	–	ns	1
/WE pulse width	t_{WP}	7	–	10	–	ns	1
/WE lead time referenced to /RAS	t_{RWL}	13	–	15	–	ns	
/WE lead time referenced to /CAS	t_{CWL}	7	–	10	–	ns	
/WE setup time	t_{WCS}	0	–	0	–	ns	2
/OE hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	7	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the /CAS falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the /WE falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	107	–	133	–	ns	
/RAS to /WE delay time	t_{RWD}	64	–	77	–	ns	1
/CAS to /WE delay time	t_{CWD}	27	–	32	–	ns	1
Column address to /WE delay time	t_{AWD}	39	–	47	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	20	–	25	–	ns	1
/RAS pulse width	t_{RASP}	50	125,000	60	125,000	ns	
/CAS pulse width	t_{HCAS}	8	10,000	10	10,000	ns	
/CAS precharge time	t_{CP}	7	–	10	–	ns	
Access time from /CAS precharge	t_{ACP}	–	30	–	35	ns	
/CAS precharge to /WE delay time	t_{CPWD}	41	–	52	–	ns	2
/RAS hold time from /CAS precharge	t_{RHCP}	30	–	35	–	ns	
Read modify write cycle time	t_{HPRWC}	52	–	66	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	ns	
/OE to /CAS hold time	t_{OCH}	5	–	5	–	ns	3
/OE precharge time	t_{OEP}	5	–	5	–	ns	
Output buffer turn-off delay from /WE	t_{WEZ}	0	10	0	13	ns	4,5
/WE pulse width	t_{WPZ}	7	–	10	–	ns	5
Output buffer turn-off delay from /RAS	t_{OFR}	0	10	0	13	ns	4,5
Output buffer turn-off delay from /CAS	t_{OFC}	0	10	0	13	ns	4,5

Notes 1. $t_{HPC\ (MIN.)}$ is applied to /CAS access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. /WE : inactive (in read cycle)

/CAS : inactive, /OE : active ..... t_{CHO} is effective.

/CAS, /OE : active ..... t_{OCH} is effective.

4. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

5. To make DQs to Hi-Z in read cycle, it is necessary to control /RAS, /CAS, /WE, /OE as follows. The effective specification depends on state of each signal.

(1) Both /RAS and /CAS are inactive (at the end of the read cycle)

/WE : inactive, /OE : active

t_{OFC} is effective when /RAS is inactivated before /CAS is inactivated.

t_{OFR} is effective when /CAS is inactivated before /RAS is inactivated.

The slower of t_{OFC} and t_{OFR} becomes effective.

(2) Both /RAS and /CAS are active or either /RAS or /CAS is active (in read cycle)

/WE, /OE : inactive ..... t_{OEZ} is effective.

Both /RAS and /CAS are inactive or /RAS is active and /CAS is inactive (at the end of read cycle)

/WE, /OE : active and either t_{RRH} or t_{RCH} must be met ..... t_{WEZ} and t_{WPZ} are effective.

The faster of t_{OEZ} and t_{WEZ} becomes effective.

The faster of (1) and (2) becomes effective.

Refresh Cycle

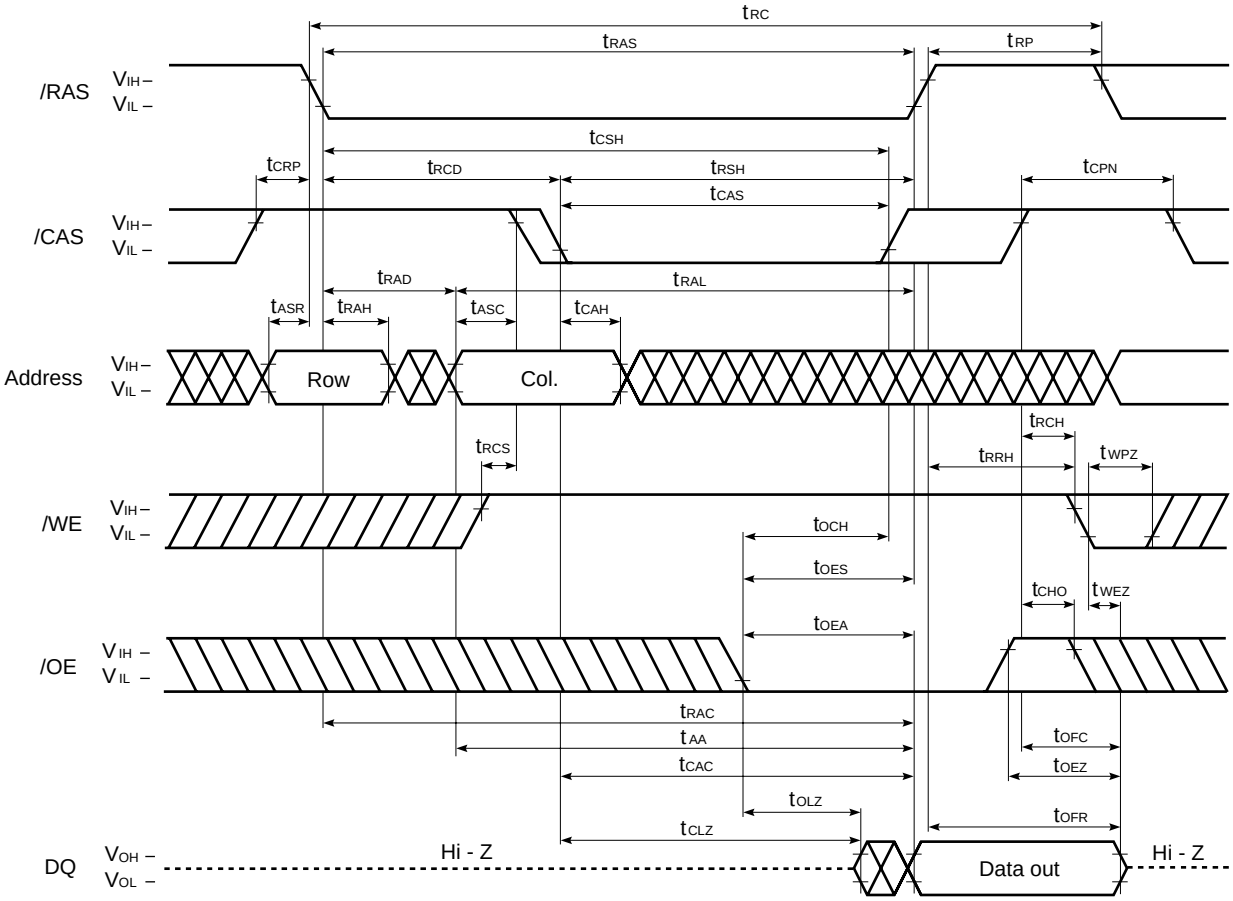
Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
/CAS setup time	t_{CSR}	5	–	5	–	ns	
/CAS hold time (/CAS before /RAS refresh)	t_{CHR}	10	–	10	–	ns	
/RAS precharge /CAS hold time	t_{RPC}	5	–	5	–	ns	
/RAS pulse width (/CAS before /RAS self refresh)	t_{RASS}	100	–	100	–	ns	
/RAS precharge time (/CAS before /RAS self refresh)	t_{RPS}	90	–	110	–	ns	
/CAS hold time (/CAS before /RAS self refresh)	t_{CHS}	–50	–	–50	–	ns	
/WE setup time	t_{WSR}	10	–	10	–	ns	
/WE hold time	t_{WHR}	15	–	15	–	ns	

Serial PD

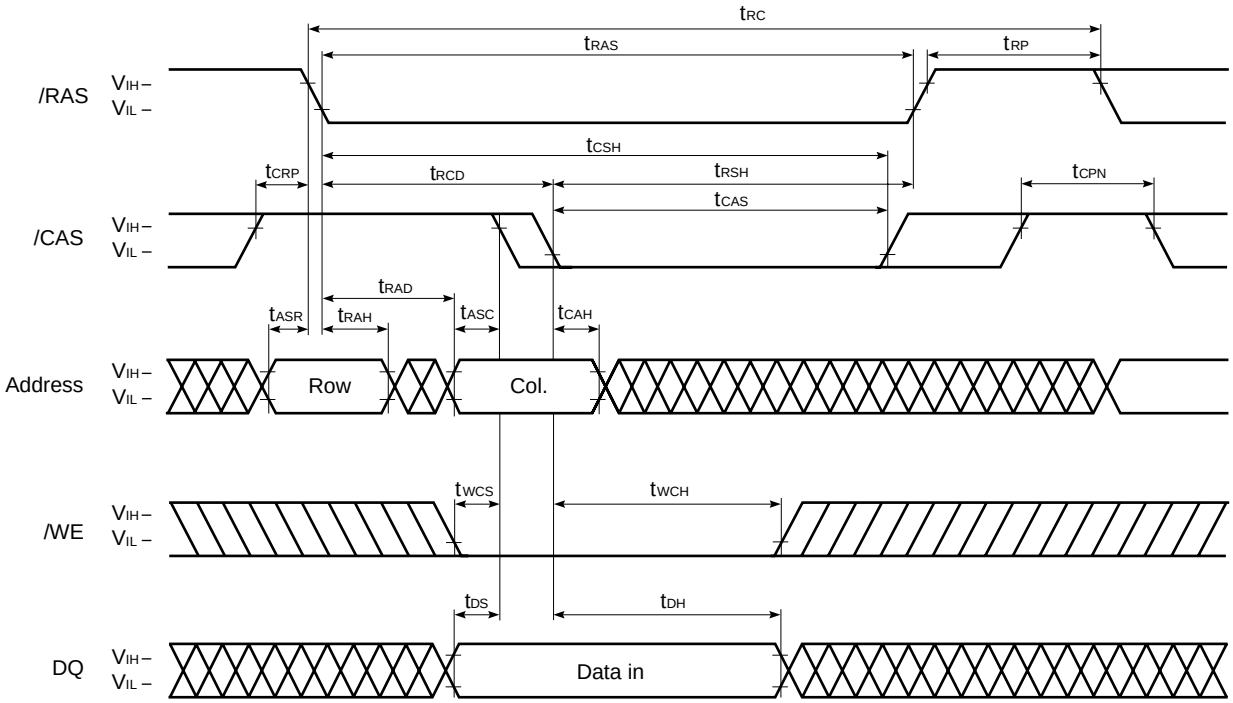
Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Number of serial PD bytes		5DH	0	1	0	1	1	1	0	1	93 bytes
1	Serial memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		02H	0	0	0	0	0	0	1	0	EDO
3	Number of rows		0CH	0	0	0	0	1	1	0	0	12 rows
4	Number of columns		0BH	0	0	0	0	1	0	1	1	11 columns
5	Number of banks		01H	0	0	0	0	0	0	0	1	1 bank
6	Data width		40H	0	1	0	0	0	0	0	0	64 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface		01H	0	0	0	0	0	0	0	1	LVTTL
9	/RAS access time	-A50	32H	0	0	1	1	0	0	1	0	50 ns
		-A60	3CH	0	0	1	1	1	1	0	0	60 ns
10	/CAS access time	-A50	0DH	0	0	0	0	1	1	0	1	13 ns
		-A60	0FH	0	0	0	0	1	1	1	1	15 ns
11	Error detection/correction		00H	0	0	0	0	0	0	0	0	None
12	Refresh period		83H	1	0	0	0	0	0	1	1	Self refresh (31.3 μs)
13	DRAM width		08H	0	0	0	0	1	0	0	0	×8
14	Error checking DRAM width		00H	0	0	0	0	0	0	0	0	None
15 - 61			00H	0	0	0	0	0	0	0	0	
62	SPD revision		01H	0	0	0	0	0	0	0	1	1
63	Checksum for bytes 0-62	-A50	8BH	1	0	0	0	1	0	1	1	
		-A60	97H	1	0	0	1	0	1	1	1	
64	Manufacture's JEDEC ID code per JEP-106E		10H	0	0	0	1	0	0	0	0	
65-71			00H	0	0	0	0	0	0	0	0	
72	Manufacturing location											
73	Part name		34H	0	0	1	1	0	1	0	0	
74	Part name		32H	0	0	1	1	0	0	1	0	
75	Part name		53H	0	1	0	1	0	0	1	1	
76	Part name		38H	0	0	1	1	1	0	0	0	
77	Part name		4CH	0	1	0	0	1	1	0	0	
78	Part name		46H	0	1	0	0	0	1	1	0	
79	Part name		46H	0	1	0	0	0	1	1	0	
80	Part name		36H	0	0	1	1	0	1	1	0	
81	Part name		34H	0	0	1	1	0	1	0	0	
82	Part name		53H	0	1	0	1	0	0	1	1	
★ 83	Part name	MC-42S8LFF64SA	41H	0	1	0	0	0	0	0	1	
		MC-42S8LFF64SD	44H	0	1	0	0	0	1	0	0	
84	Part name		44H	0	1	0	0	0	1	0	0	
85	Part name		41H	0	1	0	0	0	0	0	1	
86	Part name	-A50	35H	0	0	1	1	0	1	0	1	
		-A60	36H	0	0	1	1	0	1	1	0	
87	Part name		30H	0	0	1	1	0	0	0	0	
88	Part name		20H	0	0	1	0	0	0	0	0	
89	Part name		20H	0	0	1	0	0	0	0	0	
90	Part name		20H	0	0	1	0	0	0	0	0	
91	PCB revision code		31H	0	0	1	1	0	0	0	1	
92	Blank		20H	0	0	1	0	0	0	0	0	

Remark 1 : High level (Serial data), 0 : Low level (Serial data)

Read Cycle

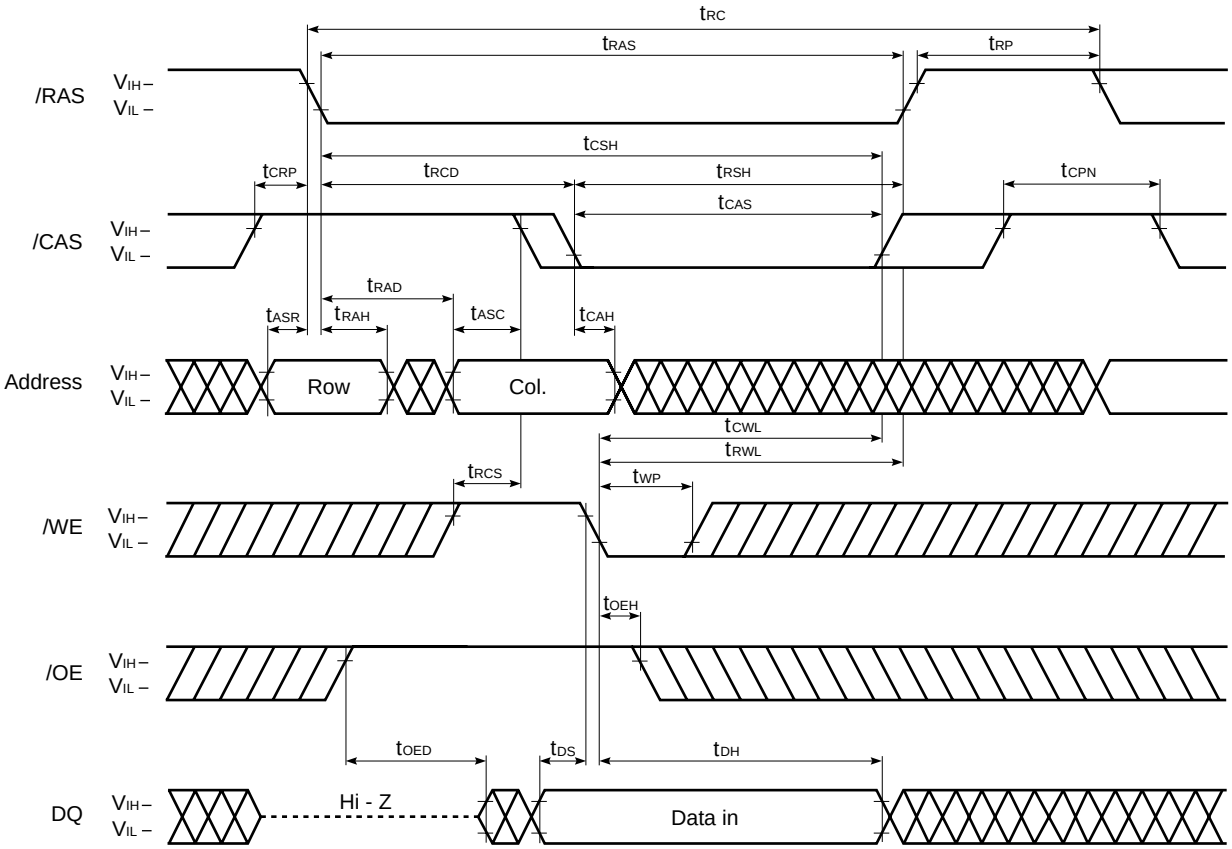

tRC
tRAS
tRP
/RAS
VIH –
VIL –
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
/CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
/WE
tOCH
tOES
tCHO
tWEZ
/OE
tOEA
tRAC
tAA
tCAC
tOFC
tOEZ
tOLZ
tOFR
tCLZ
DQ
VOH –
VOL –
Hi - Z
Data out
Hi - Z

Early Write Cycle

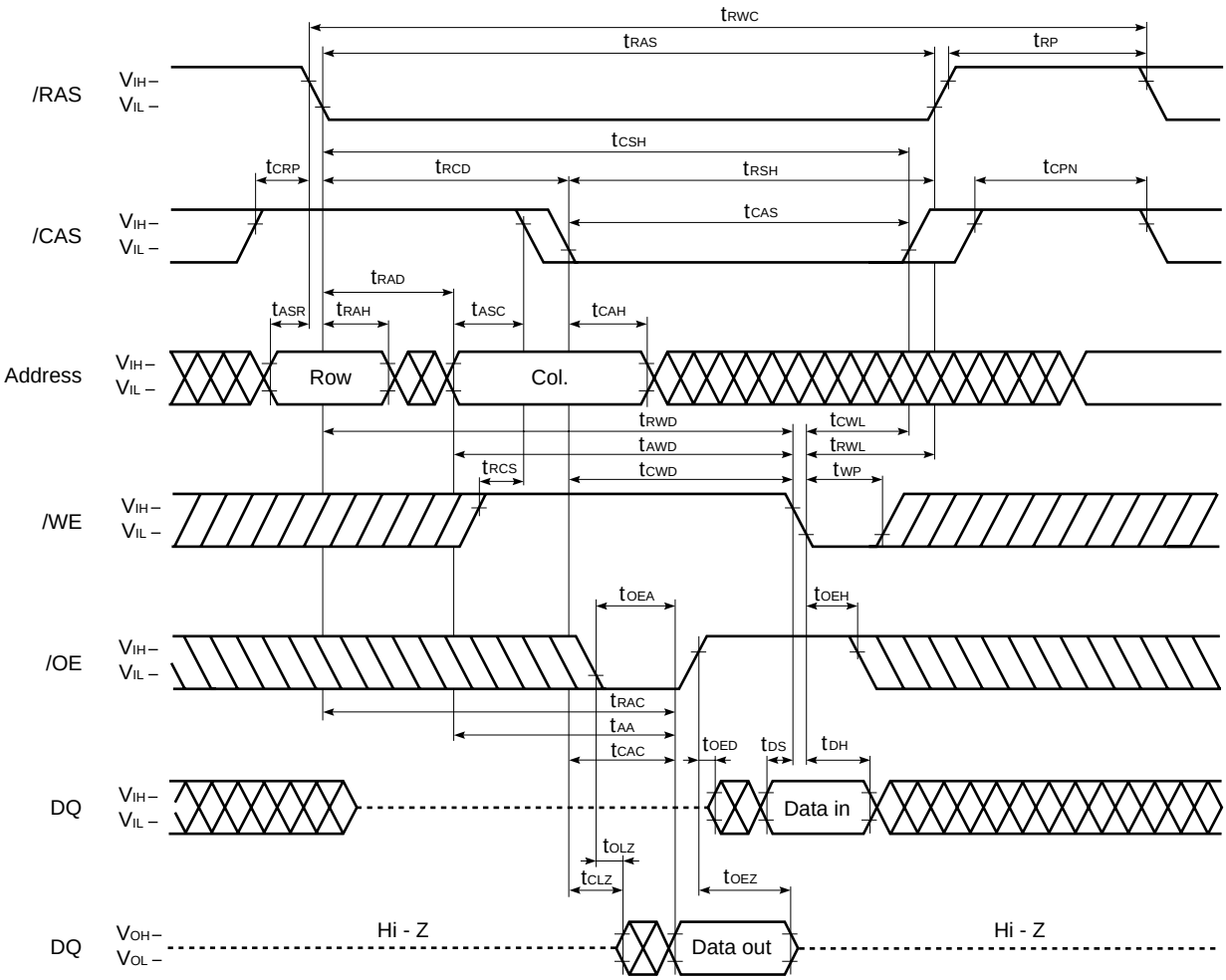


Remark /OE : Don't care

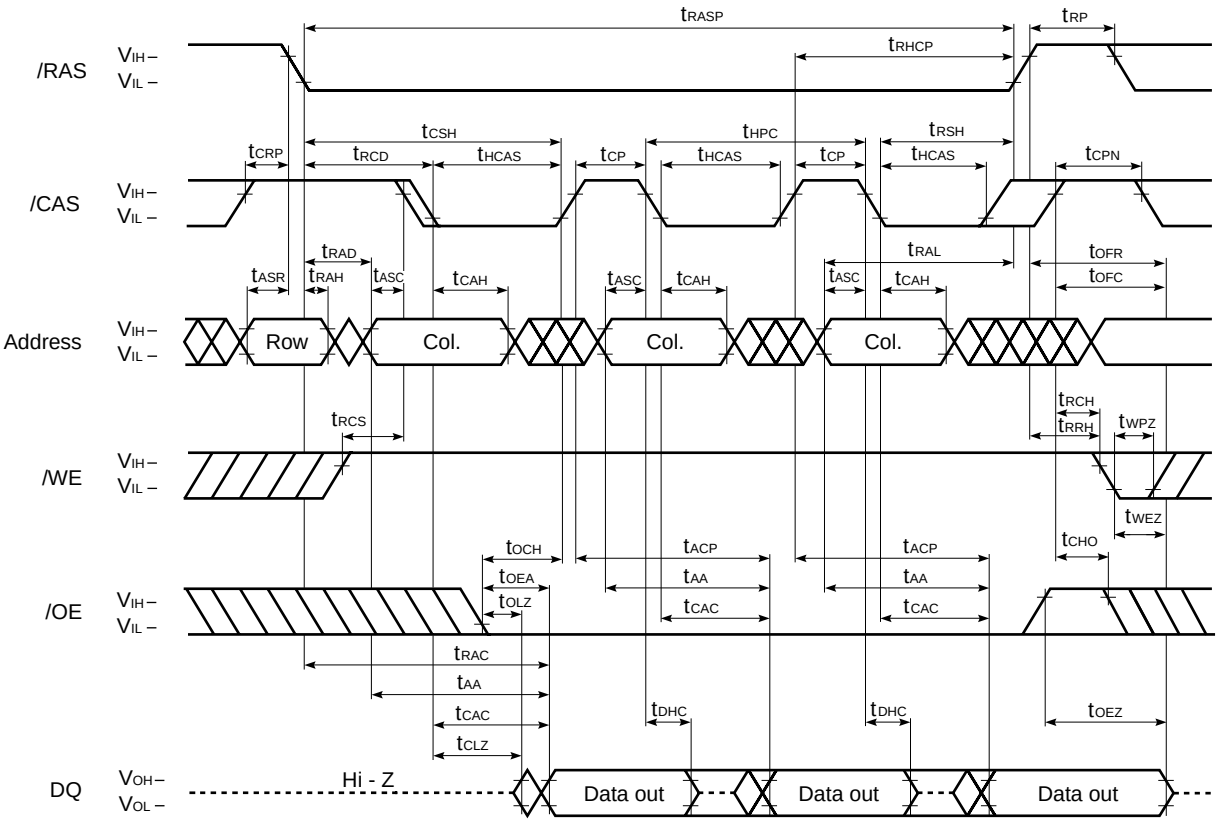
Late Write Cycle



Read Modify Write Cycle

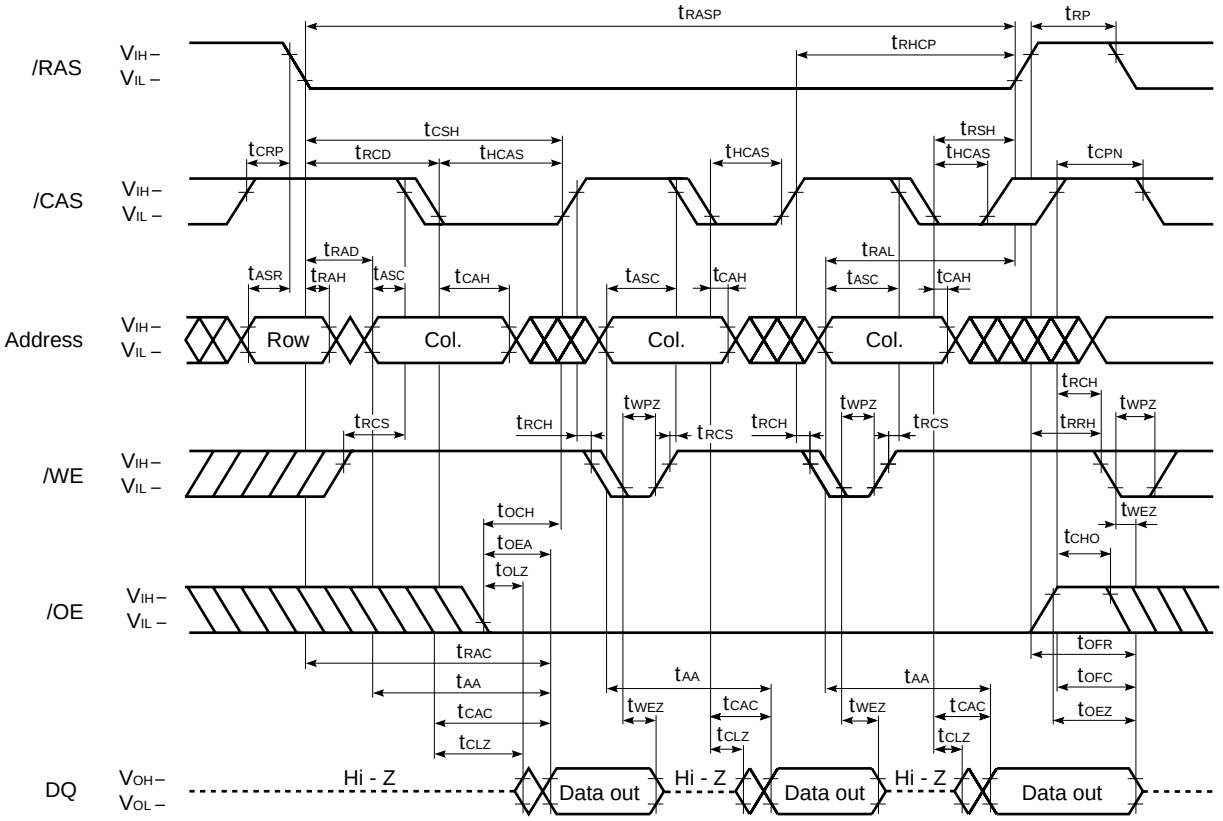


Hyper Page Mode (EDO) Read Cycle



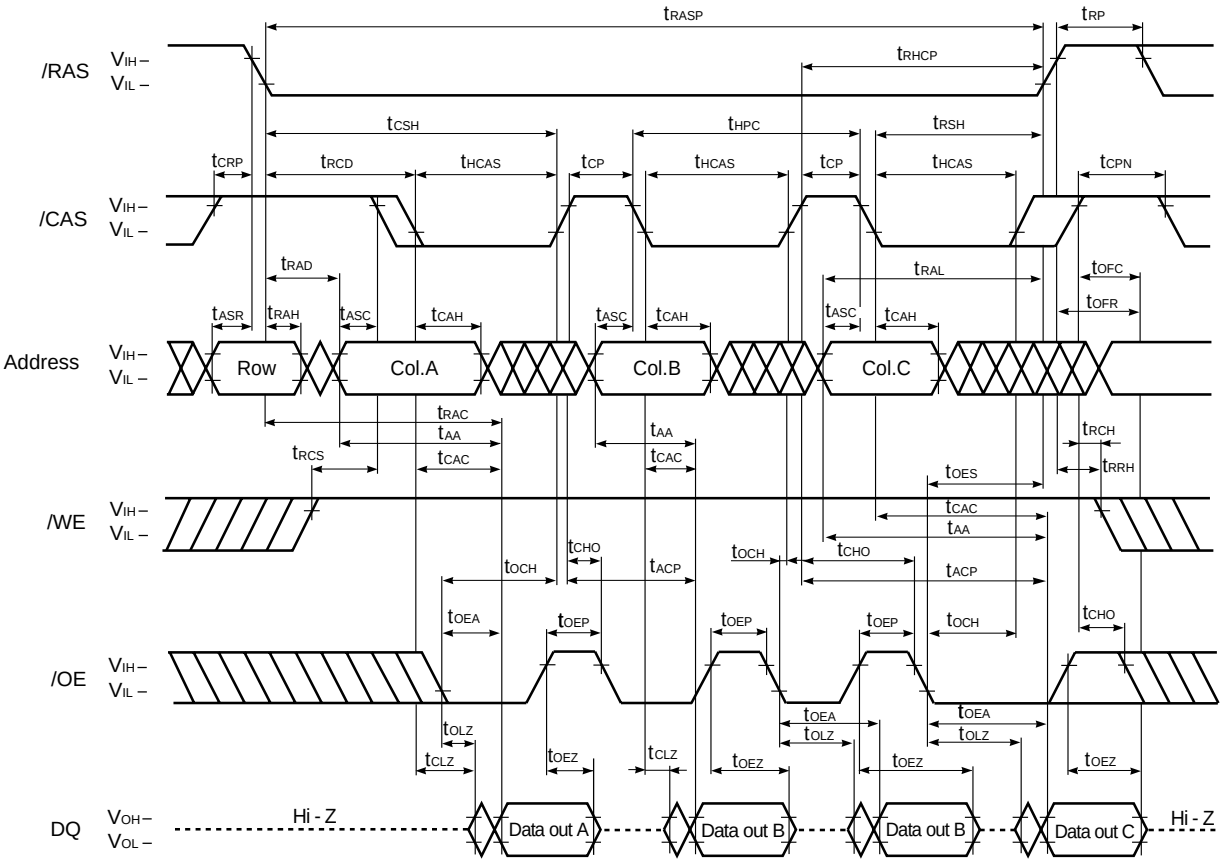
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

Hyper Page Mode (EDO) Read Cycle (/WE Control)



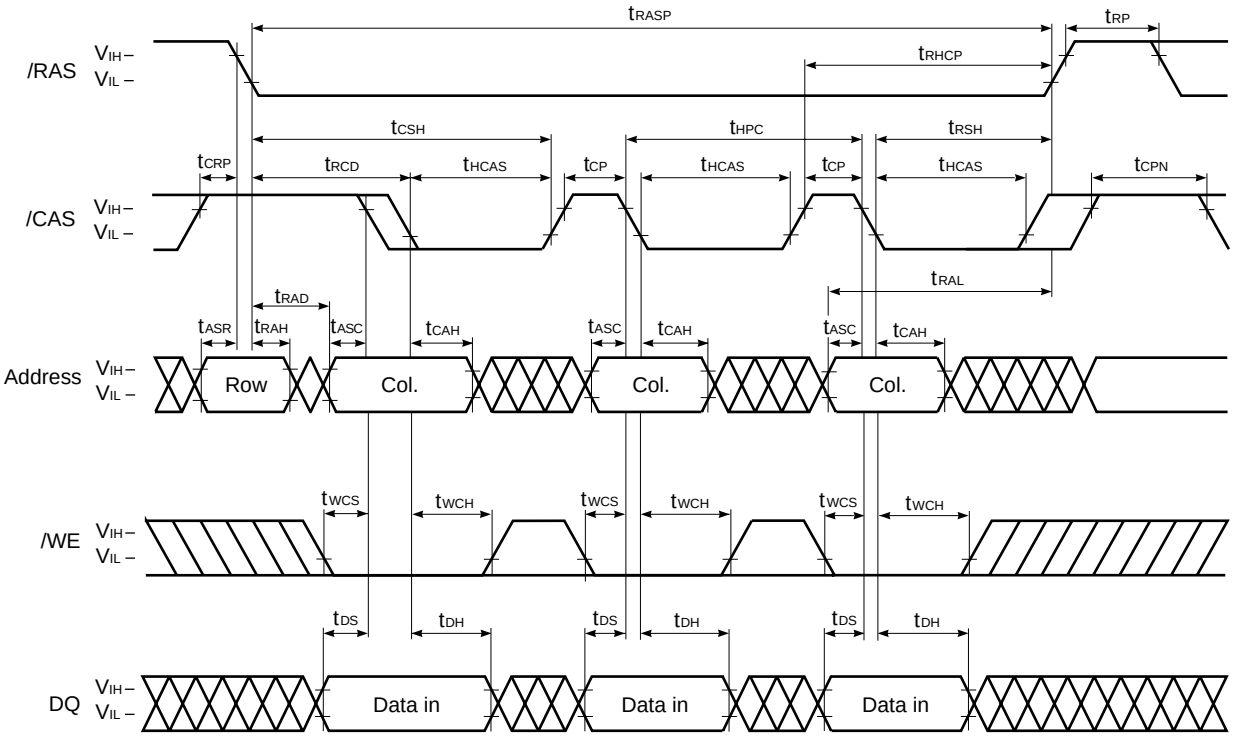
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

Hyper Page Mode (EDO) Read Cycle (/OE Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

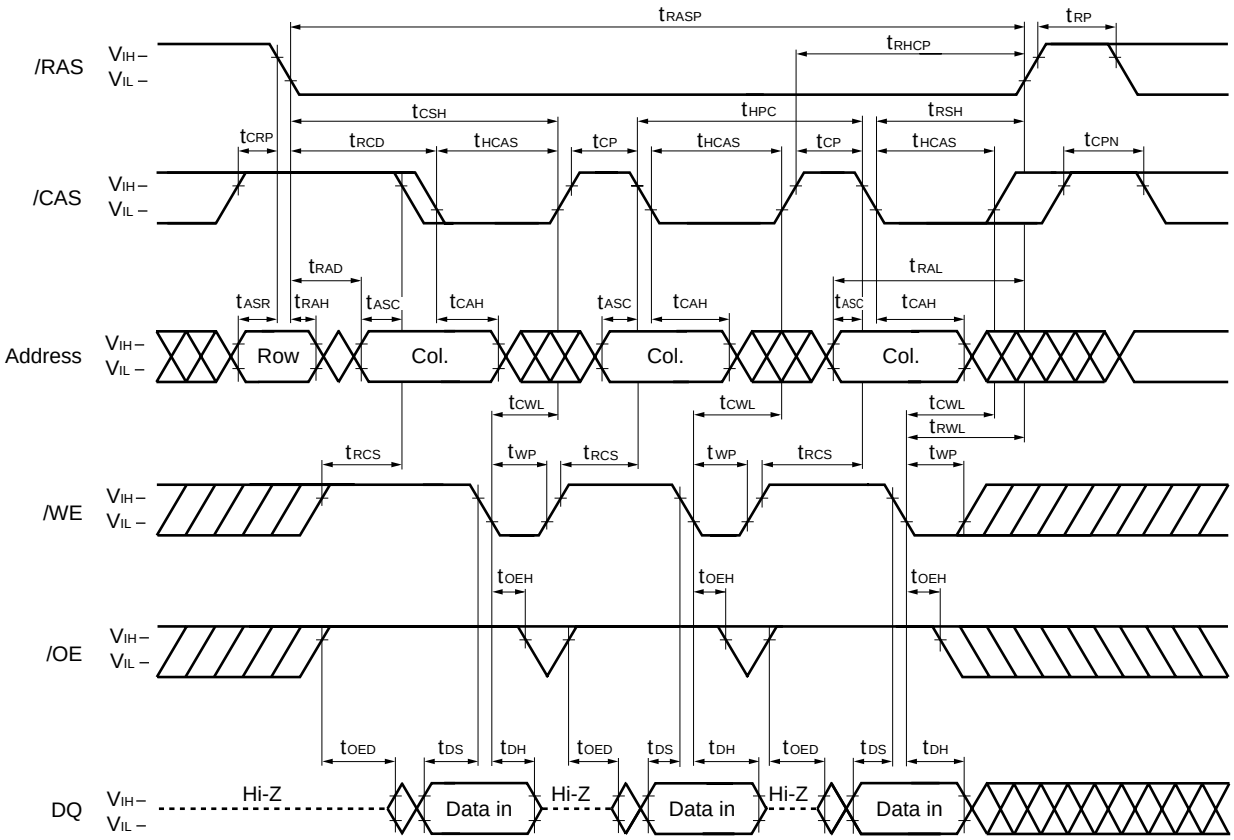
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. /OE : Don't care

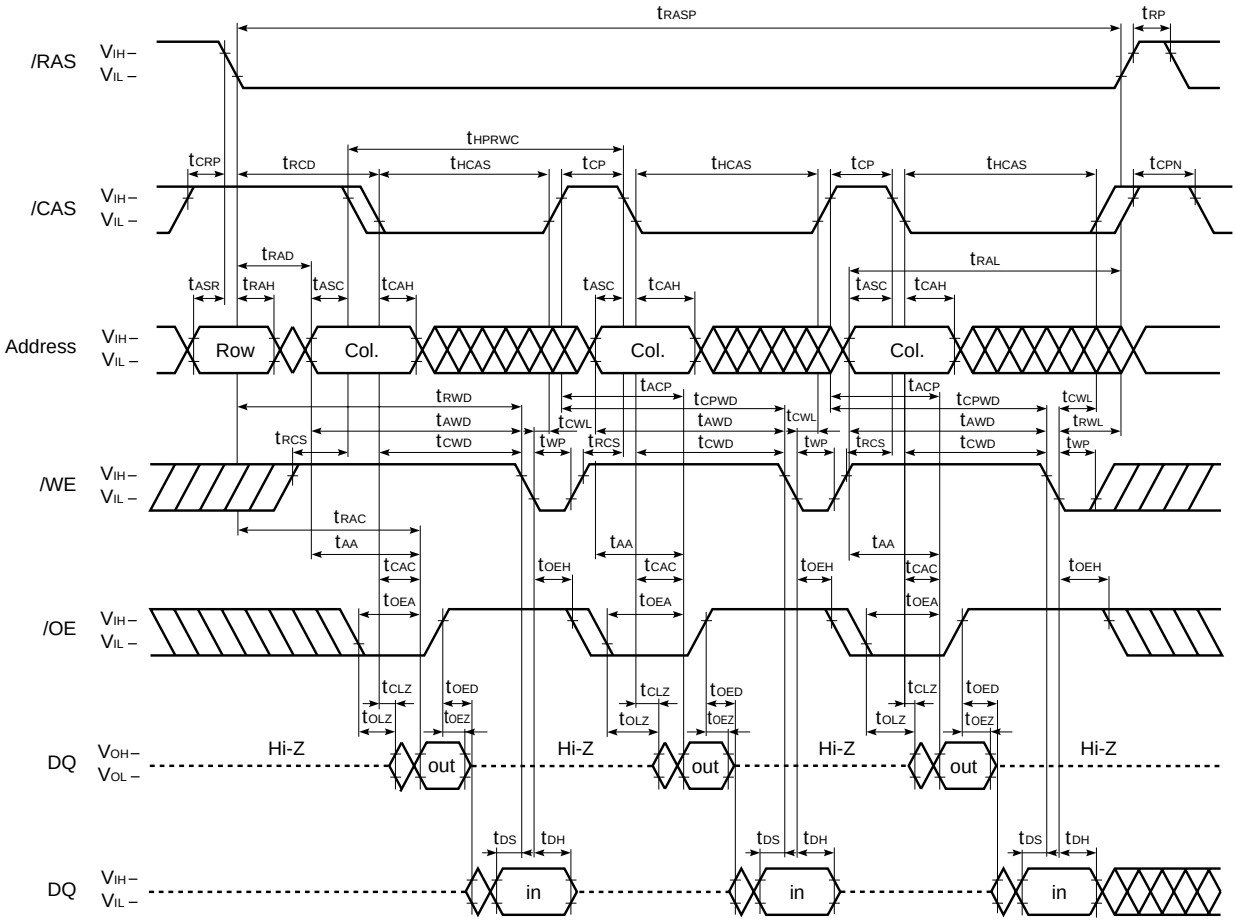
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

Hyper Page Mode (EDO) Late Write Cycle



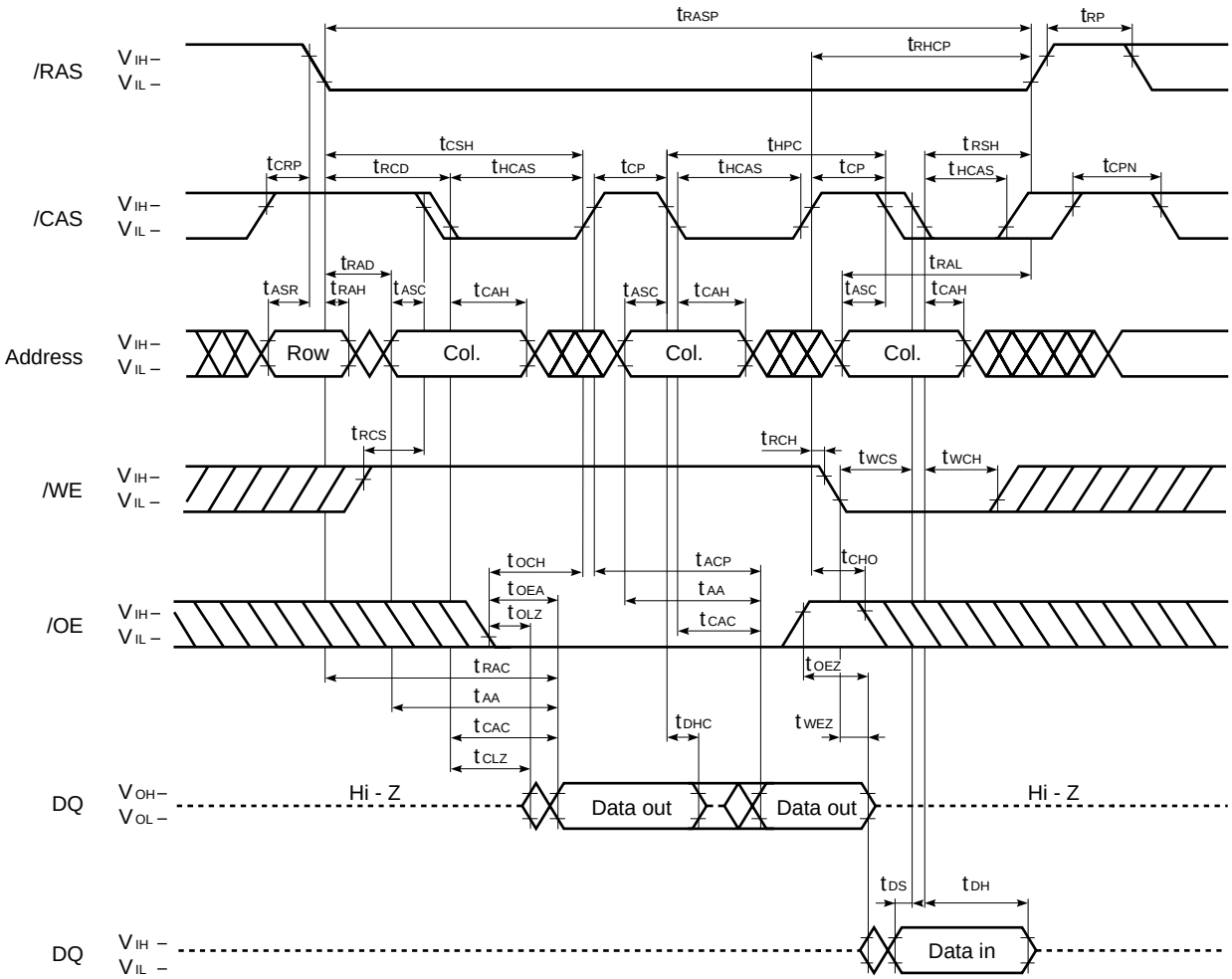
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

Hyper Page Mode (EDO) Read Modify Write Cycle



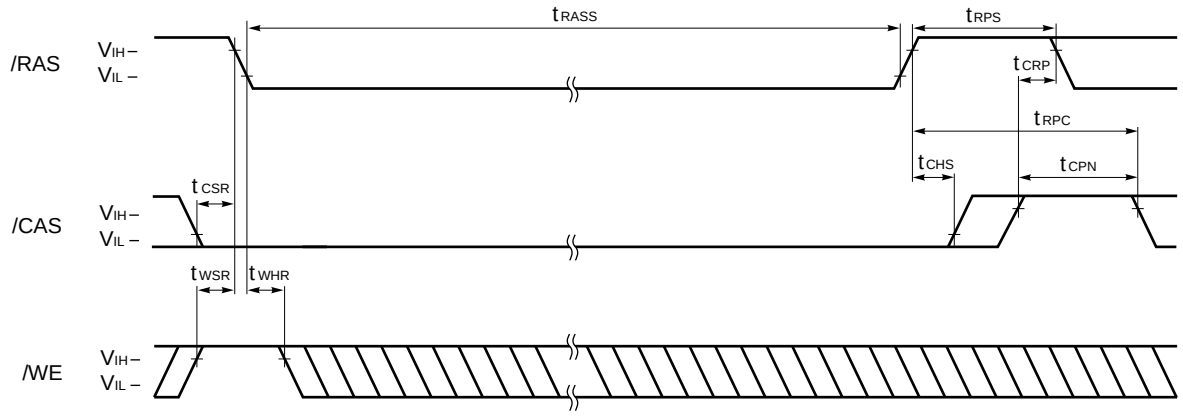
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

Hyper Page Mode (EDO) Read and Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

/CAS Before /RAS Self Refresh Cycle



Remark Address, /OE : Don't care DQ : Hi-Z

Cautions on Use of /CAS before /RAS Self Refresh

/CAS before /RAS self refresh can be used independently when used in combination with distributed /CAS before /RAS long refresh; However, when used in combination with burst /CAS before /RAS long refresh or with long /RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of /CAS Before /RAS Self Refresh and Burst /CAS Before /RAS Long Refresh

When /CAS before /RAS self refresh and burst /CAS before /RAS long refresh are used in combination, please perform /CAS before /RAS refresh 4,096 times within a 64 ms interval just before and after setting /CAS before /RAS self refresh.

(2) Normal Combined Use of /CAS Before /RAS Self Refresh and Long /RAS Only Refresh

When /CAS before /RAS self refresh and /RAS only refresh are used in combination, please perform /RAS only refresh 4,096 times within a 64 ms interval just before and after setting /CAS before /RAS self refresh.

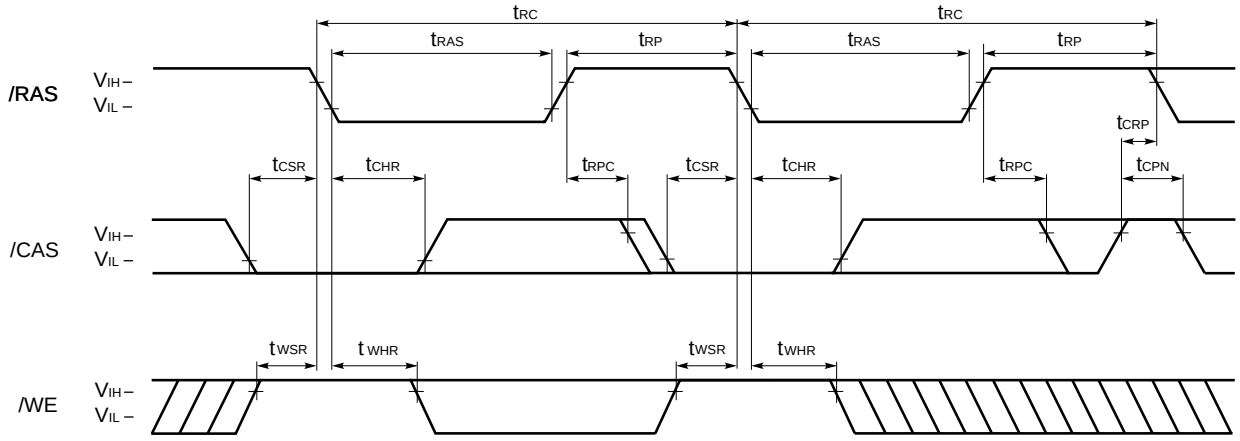
(3) If $t_{RASS(MIN.)}$is not satisfied at the beginning of /CAS before /RAS self refresh cycles (t_{RAS} < 100 μs), /CAS before /RAS refresh cycles will be executed one time.

If 10 μs < t_{RAS} < 100 μs, /RAS precharge time for /CAS before /RAS self refresh (t_{RPS}) is applied.

And refresh cycles (4,096 / 128 ms) should be met.

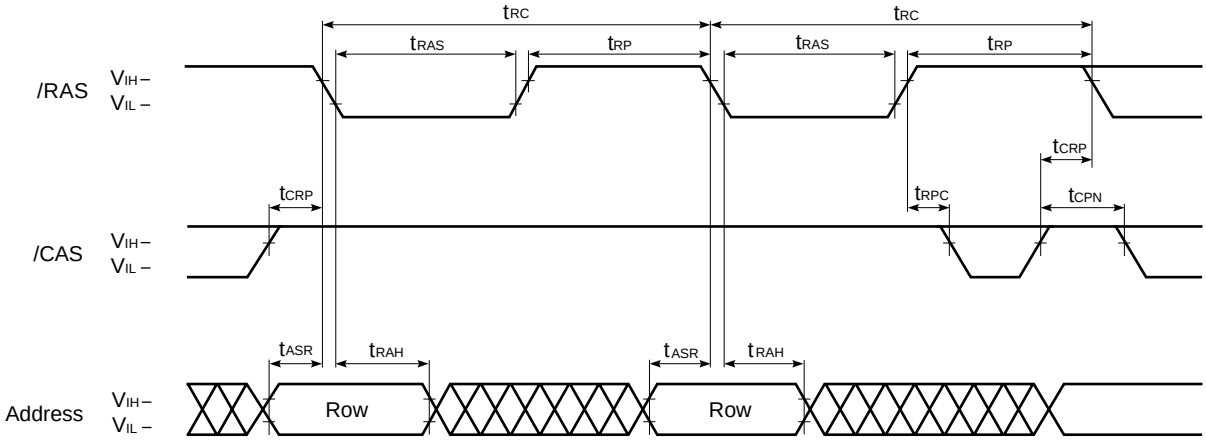
For details, please refer to **How To Use DRAM User's Manual.**

/CAS Before /RAS Refresh Cycle



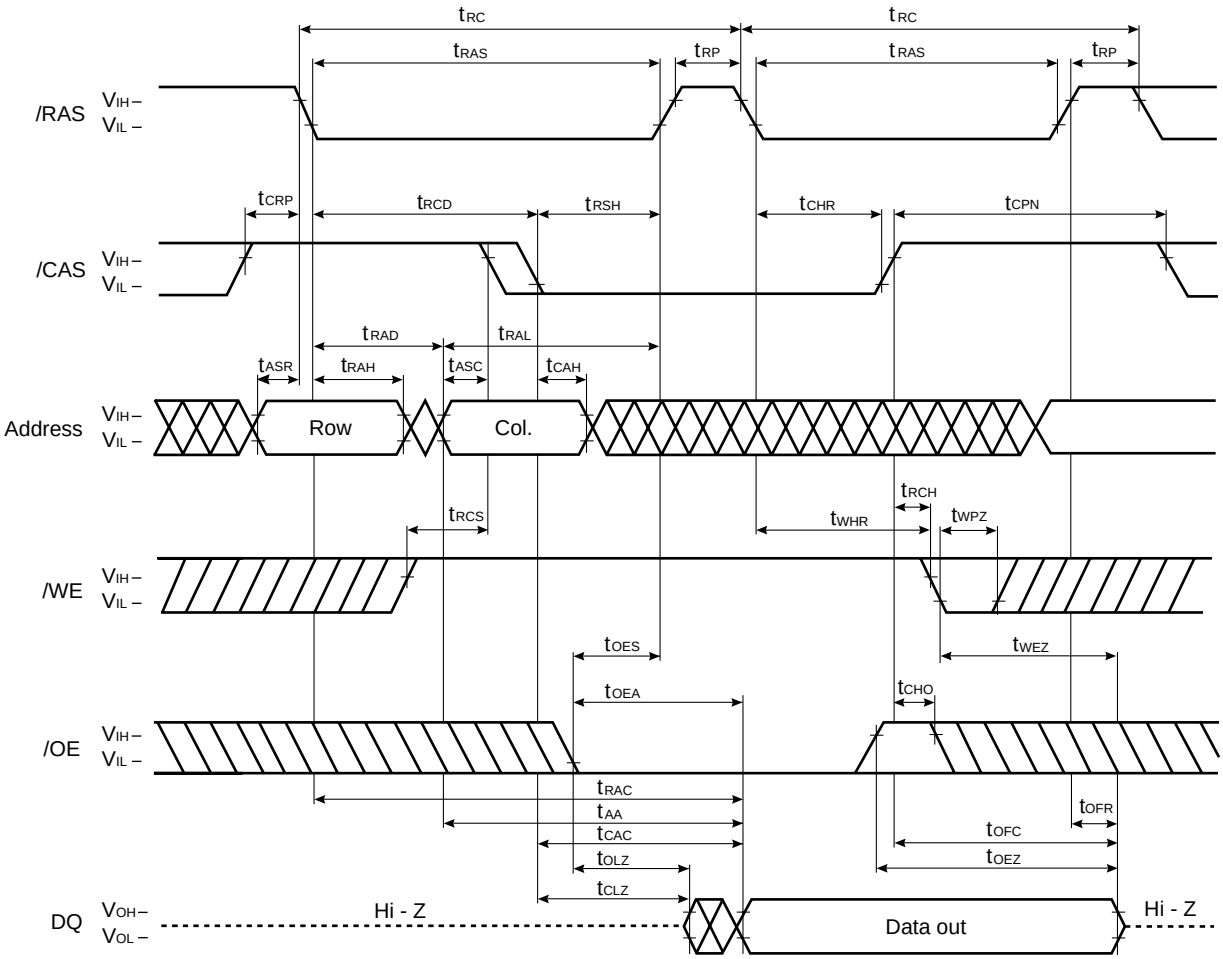
Remark Address, /OE : Don't care DQ : Hi-Z

/RAS Only Refresh Cycle

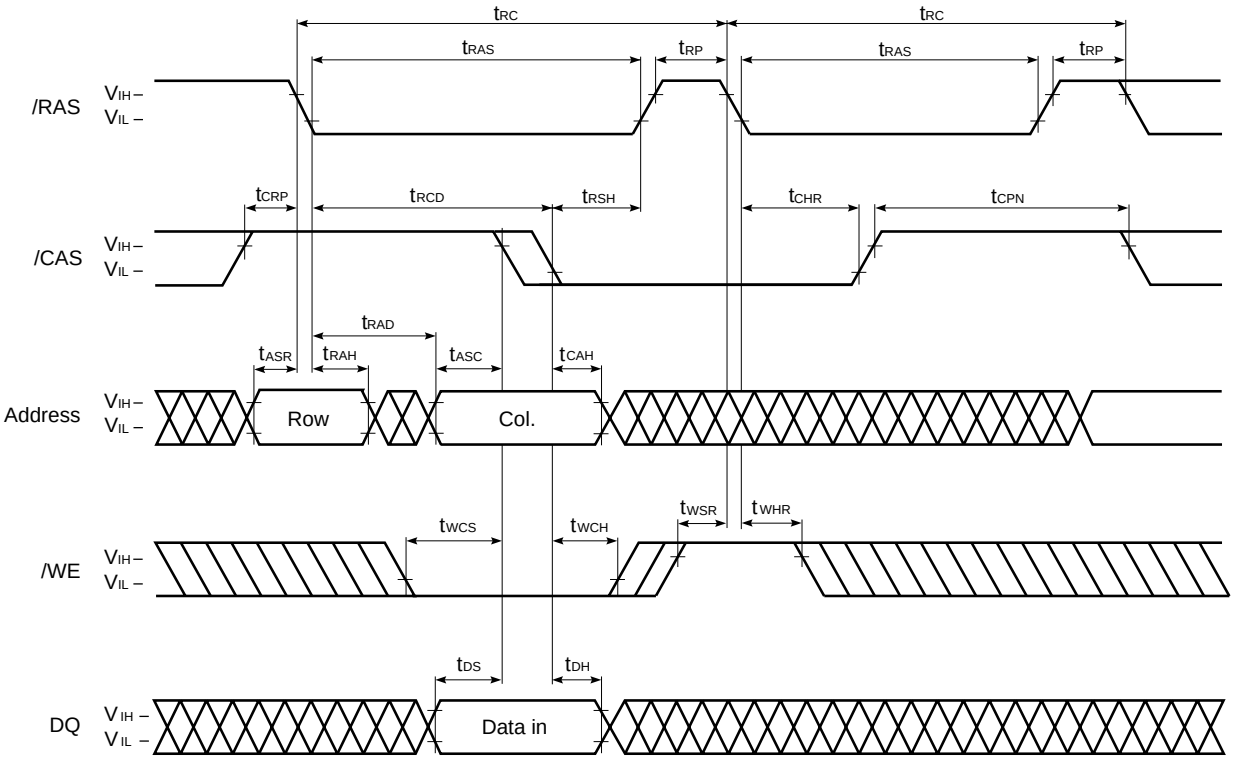


Remark /WE, /OE : Don't care DQ : Hi-Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

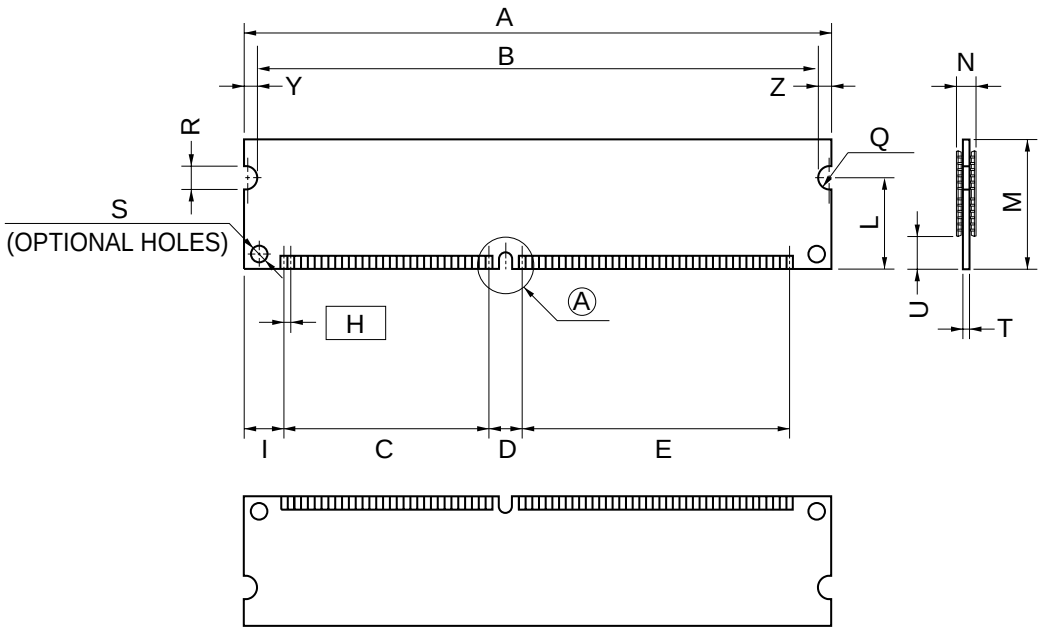


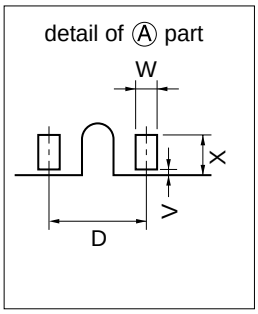
Remark /OE : Don't care

Package Drawing

[MC-42S8LFF64SA]

144 PIN SMALL OUTLINE DUAL IN-LINE MODULE (SOCKET TYPE)

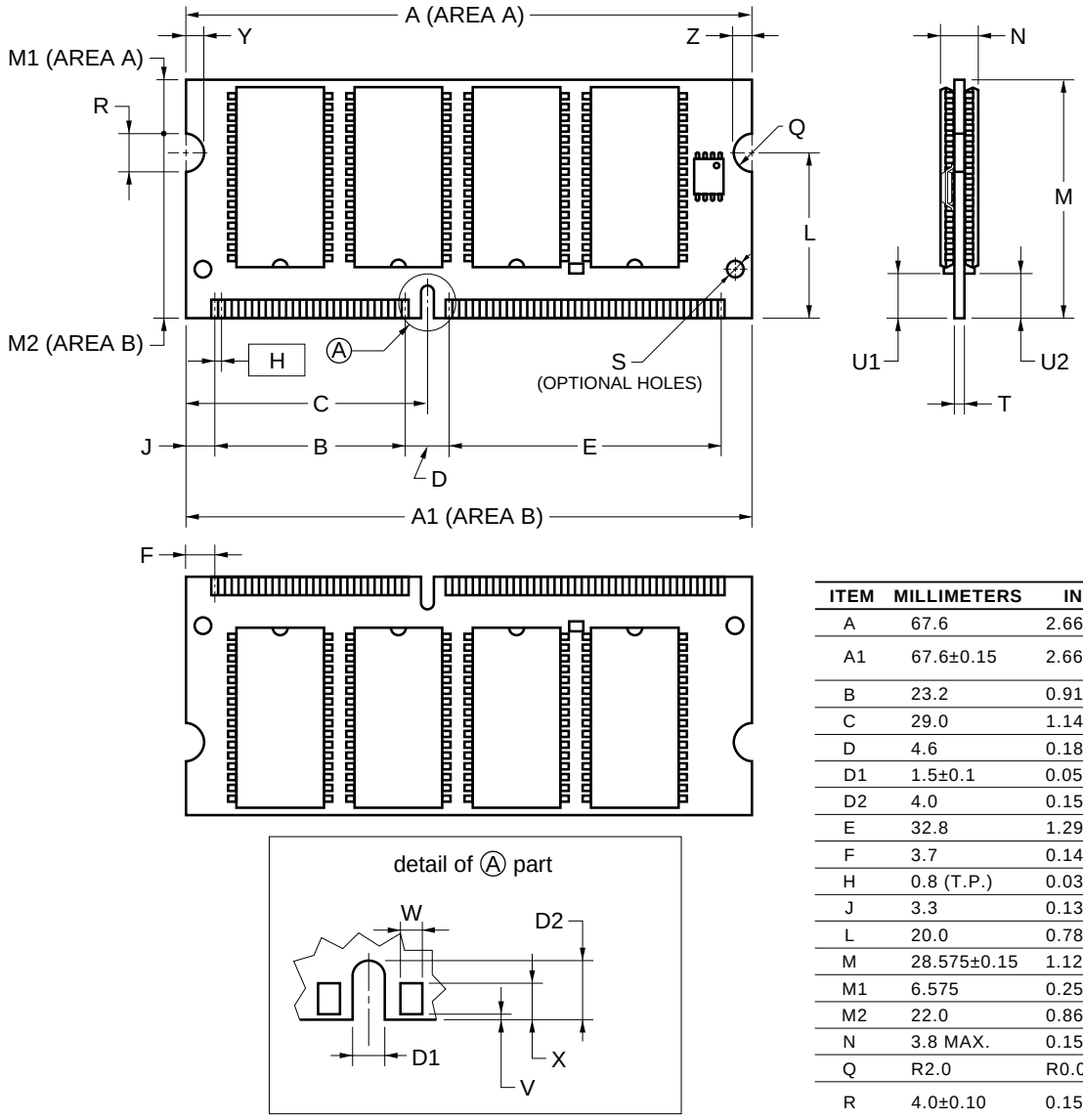




ITEM	MILLIMETERS
A	67.45 ~ 67.75
B	63.60
C	23.20 ± 0.05
D	4.60 ± 0.05
E	32.80 ± 0.05
H	0.80 (T.P.)
I	3.30
L	20.00
M	25.40 ± 0.15
N	3.80 (MAX.)
Q	R2.00
R	4.00 ± 0.10
S	1.8
T	0.9 ~ 1.10
U	3.20
V	0.25 (MAX.)
W	0.60 ± 0.05
X	2.55 (MIN.)
Y	2.00 (MIN.)
Z	2.00 (MIN.)

★ **[MC-42S8LFF64SD]**

144 PIN DUAL IN-LINE MODULE (SOKET TYPE)



ITEM	MILLIMETERS	INCHES
A	67.6	2.661
A1	67.6±0.15	$2.661^{+0.007}_{-0.006}$
B	23.2	0.913
C	29.0	1.142
D	4.6	0.181
D1	1.5±0.1	0.059±0.004
D2	4.0	0.157
E	32.8	1.291
F	3.7	0.146
H	0.8 (T.P.)	0.031 (T.P.)
J	3.3	0.13
L	20.0	0.787
M	28.575±0.15	1.125±0.006
M1	6.575	0.259
M2	22.0	0.866
N	3.8 MAX.	0.15 MAX.
Q	R2.0	R0.079
R	4.0±0.10	$0.157^{+0.005}_{-0.004}$
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U1	3.2 MIN.	0.125 MIN.
U2	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.01 MAX.
W	0.6±0.05	$0.024^{+0.002}_{-0.003}$
X	2.55 MIN.	0.100 MIN.
Y	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.

M144S-80A2

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed imme-diately after power-on for devices having reset function.

[MEMO]

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

M4 96.5