IMSG170

High Performance CMOS Color look-up table

inmos®

Preliminary

FEATURES

- Compatible with the RS 170A video standard
- Pixel rates up to 50 MHz
- 256K possible colors
- Single monolithic, high performance CMOS
- Pixel address mask
- RGB analog output, 6 bit DAC per gun, composite blank + sync
- Low DAC glitch energy
- Video signal output into 75 ohms
- TTL compatible inputs
- Micropocessor compatible write interface
- Single +5V ± 10% power supply
- Low power dissipation, 750mW max at maximum pixel rate
- Standard 600 mil 28 pin DIP package

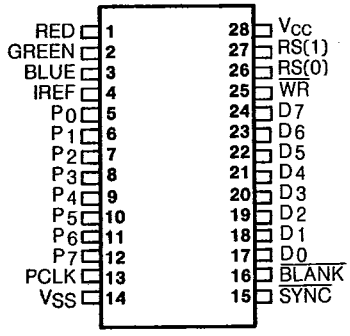
DESCRIPTION

The IMSG170 integrates the function of a color look-up table (or color palette), digital-analog convertors (with 75Ω outputs) and microprocessor interface into a single 28 pin package.

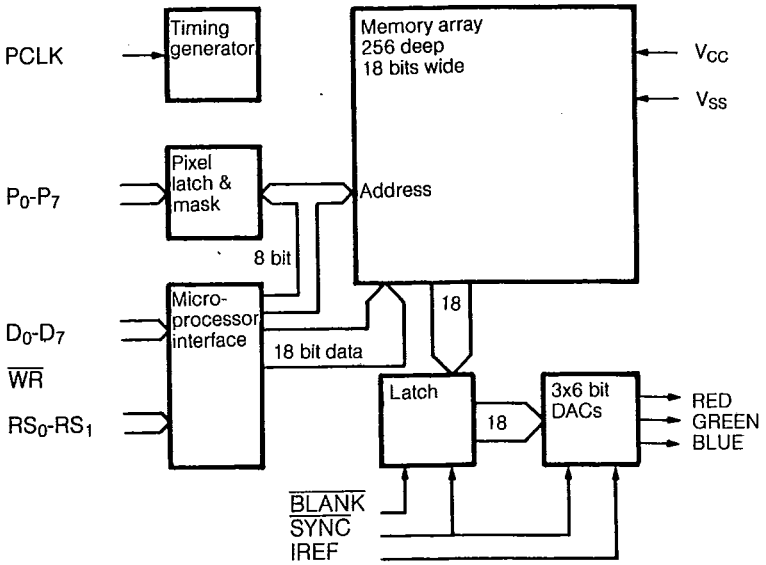
At any time, a set of up to 256 colors may be selected for display from a palette of 256K. The IMSG170 significantly reduces component cost, board area, and power consumption.

The pixel word mask allows displayed colors to be changed in a single write cycle rather than by modifying the look-up table.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES	
P_0-P_7	Pixel address inputs
D_0-D_7	Program data inputs
RS_0-RS_1	Register select
RED, GREEN, BLUE	Analog video outputs
PCLK	Pixel clock
$\overline{WR}$	Write enable
$\overline{BLANK}$	Video blanking input
$\overline{SYNC}$	Video sync input
IREF	Reference current
V_{CC}	+5 volt supply input
V_{SS}	Ground

FUNCTIONAL DESCRIPTION

PIXEL INTERFACE

SIGNAL	PIN	INPUT/ OUTPUT	SIGNAL NAME	DESCRIPTION
PCLK	13	Input	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address, Blanking and Sync inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the Color Look-Up Table to the analog outputs.
P_0-P_7	5-12	Input	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel Mask Register and then used as the address into the Color Look-Up Table. This causes an internal 18 bit wide color value to be produced.
$\overline{BLANK}$	16	Input	Blanking	A low value on this input, when sampled, will cause a color value of zero to be applied to the inputs of the DACs regardless of the color value of the current pixel.
$\overline{SYNC}$	15	Input	Sync	The value on this input, when sampled, controls an offset on the analog outputs, the offset being 30% of the full scale analog output. If $\overline{SYNC}$ is low there is no offset, if $\overline{SYNC}$ is high the offset is active.

ANALOG INTERFACE

SIGNAL	PIN	INPUT/ OUTPUT	SIGNAL NAME	DESCRIPTION
RED, GREEN, BLUE	1 2 3	Output Output Output	Red, Green, Blue,	These three signals are the outputs of three 6 bit DACs. Each DAC is composed of 90 current sources whose outputs are summed. 63 of the current sources are controlled by the binary input to the DACs, 27 are controlled by the $\overline{SYNC}$ signal.
IREF	4	Input	Reference Current	The Reference Current drawn from V_{CC} via the IREF pin determines the current sourced by each of the current sources in the DACs. Each current source producing 1/30 of IREF when turned on.

MICROPROCESSOR INTERFACE

SIGNAL	PIN	INPUT/ OUTPUT	SIGNAL NAME	DESCRIPTION
$\overline{WR}$	25	Input	Write Enable	The Write Enable signal controls the timing of write operations to the microprocessor interface. A minimum high period for the Write Enable signal is specified in terms of the Pixel Clock period allowing the two signals to be asynchronous.
RS_0-RS_1	26-27	Input	Register Select	The values on these inputs are sampled on the falling edge of the Write Enable signal, they specify which one of the three internal registers is to be written to next. See internal Register description for the function of these three registers.
D_0-D_7	17-24	Input	Program Data	On the rising edge of Write Enable the byte value on the Program Data inputs is written to the specified register.

T-52-33-09

INTERNAL REGISTERS

RS_1	RS_0	SIZE (BITS)	REGISTER NAME	DESCRIPTION
0	0	8	Pixel Address	The Pixel Address register is written with an 8 bit value to address a location within the Color Look-Up Table.
0	1	18	Color Value	The Color Value register is internally an 18 bit wide register. The 18 bit value is formed by the concatenation of the least significant 6 bits from each of 3 bytes written to the Color Value register. The first value written will be applied to the red DAC, the second to the green DAC and the third to the blue DAC. After the third byte is written to the Color Value register the 18 bit word will be written to the location in the Color Look-Up Table specified by the current contents of the Pixel Address register. The Pixel Address register is then incremented.
1	Don't Care	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P_0-P_7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, a zero setting that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the Microprocessor Interface when the look-up table is being modified.

DEVICE DESCRIPTION

The IMSG170 is intended for use as the output stage of raster scan video systems. It contains a high speed random access store of 256 x 18 bit words, three 6 bit high speed DAC's, a microprocessor interface and a pixel word mask.

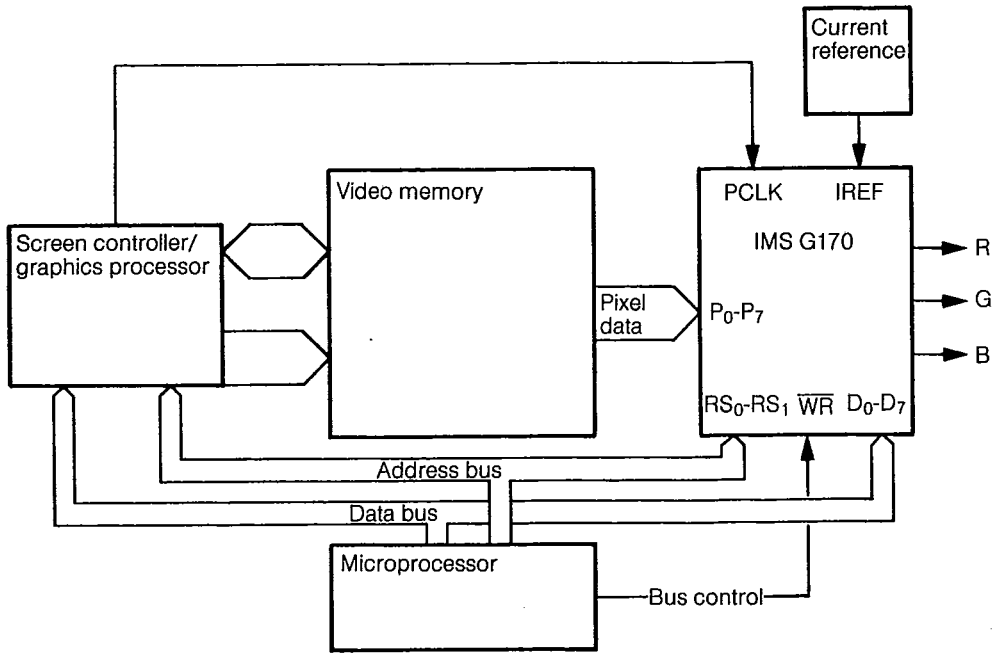
An 8 bit value read in on the Pixel Address input is used as a read address for the store and results in an 18 bit data word. This data is partitioned as three fields of 6 bits, with each field being applied to the inputs of a 6 bit DAC.

Pixel rates of up to 50 MHz are achieved by pipelining the memory access over two clock periods.

Externally generated sync and blanking signals can be input to the IMSG170, these signals act on all three of the analog outputs. The $\overline{SYNC}$ and $\overline{BLANK}$ signals are delayed internally by pipelining so that they appear at the analog outputs with the correct relationship to the pixel address stream.

The contents of the look up table can be modified via an 8 bit wide microprocessor interface. The use of an internal synchronizing circuit allows operations on the interface to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes of the effective contents of the Color Look-Up Table to facilitate such operations as animation and flashing objects.



VIDEO PATH

Pixel Address, $\overline{SYNC}$ and $\overline{BLANK}$ inputs are sampled on the rising edge of Pixel Clock and appear at the analog outputs after two further rising edges of Pixel Clock.

ANALOG OUTPUTS

The outputs of the DACs are intended to produce 1 volt peak white amplitude (i.e., 0.7 volts swing and 0.3 volts sync as specified by RS170A) when driving a 75 ohm load and when a 4.44 mA IREF is supplied.

The $\overline{BLANK}$ and $\overline{SYNC}$ inputs to the IMSG170 act on all three of the analog outputs. When the $\overline{BLANK}$ input is low a binary zero is applied to the inputs of the DACs. When the $\overline{SYNC}$ input is low an offset on the analog outputs of 30% of the full scale output current is removed. The $\overline{BLANK}$ and $\overline{SYNC}$ inputs can be operated independently of each other.

The expressions for peak white voltage/output loading combinations are given below:

1) Composite sync ($\overline{SYNC}$ going low to generate sync pulses on the analog outputs)

$$\text{V peak white} = \frac{\text{IREF} \times 90 \times \text{Rload}}{30}$$

$$\text{V black level} = \frac{\text{IREF} \times 27 \times \text{Rload}}{30}$$

2) Separate sync ($\overline{SYNC}$ continuously low)

$$\text{V peak white} = \frac{\text{IREF} \times 63 \times \text{Rload}}{30}$$

Vblack level = 0

MICROPROCESSOR INTERFACE

There are three internal registers in the IMSG170. These are:

RS1	RS0	Register
0	0	Pixel Address
0	1	Color Value
1	0	Pixel Mask

The Pixel Address register is used to specify the location in the look-up table to be written with a color value. The Color Value register contains the data used to update the contents of the location specified by the Pixel Address register. The Pixel Mask register is an 8 bit register. The value in the mask register is bitwise ANDed with the incoming pixel address to give a masked pixel address.

The microprocessor interface is asynchronous with the video path, the timing of operations on the interface registers being controlled by the Write Enable signal ($\overline{WR}$). On the falling edge of this signal the register select lines are sampled, and on the rising edge the values on the data bus are sampled. To allow for the internal synchronization of the written data with the video path, Write Enable must be high for at least three Pixel Clock cycles between write operations. Each time a new color value is written to the Look-Up Table to modify its contents the write cycle will replace the color value read cycle for one pixel.

To write a new color value to the table a pixel address must be specified and then an 18 bit data word written to that location in the Table.

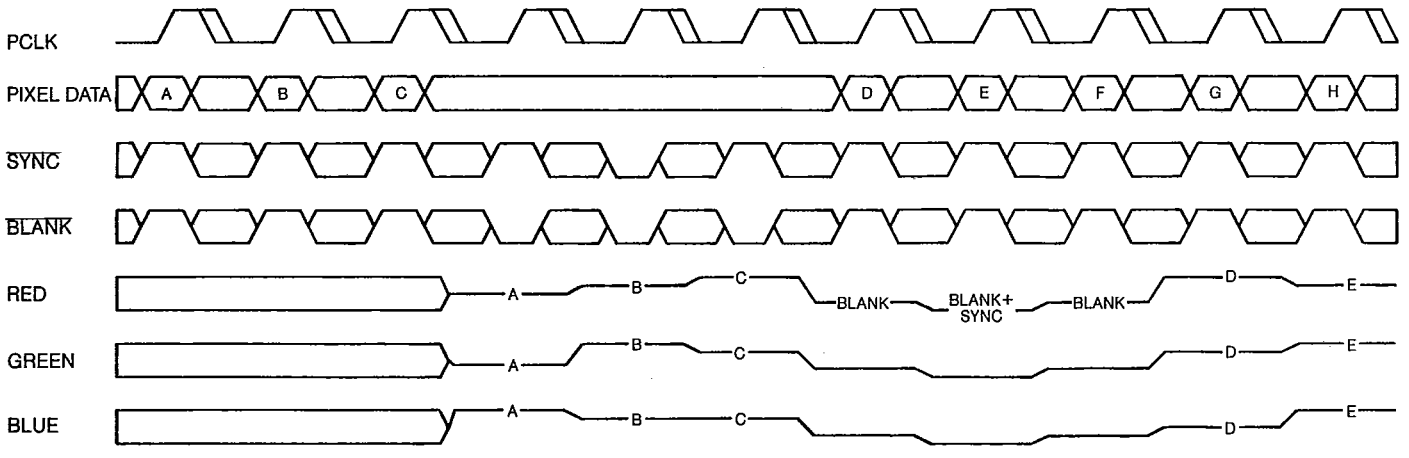
Locations in the Look-Up Table can be specified in two ways. The first is to write a pixel address and then perform a color value write sequence. The second method is to write an initial pixel address and then (as the Pixel Address register increments after every color value write sequence) write a succession of new color values for the range of pixel addresses to be written.

A color value write sequence is three successive byte writes to the Color Value register. The least significant 6 bits are taken from each byte written and concatenated into an 18 bit word. The first byte written will define the red intensity, the second the green and the last the blue.

The pixel address used to access the Color Look-Up Table is the result of the bitwise ANDing of the incoming pixel address and contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory or the look-up table contents. Thus, by partitioning the color definitions by one or more bits in the pixel address rapid animation and flashing objects can be produced.

In the event that the Pixel Address register is modified during a color value write sequence the Color Value register is initialized, aborting any unfinished write sequence.

The Pixel Mask register is independant of the Pixel Address and Color Value registers.



ABSOLUTE MAXIMUM RATINGS[a]

Voltage on V_{CC} 7.0V
Voltage on Other Pin . . . . V_{SS} −0.5V to V_{CC} +0.5V
Temperature Under Bias . . . . . −40°C to 85°C
Storage Temperature (Ambient) . . . −65°C to 150°C
Power Dissipation 1W
Reference Current . . . . . −15mA
Analog Output Current (Per Output) 45mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS[a]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	Volts	
V_{SS}	Ground		0		Volts	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC} +0.5	Volts	
V_{IL}	Input Logic "0" Voltage	−0.5		0.8	Volts	−2.0 V Min for 20 ns pulse width
T_A	Ambient Operating Temperature	0		70	°C	

DC ELECTRICAL CHARACTERISTICS[a, b] (0°C ≤ T_A ≤ +70°C) (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	Average Power Supply Current		150	mA	c
IREF	Reference Current	−1.5	−7	mA	d
VO max	Maximum Output Voltage	2		V	e, $I_O \leq$ 10mA
I_O max	Maximum Output Current	21		mA	e, $V_O \leq$ 1V
	Full Scale Accuracy	±5		%	e
	Sync Accuracy	29	31	%	g
	Differential Accuracy	±1		%	h
	Linearity	±0.5		LSB	i

AC TEST CONDITIONS

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 2.5ns
Input Timing Reference Level 1.5V

AC ELECTRICAL CHARACTERISTICS[a]

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ± 10%)

PARAMETER	MIN	MAX	UNITS	NOTES
Rise Time (10% to 90%)		8	ns	j
Full Scale Settling Time		20	ns	j,k,f
Glitch Energy		400	pVsec	f

Note a: All voltages in this data sheet are with respect to V_{SS} unless specified otherwise.
Note b: The Pixel Clock frequency must be stable for a period of at least 20μS after power-up (or after a change in Pixel Clock frequency) before proper device operation is achieved.
Note c: Pixel Clock frequency = 50 MHz (Io = Io max)
Note d: Reference currents below the minimum specified may cause the analog outputs to become invalid.
Note e: $\overline{SYNC} \geq V_{IH}$ (min).
Note f: This parameter is sampled, not 100% tested.
Note g: Sync current is nominally 30% of peak white current.
Note h: Between different analog outputs on the same device.
Note i: Monotonicity guaranteed.
Note j: Load = 75 Ω + 30 pF.
Note k: To within 1% of full scale voltage.

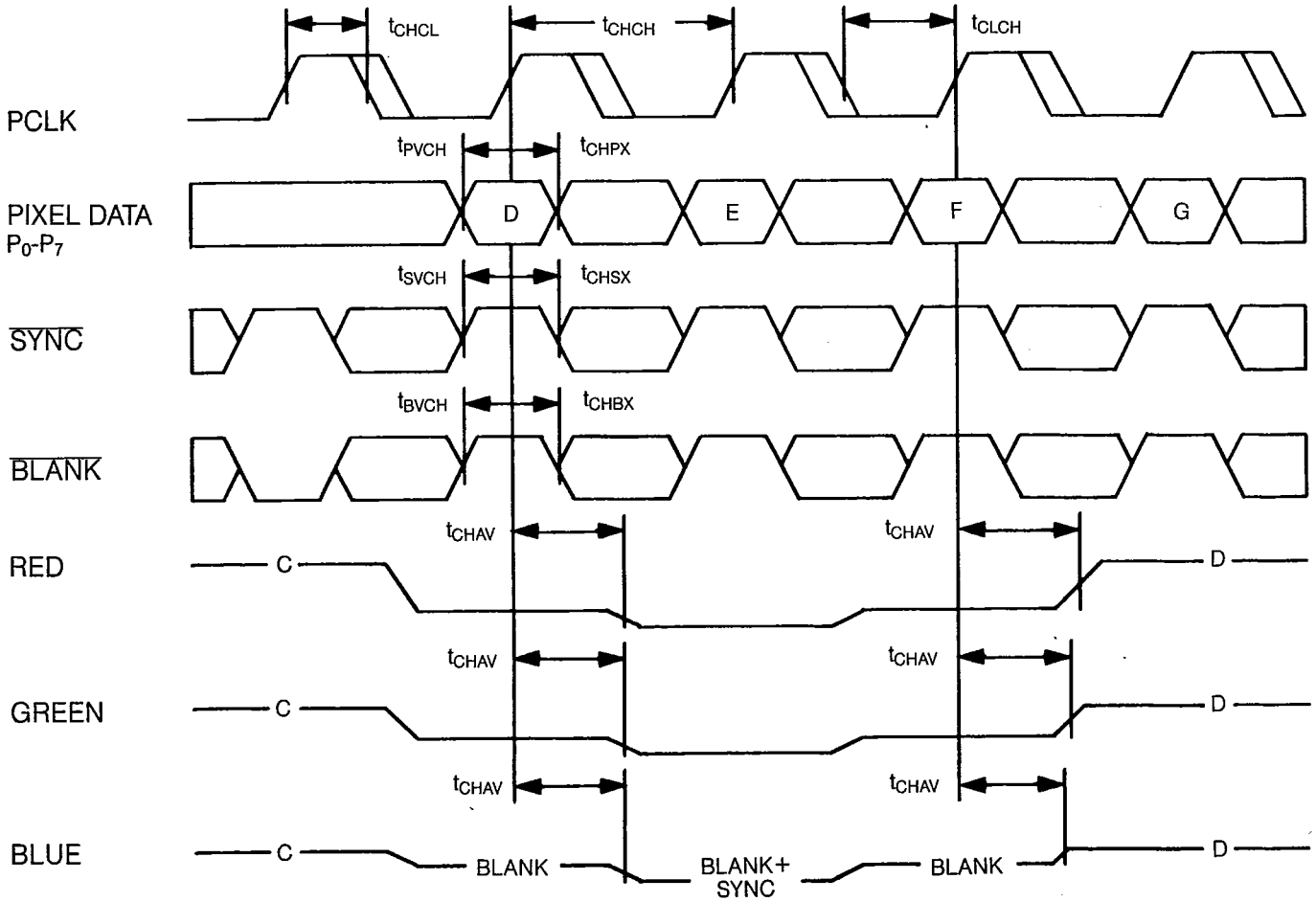
VIDEO OPERATION

AC OPERATING CONDITIONS: V_{CC} = +5.0V ± 10%, 0°C ≤ T_A ≤ 70°C[b]

SYMBOL	PARAMETER	IMSG170-50		IMSG170-35		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{CHCH}	PCLK Period	20	10000	28	10000	ns	
Δt_{CHCH}	PCLK Jitter		±2.5		±2.5	%	n
t_{CLCH}	PCLK Width Low	6	10000	9	10000	ns	
t_{CHCL}	PCLK Width High	6	10000	9	10000	ns	
t_{PVCH}	Pixel Word Setup Time	3		4		ns	
t_{CHPX}	Pixel Word Hold Time	3		4		ns	
t_{SVCH}	$\overline{SYNC}$ Setup Time	3		4		ns	
t_{BVCH}	$\overline{BLANK}$ Setup Time	3		4		ns	
t_{CHSX}	$\overline{SYNC}$ Hold Time	3		4		ns	
t_{CHBX}	$\overline{BLANK}$ Hold Time	3		4		ns	
t_{CHAV}	PCLK to Valid DAC Output	15	30	15	45	ns	o
Δt_{CHAV}	Differential Output Delay		1		1	ns	p
	Pixel Clock Transition Time		50		50	ns	

Note n: This parameter for allowed variation in the Pixel Clock frequency does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (t_{CHCH}) period specified above.
Note o: A valid analog output is defined as when the changing analog signal is half way between its successive values.
Note p: Between different analog outputs on the same device.

VIDEO TIMING



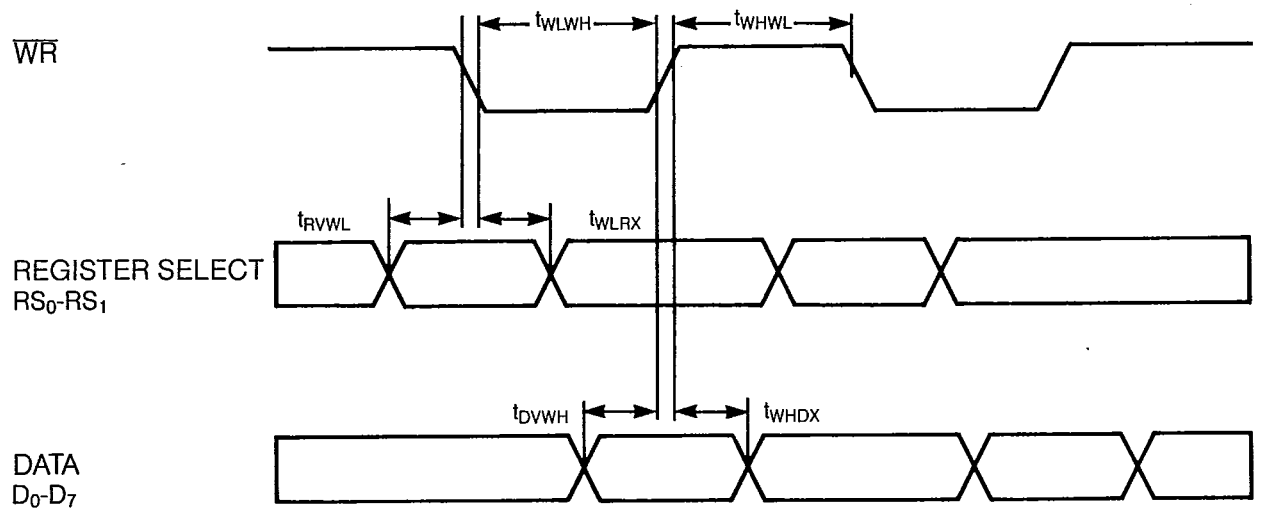
MICROPROCESSOR INTERFACE: WRITE CYCLE TIMING T-52-33-09

AC OPERATING CONDITIONS: V_{CC} = +5.0V ± 10%, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	IMSG170-50		IMSG170-35		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{WLWH}	$\overline{WR}$ Pulse Width Low	50		50		ns	
t_{WHWL}	$\overline{WR}$ Pulse Width High	3*t_{CHCH}		3*t_{CHCH}		ns	m
t_{RVWL}	Register Select Setup Time	10		15		ns	
t_{WLRX}	Register Select Hold Time	10		15		ns	
t_{DVWH}	Data Setup Time	10		15		ns	
t_{WHDX}	Data Hold Time	10		15		ns	
	Write Enable Transition Time		50		50	ns	

Note m: The parameter t_{WHWL} allows for the write data to be synchronized with the pixel clock, hence this parameter is expressed in terms of the pixel clock period t_{CHCH}.

WRITE CYCLE TIMING



Note: device charaterization is underway. The values given here represent a design goal and are subject to change.

APPLICATION

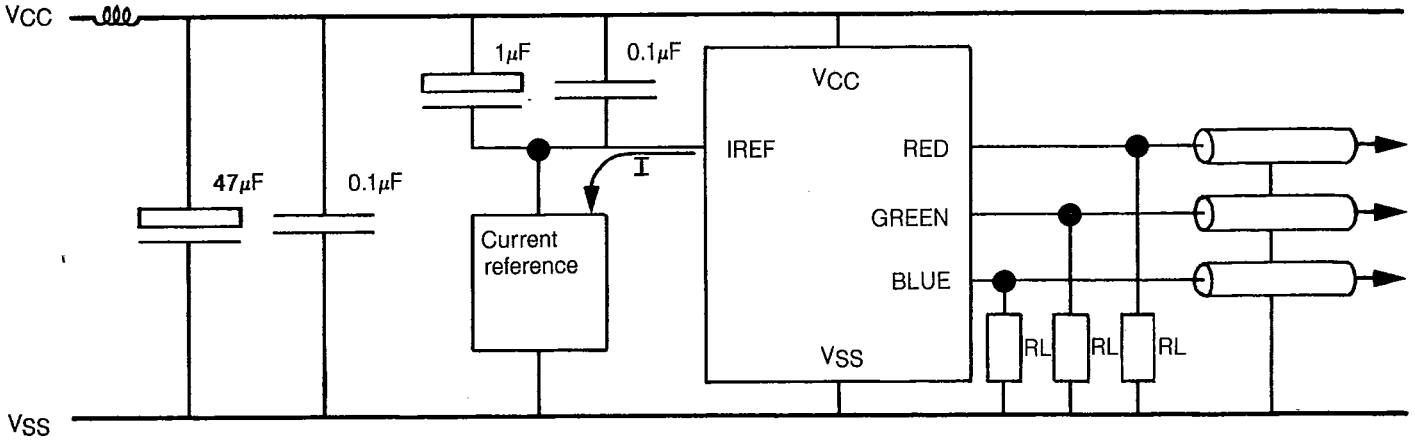
The IMSG170 has no on chip power supply rejection to analog outputs. To ensure proper operation in a system environment it is recommended that the following guidelines are followed.

POWER DISTRIBUTION

Transient currents are required by high speed CMOS circuitry such as the IMSG170. These transient current spikes can cause significant power supply and ground noise unless adequate power distribution and decoupling is used. The recommended power distribution scheme combines proper layout and placement of decoupling capacitors. A ground plane and locally isolated V_{CC} supply, as shown below, will help to minimize V_{CC} noise generated by eternal circuitry. A high frequency decoupling capacitor with value of 0.1μF and a larger tantalum capacitor with a value of 47μF should be placed in parallel between V_{CC} and V_{SS} as close as possible to the device.

CURRENT REFERENCE

The current reference (IREF) input to the IMSG170 provides an onboard voltage reference by sourcing a current from the V_{CC} supply. To prevent noise modulating the analog outputs the current reference should be as stable as possible and decoupled to V_{CC}. To minimize cross-talk onto IREF the current source should be sited as close as possible to the IMSG170 and a ground plane should be used.



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