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Innovating the HP Way

DC – 12 GHz Packaged High Efficiency Divide-by-4 Prescaler

Technical Data

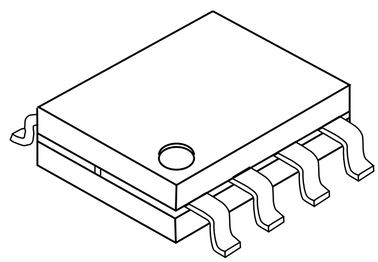
HMMC-3124

Features

- **Wide Frequency Range:** 0.2 - 12 GHz
- **High Input Power Sensitivity:** On-chip pre- and post-amps
  -15 to +10 dBm (1 - 8 GHz)
  -10 to +8 dBm (8 - 10 GHz)
  -5 to +2 dBm (10 - 12 GHz)
- **P_{out}:** 0 dBm (0.5 V_{p-p})
- **Low Phase Noise:** -153 dBc/Hz @ 100 kHz Offset
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range:** 4.5 to 6.5 volt operating range
- **Differential I/0 with on-chip 50Ω matching**

Description

The HMMC-3124 is a packaged GaAs HBT MMIC prescaler which offers DC to 12 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.



Package Type:	8-lead SSOP Plastic
Package Dimensions:	4.9 x 3.9 mm Typ.
Package Thickness:	1.55 mm Typ.
Lead Pitch:	1.25 mm Nom.
Lead Width:	0.42 mm Nom.

Absolute Maximum Ratings[1]

(@ T_A = 25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{CC}	Bias Supply Voltage	volts		+7
V_{EE}	Bias Supply Voltage	volts	-7	
$\|V_{CC} - V_{EE}\|$	Bias Supply Delta	volts		+7
V_{Logic}	Logic Threshold Voltage	volts	V_{CC}-1.5	V_{CC}-1.2
$P_{in(CW)}$	CW RF Input Power	dBm		+10
V_{RFin}	DC Input Voltage (@ RF_{in} or $\overline{RF}_{in}$ Ports)	volts		$V_{CC} \pm 0.5$
T_{BS}[2]	Backside Operating Temp.	°C	-40	+85
T_{STG}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp. (60 seconds max.)	°C		310

Notes:
1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10^6 hours @ T_{BS} < 85°C. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

HMMC-3124 DC Specifications/Physical Properties,

(T_A = 25°C, V_{CC} - V_{EE} = 5.0 V unless otherwise listed)

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
V_{CC} - V_{EE}	Operating Bias Supply Difference[1]	volts	4.5	5.0	6.5
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias Supply Current	mA	34	40	46
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent DC Voltage appearing at all RF Ports	volts		V_{CC}	
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	volts	V_{CC} - 1.45	V_{CC} - 1.32	V_{CC} - 1.25

Note:

1. Prescaler will operate over full specified supply voltage range. V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.

RF Specifications, (T_A = 25°C, Z_O = 50Ω, V_{CC} - V_{EE} = 5.0 V)

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
$f_{in(max)}$	Maximum input frequency of operation	GHz	12	14	
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)	GHz		0.2	0.5
$f_{Self-Osc.}$	Output Self-Oscillation Frequency[2]	GHz		3.4	
P_{in}	@ DC, (Square-wave input)	dBm	-15	>-25	+10
	@ f_{in} = 500 MHz, (Sine-wave input)	dBm	-15	>-20	+10
	f_{in} = 1 to 8 GHz	dBm	-15	>-20	+10
	f_{in} = 8 to 10 GHz	dBm	-10	>-15	+5
	f_{in} = 10 to 12 GHz	dBm	-5	>-10	-1
RL	Small-Signal Input/Output Return Loss (@ f_{in} < 12 GHz)	dB		15	
S_{12}	Small-Signal Reverse Isolation (@ f_{in} < 12 GHz)	dB		30	
φ_N	SSB Phase Noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz Carrier)	dBc/Hz		-153	
Jitter	Input Signal Time Variation @ Zero-Crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)	ps		1	
T_r or T_f	Output Transition Time (10% to 90% rise/fall time)	ps		70	
P_{out}[3]	@ f_{out} < 1 GHz	dBm	-2.0	0	
	f_{out} = 2.5 GHz	dBm	-3.5	-1.5	
	f_{out} = 3.5 GHz	dBm	-4.5	-2.5	
$\|V_{out(p-p)}\|$[4]	@ f_{out} < 1 GHz	volts		0.5	
	f_{out} = 2.5 GHz	volts		0.42	
	f_{out} = 3.5 GHz	volts		0.37	
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, Unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)	dBm		-50	
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 12 GHz, Both RF_{out} & $\overline{RF}_{out}$ **terminated**)	dBm		-55	
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, Referred to $P_{in}(f_{in})$)	dBc		-30	
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, Referred to $P_{out}(f_{out})$)	dBc		-25	

Notes:

1. For sine-wave input signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler can exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the input DC offset technique described on page 3.
3. Fundamental of output square wave's Fourier Series.
4. Square wave amplitude calculated from P_{out}.

Applications

The HMMC-3124 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 16 GHz bandwidth. Below 200 MHz the prescaler input is “slew-rate” limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to DC when driven with a squarewave. AC coupling at pin 5 (RF_{in}) is recommended for most applications.

The device can be operated from either a single positive or single negative supply. For positive supply operation V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with pin 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to pin 8 (V_{EE}).

Input DC Offset

To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV DC offset voltage between the RF_{in} and $\overline{RF}_{in}$ ports. This prevents noise or spurious low level signals from triggering the divider.

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

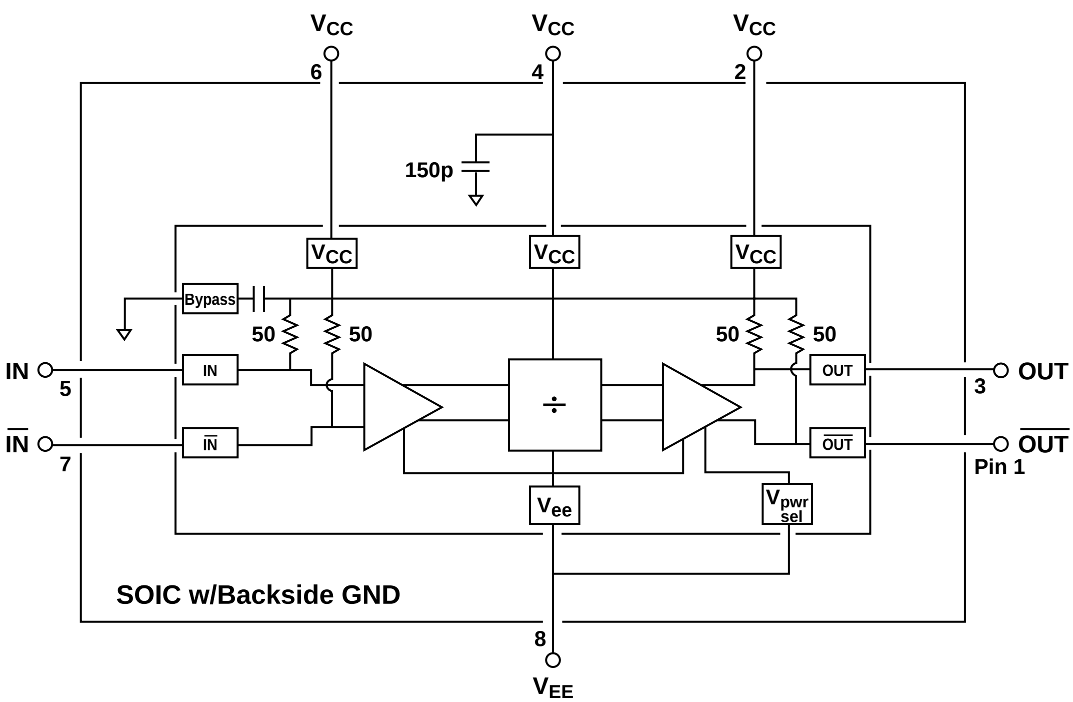


Figure 1. HMMC-3122 Simplified Schematic.

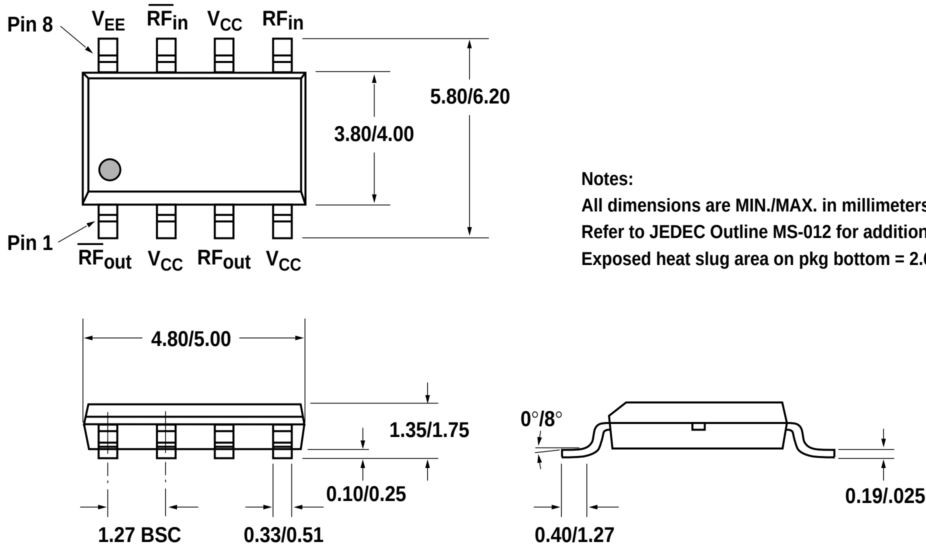


Figure 2. Package and Dimensions.

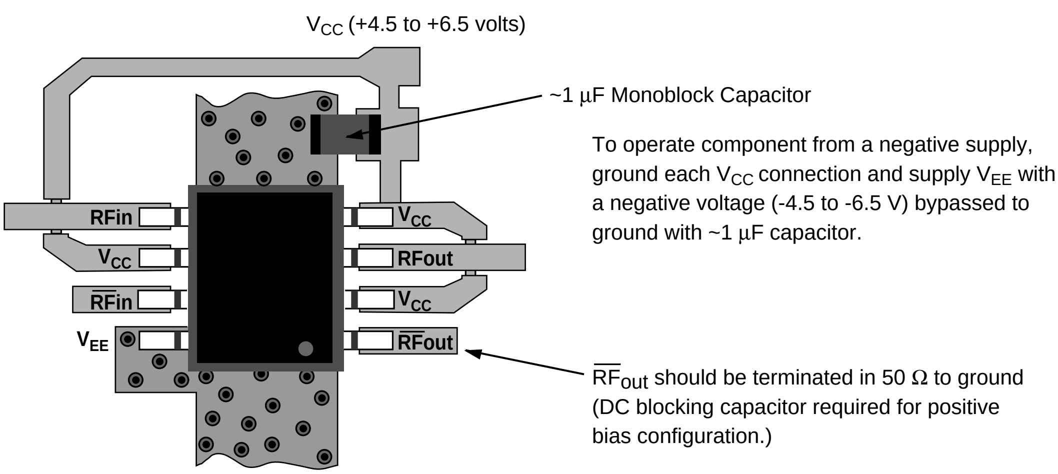


Figure 3. Assembly Diagram. (single-supply, positive-bias configuration shown)

HMMC-3124 Supplemental Data

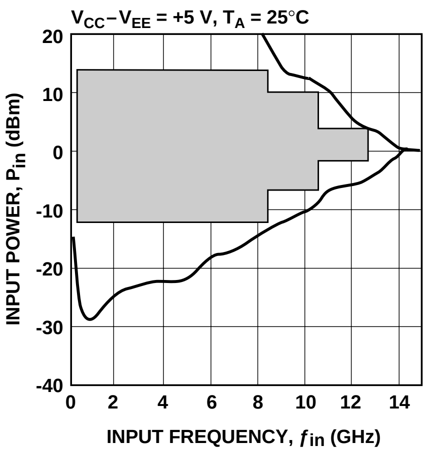


Figure 4. Typical Input Sensitivity Window.

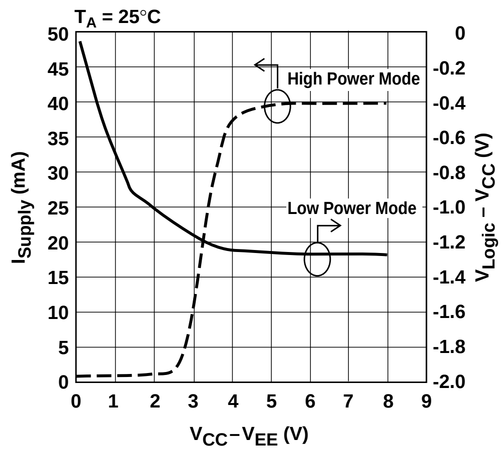


Figure 5. Typical Supply Current & V_{Logic} vs. Supply Voltage.

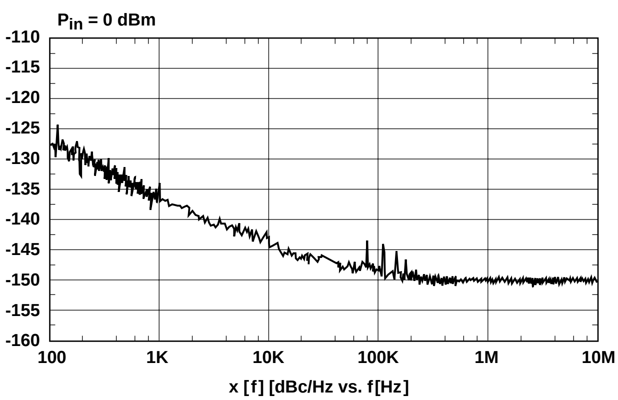


Figure 6. Typical Phase Noise Performance.

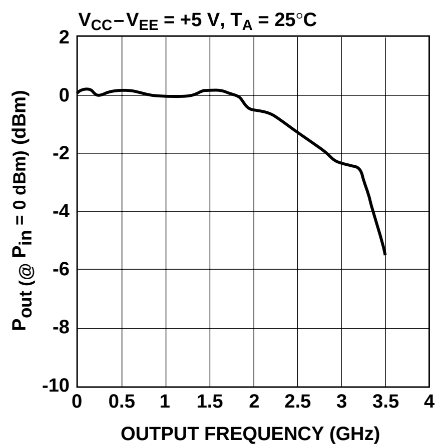


Figure 7. Typical Output Power vs. Output Frequency, f_{out} (GHz).

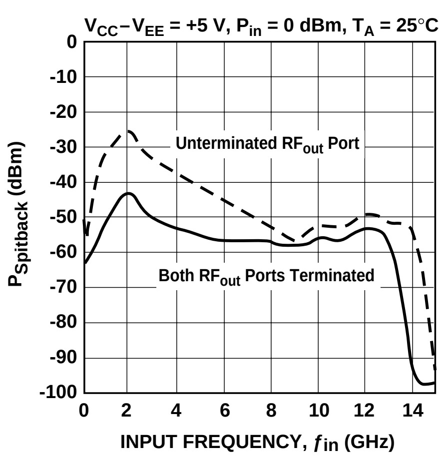


Figure 8. Typical *"Spitback"* Power. $P(f_{out})$ appearing at RF input port.

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Supplemental Information

Input DC Offset

As long as an RF signal is always present and within the input power specifications, there will not be any problems with false triggering or self-oscillations. If this is not the case, you can put ≈10KΩ to ground from the unused input and this, when combined with the on-chip 50Ω resistor to V_{CC} = 5, will put an offset of ≈25 mV between the RF inputs (i.e., if $\overline{RF}_{in}$ has 10KQ to ground, it will be at ≈4.975 V and RF_{in} will be at ≈5V). If you want a 20 to 100 mV offset per the note on page 3, the resistor value to ground will be 12.45KΩ to 2.45KΩ when V_{CC} = 5.

Biasing and DC-Blocking

The backside of the divider chip is gold plated and attached to the heat slug in the package. Also in the package is a capacitor connected between the chip's topside V_{CC} rail and the heat slug making the heat slug an RF ground. In the majority of cases, you would tie the exposed heat slug on the bottom of the package to ground. In a typical positive bias setup with V_{CC} = 5, V_{EE} is DC ground along with the package's heat slug. The RF input and RF output nodes are each tied to V_{CC} through 50Ω and will be floating nominally at that bias level (depending, of course, on the input drive level and the appropriate output state) so blocking capacitors will usually be required. For a typical negative bias setup with V_{EE} = -5, V_{CC} is DC ground along with the package's heat slug. In some cases, such as level shifting to subsequent stages, you might want to "float" the package and apply bias as the difference between V_{CC} and V_{EE}. For such applications, the package's heat slug must be attached to a point that is both a good heat sink and a good RF ground.

Heat Slug/Bonding Pad

The exposed area of the package's backside heat slug (or pad) measures 2.67 x 1.65 mm (0.105" x 0.065"). Anything larger than this on a PCB would be at the customer's preference or convenience. On our test PCBs, we use a 0.200" x 0.082" pad with eight 0.020" diameter solder-filler thermal vias.

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Data subject to change.

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