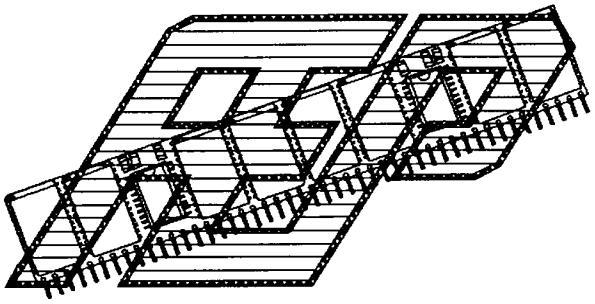
- >> *1,048,576 x 16 Organization*
- >> *On board Registers for all address and chip enable lines.*
- >> *Double sided to maximize bit density*
- >> *Completely Static operation*
- >> *TTL compatible*
- >> *Uses single +5V power supply*



1 MEGAWORD BY 16 BIT HIGH SPEED STATIC RAM MODULE WITH ON-BOARD REGISTERS

DESCRIPTION:

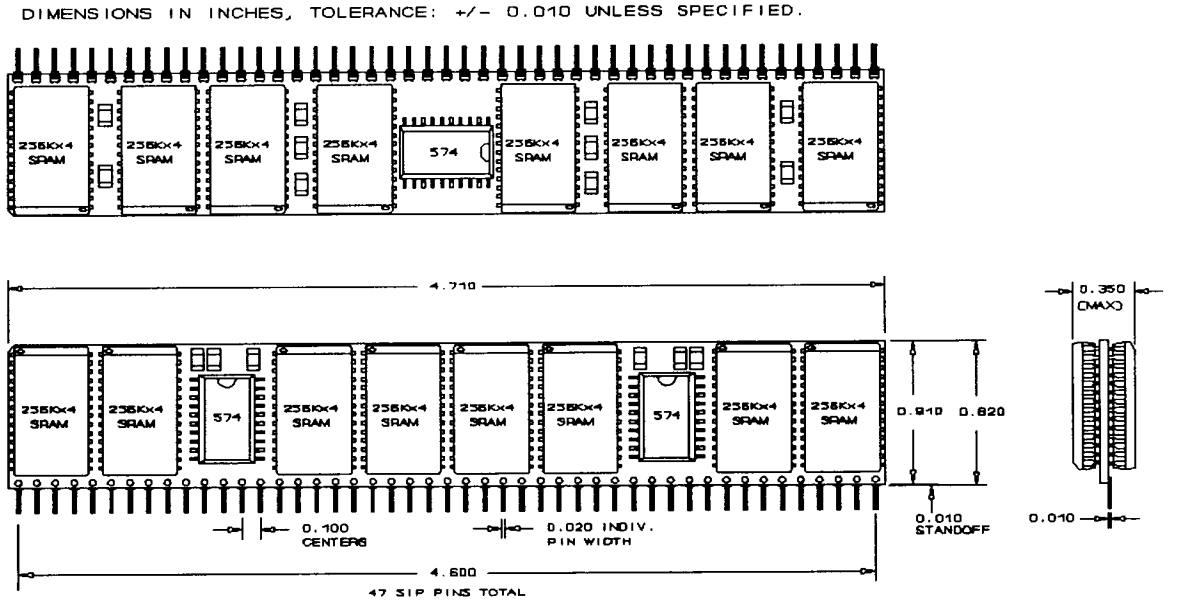
The AEPSS1M16 is a high speed, high density 1 megaword by 16 bit static random access memory module with on board registers. The registers on the module allow for high speed pipelining, which is ideal for use in today's high speed microprocessor systems that require quick and reliable memory.

Performance specifications and electrical characteristics are determined by the IC devices used. A typical memory component module will draw 0.8mW (typical) in standby mode and 2800mW (typical) during access.

The module can use any 256Kx4 SRAM ICs with SOJ lead packages and standard pin-out made by any of variety of manufacturers in both Mix-CMOS technologies. A wide range of access speeds are available. The register normally used is the 74F574, please check with AEP for the availability and compatibility of other technologies.

Physically it consists of an FR4 PC material substrate surface mounted with sixteen 256Kx4 high speed SRAM ICs, three 74F574 ICs, sixteen 0.10 microfarad decoupling capacitors, and 47 press-in I/O pins in a single in-line packaging (SIP) format. Mechanical dimensions are 0.820 in. high by 4.710 in. long by 0.350 in. wide. The SIP I/O pins are on 0.1 inch center spacing.

SPECIFICATION DRAWING
1M x 16 SRAM MODULE



1M x 16 STATIC RAM MODULE

SIP PIN-OUT CONFIGURATION

1	I/O_1
2	I/O_2
3	I/O_3
4	I/O_4
5	VCC
6	OE_L*
7	WE_L*
8	A_0
9	A_1
10	A_2
11	A_3
12	A_4
13	A_5
14	A_6
15	GND
16	I/O_5
17	I/O_6
18	I/O_7
19	I/O_8
20	A_7
21	A_8
22	CS_1*
23	CS_2*
24	CLK
25	CS_3*
26	CS_4*
27	A_9
28	A_{10}
29	I/O_9
30	I/O_{10}
31	I/O_{11}
32	I/O_{12}
33	GND
34	A_{11}
35	A_{12}
36	A_{13}
37	A_{14}
38	A_{15}
39	A_{16}
40	A_{17}
41	WE_H*
42	OE_H*
43	VCC
44	I/O_{13}
45	I/O_{14}
46	I/O_{15}
47	I/O_{16}

* ACTIVE WHEN LOW

FUNCTIONAL DIAGRAM